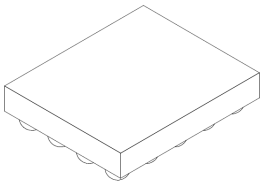
TOSHIBA CMOS Integrated Circuit Silicon Monolithic

TC94B15WBG

DAC + Stereo Headphone Amplifier with Electronic Volume

The TC94B15WBG is a DAC + stereo headphone amplifier IC. It is built in stereo DAC and an G-class stereo headphone amplifier with electric volume function.

It is suitable for mobile phone and digital audio player etc.



S-UFBGA20-0303-0.50A01

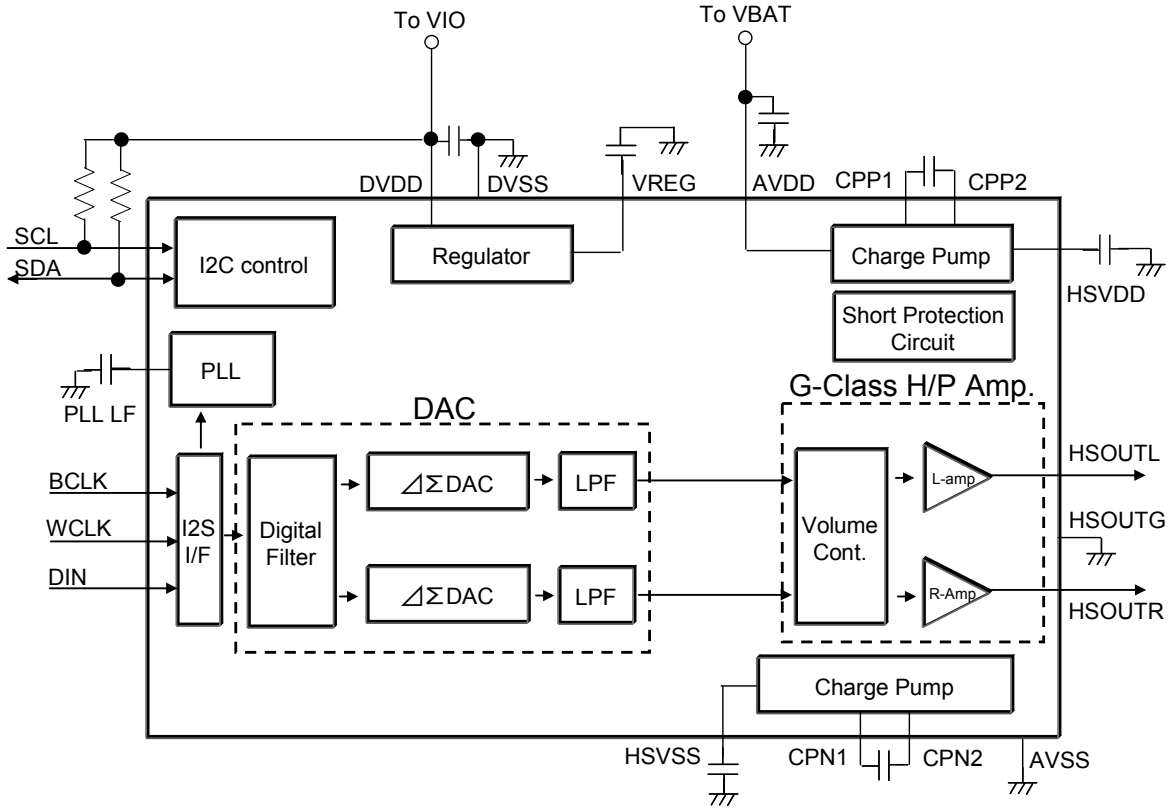
Weight: 7.0mg (typ.)

Marking: B15WBG

Features

- I²C control Bus
- DA converter
  - I2S input compatible
    Data bits : 16bit
    Sampling rate : 48kHz
- G-class Headphone Amplifier
  - Output Coupling Capacitor-less
- Low supply current
  IDDQ(DVDD) : 1.8mA(Typ.)
  IDDQ(AVDD) : 2.2mA(Typ.)
- High Sound Quality : S/N = 92dB(Typ. AES17+CCIR Weighting)
- Electric Volume : 32steps and mute
- Package WCSP 20pin , 0.5mm pitch
- Operating temperature range
  T(opr) = -30 to 85℃
- Operating supply voltage range: Ta = 25℃
  DVDD(opr) = 1.65 to 1.95V
  AVDD (opr) = 2.3 to 4.8V

Block Diagram



Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

Pin Assignment (Top View : Marking side)

A1 AVSS	A2 CPP2	A3 CPP1	A4 CPN1	A5 CPN2
B1 PLL LF	B2 AVDD	B3 VREG	B4 DVDD	B5 DVSS
C1 SDA	C2 SCL	C3 HS OUTG	C4 HSVDD	C5 HSOUTL
D1 BCLK	D2 WCLK	D3 DIN	D4 HSOUTR	D5 HSVSS

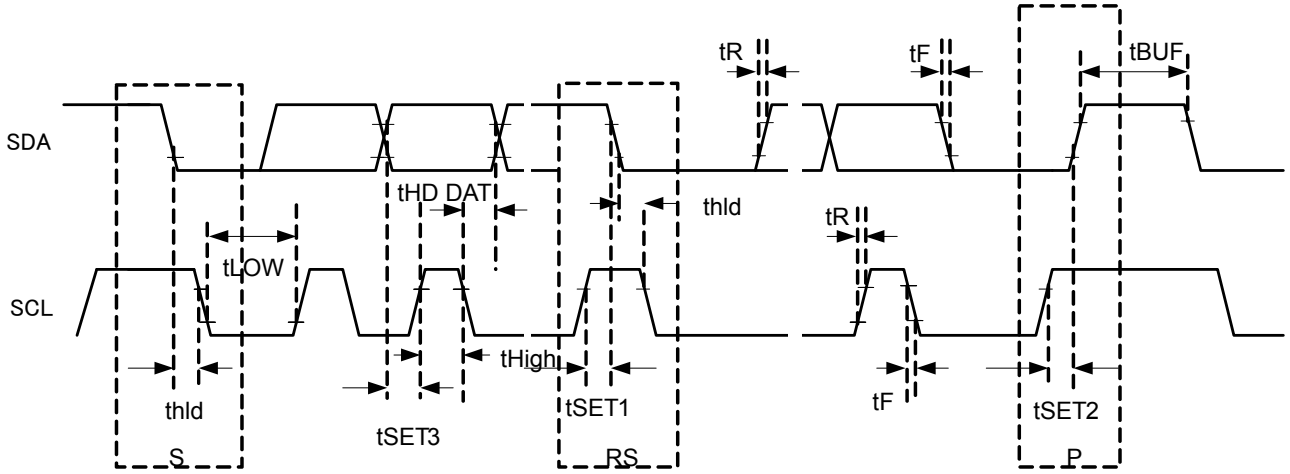
Pin Descriptions

Pin No. and name		I/O	Function	Note
A1	AVSS	–	Analogue ground	—
A2	CPP2	—	Positive voltage of charge pump flying capacitor. Negative terminal	—
A3	CPP1	—	Positive voltage of Charge pump flying capacitor. Positive terminal	—
A4	CPN1	—	Negative voltage of charge pump flying capacitor. Positive terminal	—
A5	CPN2	—	Negative voltage of charge pump flying capacitor. Negative terminal	—
B1	PLL LF	-	PLL loop filter pin	—
B2	AVDD	–	Analogue voltage supply. Connected to Vbat	—
B3	VREG	–	Output from Digital stage regulator circuit	—
B4	DVDD	–	Digital voltage supply. Connected to VIO	—
B5	DVSS	–	Digital ground	—
C1	SDA	I/O	I^2C data	—
C2	SCL	I	I^2C serial clock	—
C3	HSOUTG	–	Output ground	—
C4	HSVDD	–	Positive voltage of charge pump output	—
C5	HSOUTL	O	Amplifier output left	—
D1	BCLK	I	Audio serial data bus bit clock	—
D2	WCLK	I	Audio serial data bus word clock	—
D3	DIN	I	Audio serial data bus data	—
D4	HSOUTR	O	Amplifier output right	—
D5	HSVSS	—	Negative voltage of charge pump output	—

Functional Description

1. I²C control
This IC supports the I²C control protocol using 8-bit addressing and is capable of both standard and fast modes.

(1) I²C interface timing.



S : Start, RS : Re-start, P : Stop

Figure 1 I²C Interface Timing

Timing chart may be simplified for explanatory purpose.

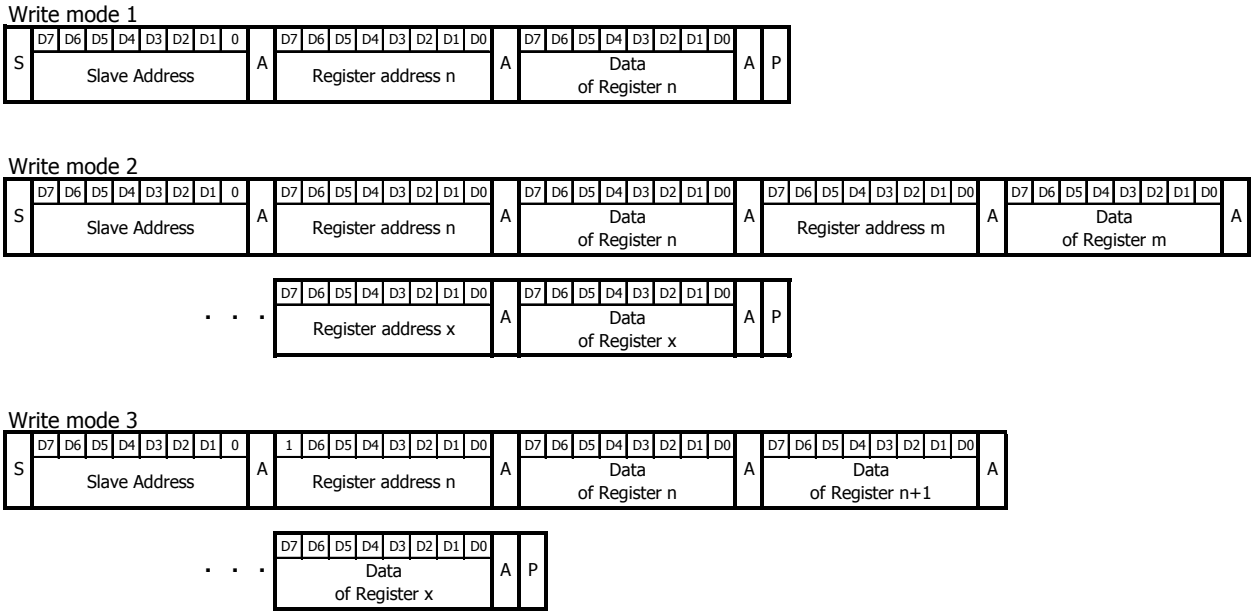
Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SCL Clock frequency	fSCL	—	—	—	400	kHz
Hold time, start condition to SCL	thld	—	0.6	—	—	μs
Setup time, SCL to start condition	tSET1	—	0.6	—	—	μs
Setup time, SCL to stop condition	tSET2	—	0.6	—	—	μs
Data setup time	tSET3		100	—	—	ns
Bus free time between stop and start condition	tBUF	—	1.3	—	—	μs
SCL clock width “Low”	tLOW	—	1.3	—	—	μs
SCL clock width “High”	tHigh	—	0.6	—	—	μs
SCL / SDA rise time	tR	—	—	—	300	ns
SCL / SDA fall time	tF	—	—	—	300	ns
Data hold time	tHD DAT	—	0	—	—	μs

Table 1 I²C Characteristics

(2) Write mode

In the case that other serial I²C data are newly transmitted after one transmission, it is necessary to open the term more than one clock cycle.

And this IC supports the following 3 formats.



S : Start condition, A : Acknowledge, P : Stop condition

Figure 2 Format of write mode

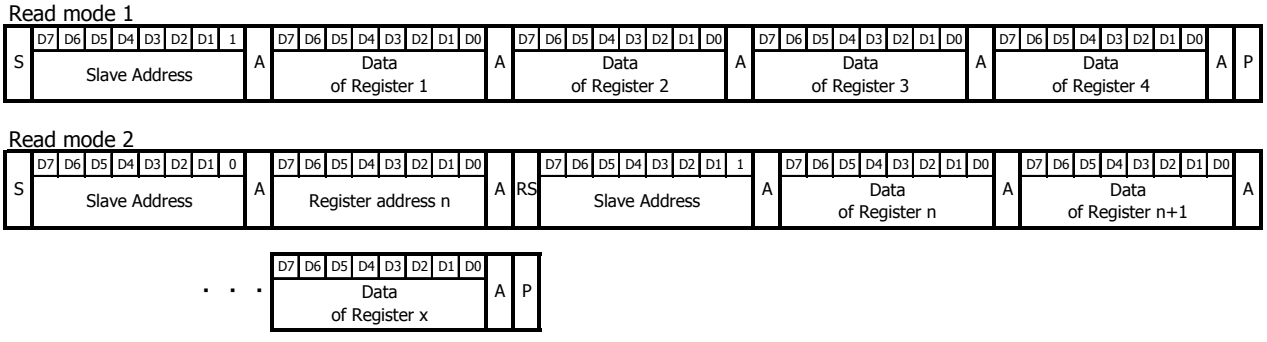
(3) Read mode

The slave address became the read mode by changing the 8 Bit of the slave address from 0 to 1.

The micro controller shall send the stop condition P after it sent the reversed Acknowledge (high) in case of the read mode finished.

The data transmission became not available condition if the micro controller intended to send the stop condition P expect for this procedure because this IC occupies the data bus until the micro controller send the start conditions again.

And this IC supports the following 2 formats.



S : Start condition, A : Acknowledge, RS : Repeat start condition, P : Stop condition

Figure 3 Format of read mode

1-1. Slave address

Writing mode : 0x34

Reading mode : 0x35

1-2. Register map

Register Address	D7	D6	D5	D4	D3	D2	D1	D0	Preset
0x01	HSL_EN	HSR_EN	0	0	0	0	Thermal	CHIP_ EN	0x00
0x02	HSL_MUTE	HSR_MUTE	VOL (4)	VOL (3)	VOL (2)	VOL (1)	VOL (0)	0	0xC0
0x03	0	0	0	0	0	0	HIZ_L	HIZ_R	0x00

Note

The register address is for TOSHIBA testing from 0x04.

Under no circumstances must any data be written to these registers. Writing to these bits may change the function of device, or complete failure. If read, these bits may assume any value.

* 0x01

Bit	Name	Read/ Write	Value	Description	Preset
D7	HSL_EN	R/W	0	Disable left headset driver	0
			1	Enable left headset driver	
D6	HSR_EN	R/W	0	Disable right headset driver	0
			1	Enable right headset driver	
D5:D2	-	-	0	Reserved	0
D1	Thermal	R	0	Thermal shutdown not activated	0
			1	Thermal shutdown activated	
D0	CHIP_EN	R/W	0	Disable IC	0
			1	Enable IC	

0x02

Bit	Name	Read/ Write	Value	Description	Preset
D7	HSL_MUTE	R/W	0	Headset Left un-mute	1
			1	Headset Left mute	
D6	HSR_MUTE	R/W	0	Headset Right un-mute	1
			1	Headset Right mute	
D5:D1	VOL	R/W	-	Volume level. See Volume table	00000
D0	-	-	0	Reserved	0

0x03

Bit	Name	Read/ Write	Value	Description	Preset
D7:D2	-	-	0	Reserved	000000
D1	HIZ_L	R/W	0	Left channel normal impedance	0
			1	Left channel high impedance	
D0	HIZ_R	R/W	0	Right channel normal impedance	0
			1	Right channel high impedance	

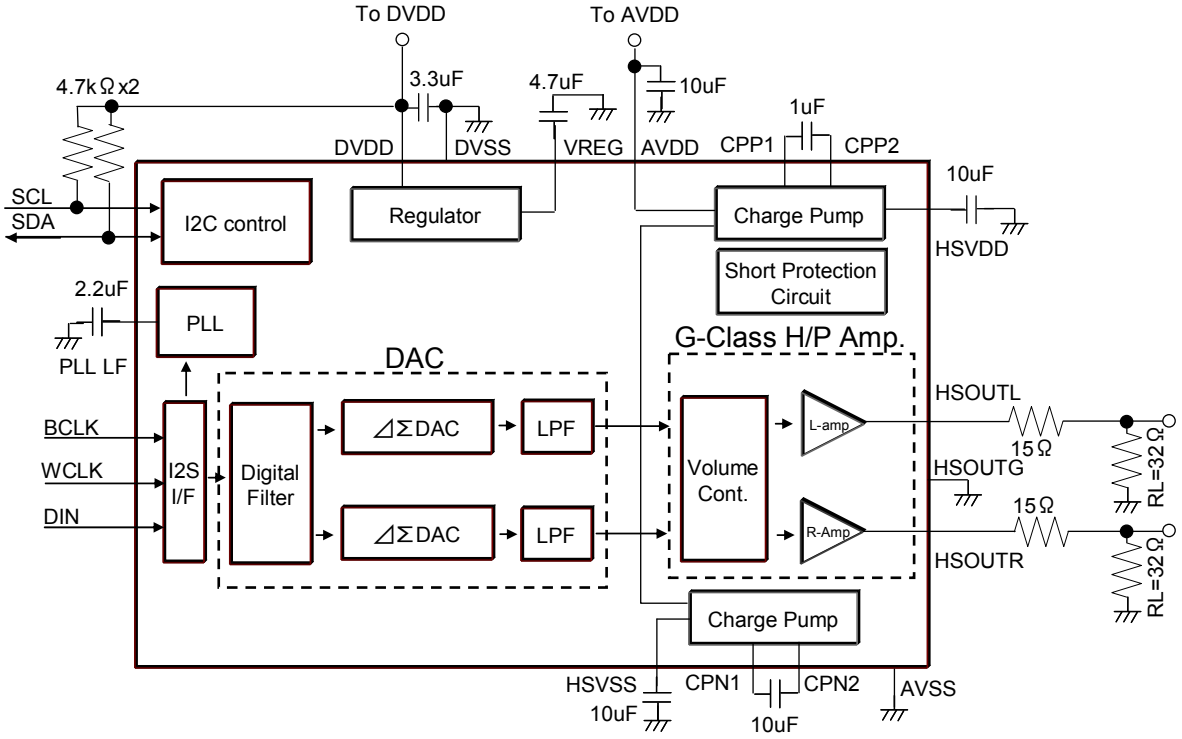
1-3. Volume table

Gain control Mute[7:6], Volume[5:0]	Read/ Write	Gain [dB]	Output level (rms) [mVrms]	Gain control Mute[7:6], Volume[5:0]	Read/ Write	Gain [dB]	Output level (rms) [mVrms]
10xx xxxx	R/W	Mute_Lch		0001 111x	R/W	-13	98.9
01xx xxxx		Mute_Rch		0010 000x		-11	124
0000 000x		-59	0.5	0010 001x		-10	14
0000 001x		-55	0.79	0010 010x		-9	157
0000 010x		-51	1.24	0010 011x		-8	176
0000 011x		-47	1.97	0010 100x		-7	197
0000 100x		-43	3.13	0010 101x		-6	221
0000 101x		-39	4.94	0010 110x		-5	248
0000 110x		-35	7.85	0010 111x		-4	279
0000 111x		-31	12.4	0011 000x		-3	313
0001 000x		-27	19.7	0011 001x		-2	351
0001 001x		-25	24.8	0011 010x		-1	394
0001 010x		-23	31.3	0011 011x		0	442
0001 011x		-21	39.4	0011 100x		1	496
0001 100x		-19	49.6	0011 101x		2	556
0001 101x		-17	62.4	0011 110x		3	624
0001 110x		-15	78.5	0011 111x		4	700

Level definition

DVDD=1.8V, AVDD=3.7V, Din=0dBFS, fWCLK=48kHz, fin=1kHz, RL=15+32Ω(Measurement point :32Ω), Ta=25℃

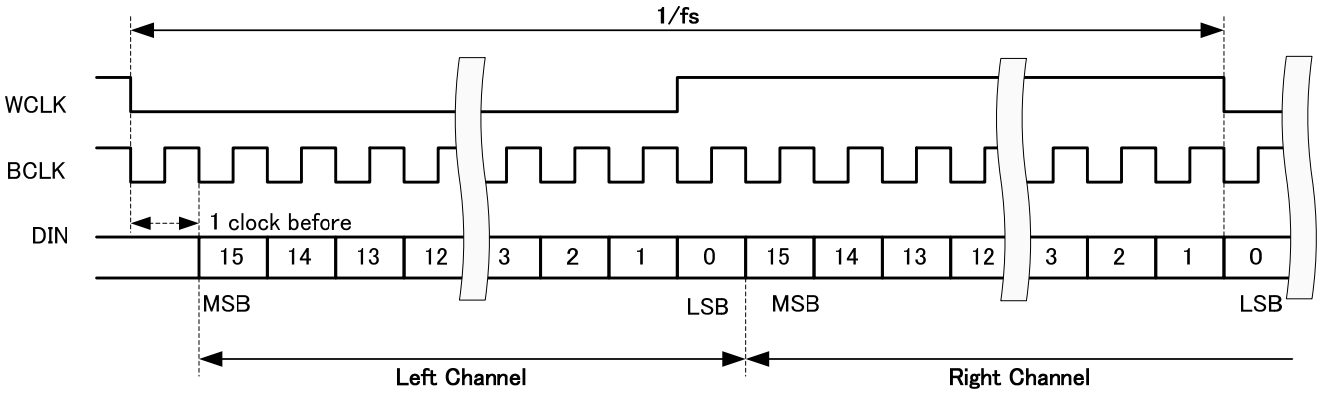
Circuit definition



2. I2S control
The I2S of this IC supports the following format.
Data bits : 16bit
Sampling rates : 48kHz
Slave mode operation

The volume mute should be applied when the format is changed via I²C.

3-1 I2S Serial data bus mode operation
* Left channel
The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock.
* Right channel
The MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.



Note : WCLK = 32 BCLK

Figure 4 I2S Mode operation

3-2 I2S Interface Timing

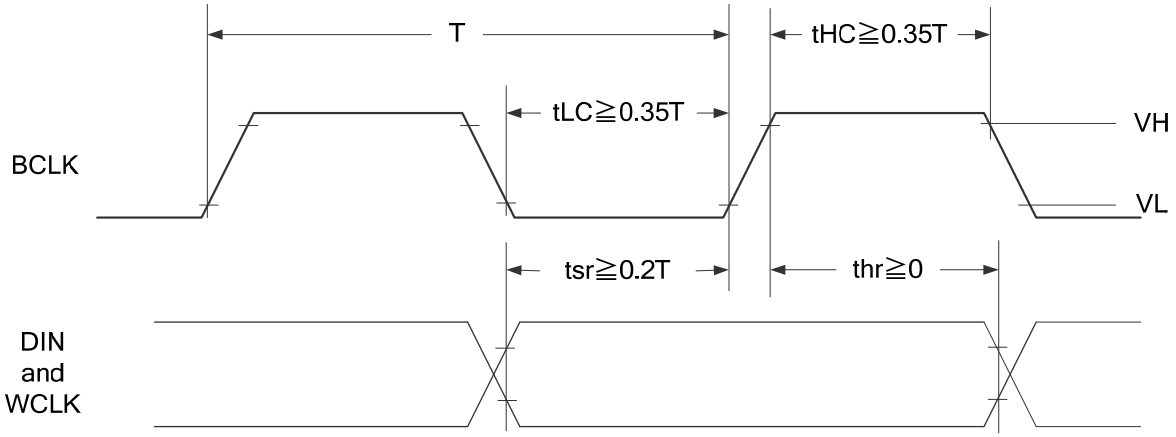


Figure 5 I2S Receiver timing

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Clock Period	T	644.5	651	657.5	ns
Control Voltage (H)	VH	0.65xDVDD	—	—	V
Control Voltage (L)	VL	—	—	0.35xDVDD	V
Clock High	tHC	200	—	—	ns
Clock Low	tLC	200	—	—	ns
Set-up Time	tsr	100	—	—	ns
Hold Time	thr	0	—	—	ns

Table 2 I2S Characteristics

4. Power on sequence

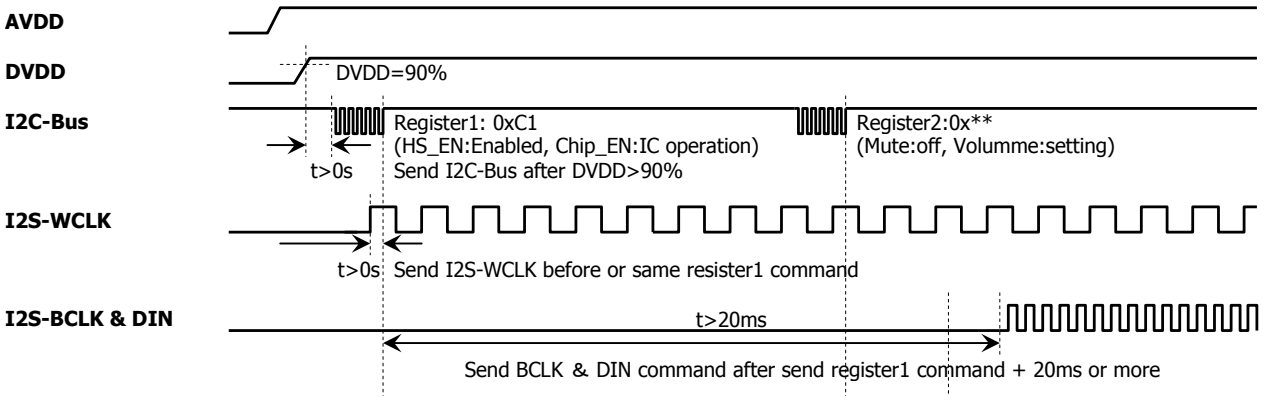


Figure 6 Power on sequence

5. Power off sequence (Tentative)
WCLK signal must not be stopped until chip_EN is set "disenabled",
because it prevent the error of PLL circuit.
On the other hand, there is no problem even if WCLK remains after chip_EN is set to "disenabled".

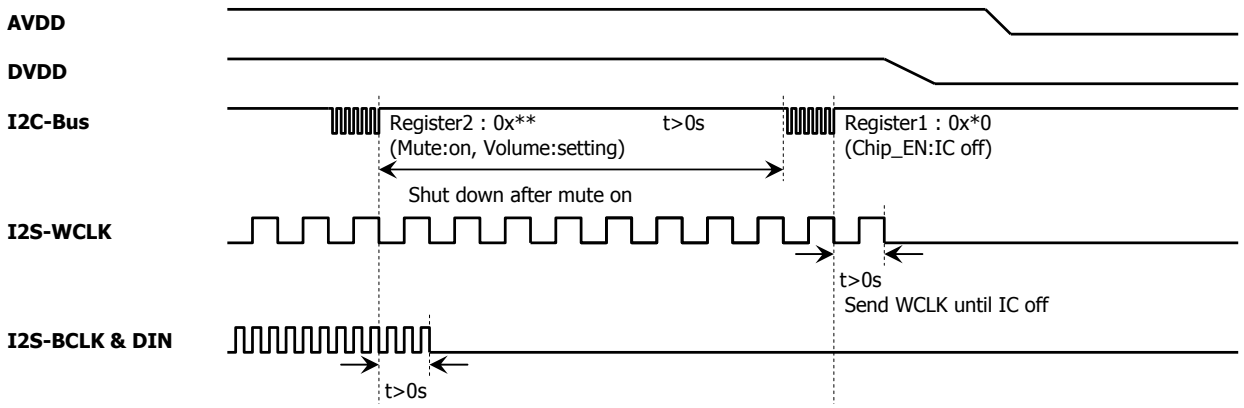


Figure 7 Power off sequence

6. DAC
The DAC system incorporate a multi-bit ⊿Σ type of 128fs.

7. Charge pump Circuit
This IC adopts the charge pump circuit of the inductor-less type, therefore it hold down the external parts cost.
This circuit has 2 mode operations. And it is decided by headphone output power and AVDD.
It explains as an example of the positive power source.

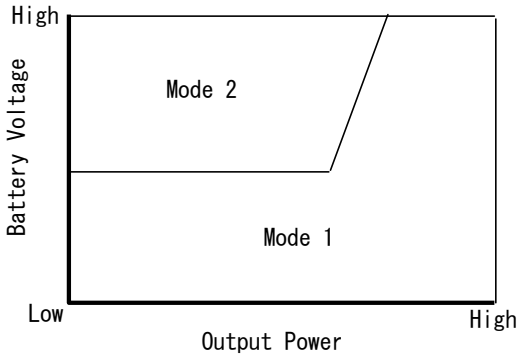


Figure 8 Operation mode of Charge Pump

Mode 1
The system is shown in figure 9.
The switch is set to "a" side, and the 1uF is charged by AVDD voltage source. Then the switch is changed by the switching frequency circuit of charge pump to "b" side. The internal circuit is operated by the electric charge of 1uF.

Mode 2
The system is shown in figure 10. The switch is set to "a" side, and the 1uF and 10uF are charged by AVDD voltage source. Then the switch is changed by the switching frequency circuit of charge pump to "b" side.
The internal circuit is operated by the electric charge of 1uF.

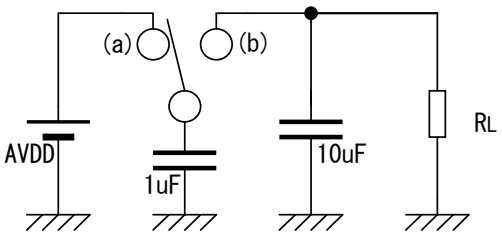


Figure 9 Mode 1 of Charge pump operation

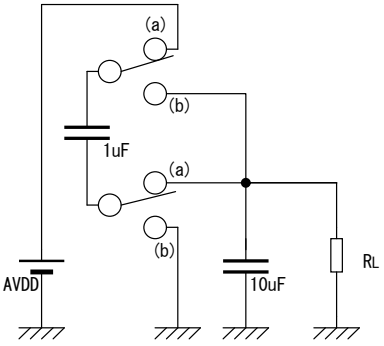


Figure 10 Mode 2 of Charge pump operation

About the negative voltage source, the operation mode is 1 anytime.

8. Amplifier
This IC adopts the G-class method, therefore the power efficiency is higher than the AB-Class.
And the output coupling capacitor is unnecessary because it is built in the negative voltage source.

9. Protection circuit
This IC built in the over current detection type of protection circuit.
The flow chart of the protection circuit is the following.

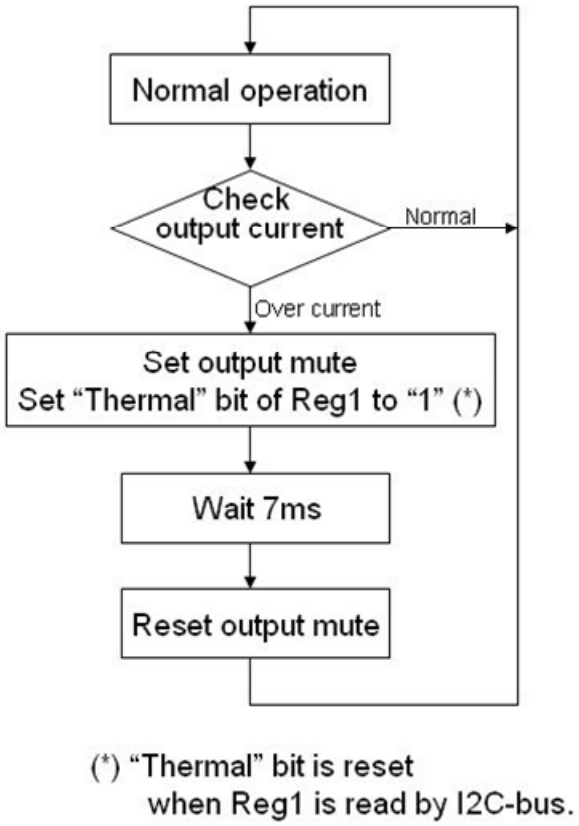


Figure 11 Flow chart of protection circuit

Register Address	Bit	Name	Read/ Write	Value	Description
0x01	D1	Thermal	R	0	Thermal shutdown not activated
				1	Thermal shutdown activated

Table 3 Operation mode of protection circuit

These protection functions are intended to avoid some output short circuits or other abnormal conditions temporarily. These protect functions do not warrant to prevent the IC from being damaged.
In case of the product would be operated with exceeded guaranteed operating ranges, these protection features may not operate and some output short circuits may result in the IC being damaged.
The over-current protection feature in only intended to protect the IC from a temporary circuit.
Long time short circuit may stress excessively on the IC to be damaged. The system must be configured so that any over-current condition will be eliminated as soon as possible.

10. OUT GND
This IC has OUT GND pin.
In case the GND of earphone code uses the tuner antenna, this pin connect with headphone jack GND.
Then the separation characteristic can keeps.
If the set don't have tuner application, this pin connect with AVSS pin.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	AVDD	-0.3 to 5.5	V
	DVDD	-0.3 to 2.2	V
Breakdown Voltage at amplifier outputs	Vo	5.5	V
Lead temperature	Tlead	240	℃
Power dissipation	P_D (Note)	2	W
Operating temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−55 to 105	°C

Note: IC+PCB Derated by 20 mW/°C above Ta = 25°C

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.
If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed.
Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment.
Applications using the device should be designed such that each absolute maximum rating will never be exceeded in any operating conditions.
Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

Electrical Characteristics

Unless otherwise specified, DVDD = 1.8V, AVDD = 3.7V, Ta = 25°C

DC Characteristics

Characteristics	Symbol	Test circuit	Test Condition	Min	Typ.	Max	Unit
Shutdown current	ISD(DVDD)	2	SW shutdown	—	—	1	μA
	ISD(AVDD)			—	—	3	μA
Quiescent Current	IDDQ(DVDD)	2	Both channels enabled. No audio signal	—	1.8	2.2	mA
	IDDQ(AVDD)			—	2.2	2.8	mA
Supply Current	IDD	2	0.1mW*2ch, 10dB Crest Factor	—	—	6	mA
			0.5mW*2ch, 10dB Crest Factor	—	—	8	mA
Wake up time	Twake	2		—		20	ms
Output Impedance	Zout1	4	HiZ mode, f＜40kHz	10	45	—	kΩ
	Zout2	5	HiZ mode, f=6MHz	500	640	—	Ω
	Zout3	5	HiZ mode, f=36MHz	—	135	—	Ω
Output DC offset	⊿Vo	2	Both channels enabled	—	—	500	uV
Control Voltage (H)	Vih	2	DVDD=1.65 to 1.95V	0.65x DVDD	—	DVDD	V
Control Voltage (L)	Vil	2	DVDD=1.65 to 1.95V	0	—	0.35x DVDD	V
Input Current (H)	Iih	2	I2S/I^2C pin, Vih=DVDD	—	—	1	uA
Input Current (L)	Iil	2	I2S/I^2C pin, Vil=0V	—	—	1	uA

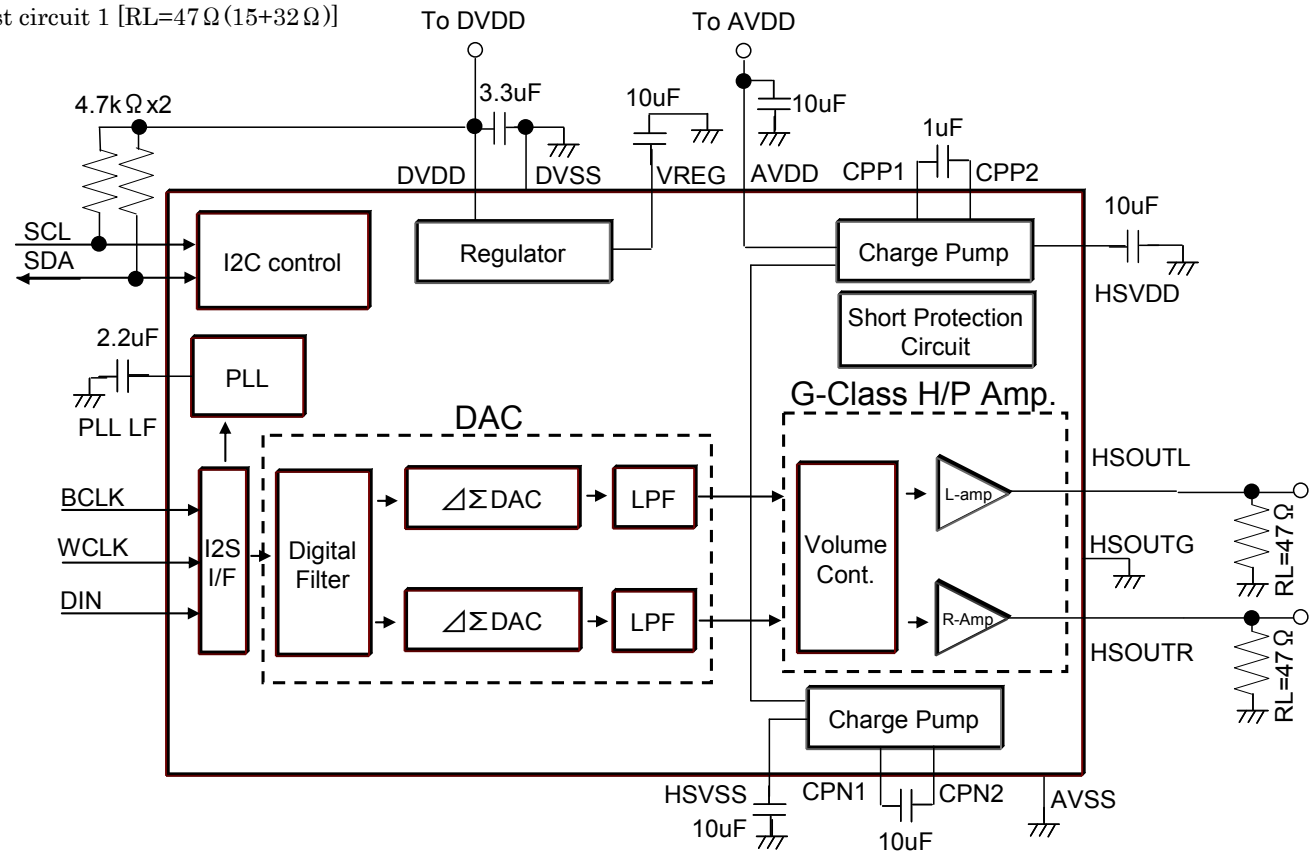
Unless otherwise specified,
DVDD = 1.8V, AVDD = 3.7V, Din=0dBFS, fWCLK=48kHz, fin=1kHz, Gv=+4dB,
Ta = 25°C

AC Characteristics

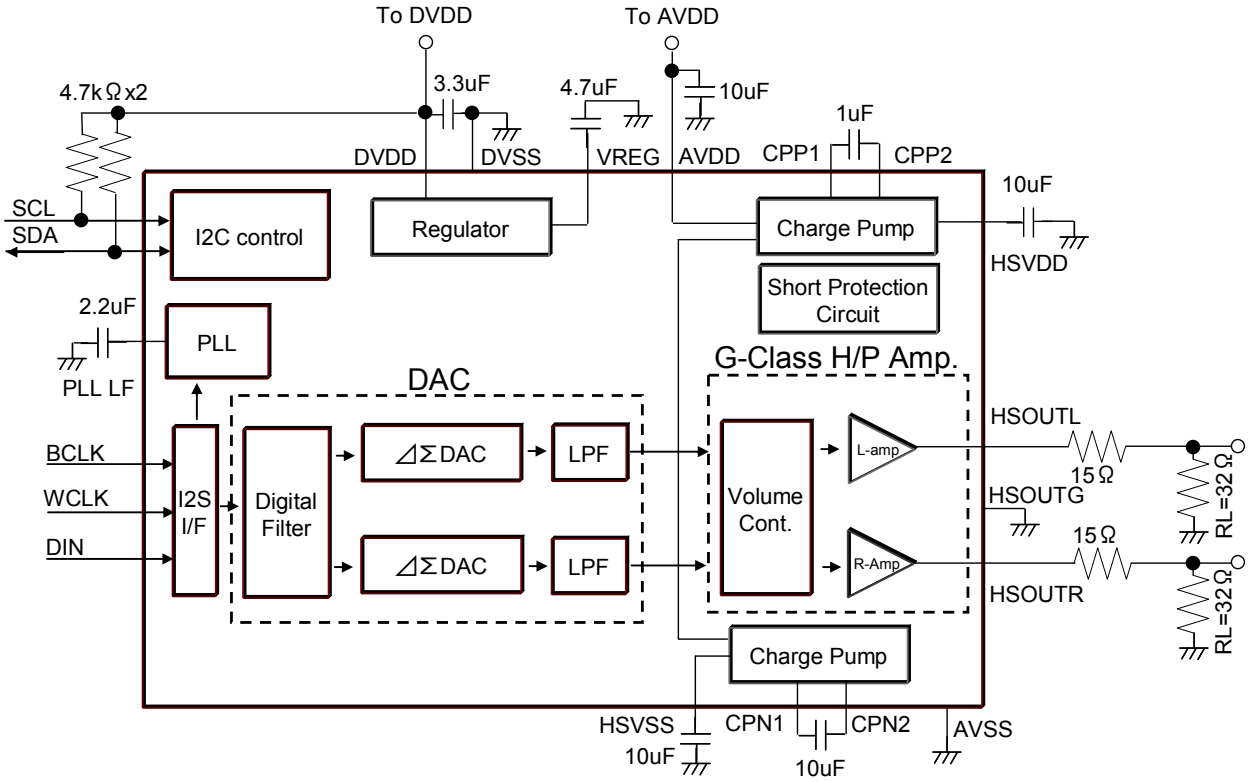
Characteristics	Symbol	Test circuit	Test Condition	Min	Typ.	Max	Unit
Maximum output amplitude AES17 at output terminals (rms)	Vo	1	RL=47Ω(15+32Ω) THD+N=1%, L+R in phase	0.935	1.03	1.135	V
Amplitude across headset Load (rms)	Vo1	3	RL=15Ω+16Ω, THD+N=1%	460	530	600	mV
	Vo2	2	RL=15Ω+32Ω, THD+N=1%	635	700	775	mV
Frequency response	⊿Gv	1	f=20 to 20kHz	-0.5	0	+0.5	dB
Total Harmonic Distortion + Noise	THD+N	2	Din=-1dBFS	—	0.02	0.032	%
Power Supply Rejection Ratio	PSRR	2	Gv=0dB	80	90	—	dB
Signal to Noise Ratio	S/N	2	AES17+CCIR Weighting	90	92	—	dB (CCIR)
Channel Separation	SEP	2	-	90	95	—	dB

Test Circuit

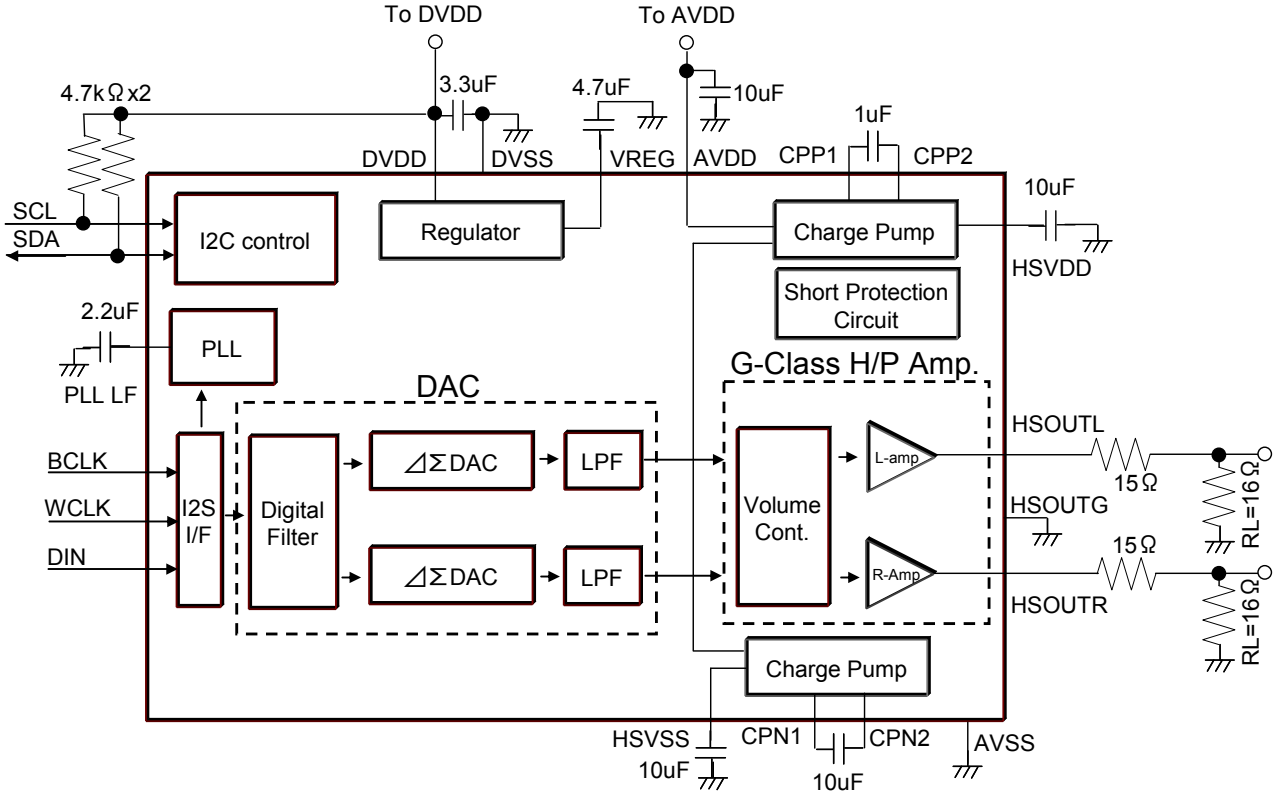
Test circuit 1 [RL=47Ω(15+32Ω)]



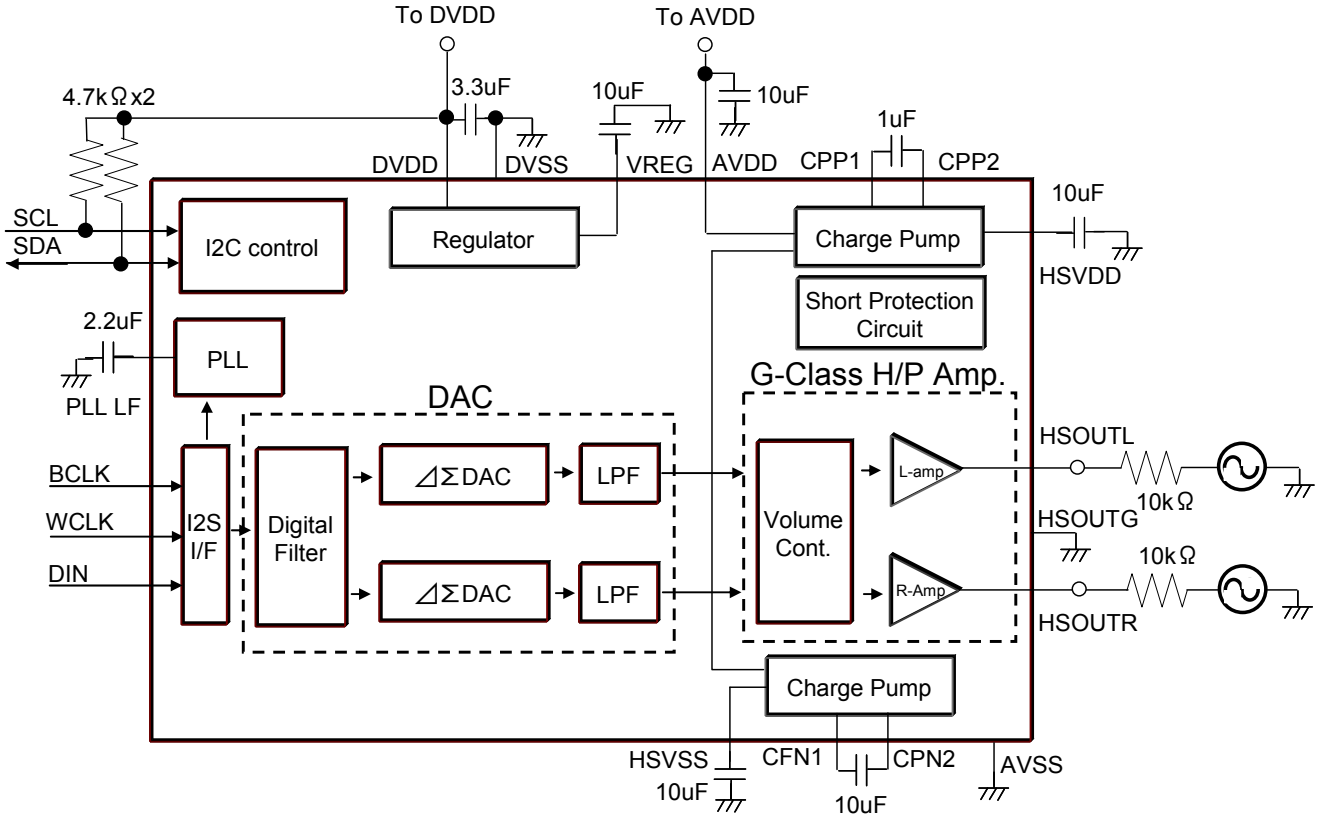
Test circuit 2 (RESD=15Ω+RL=32Ω)



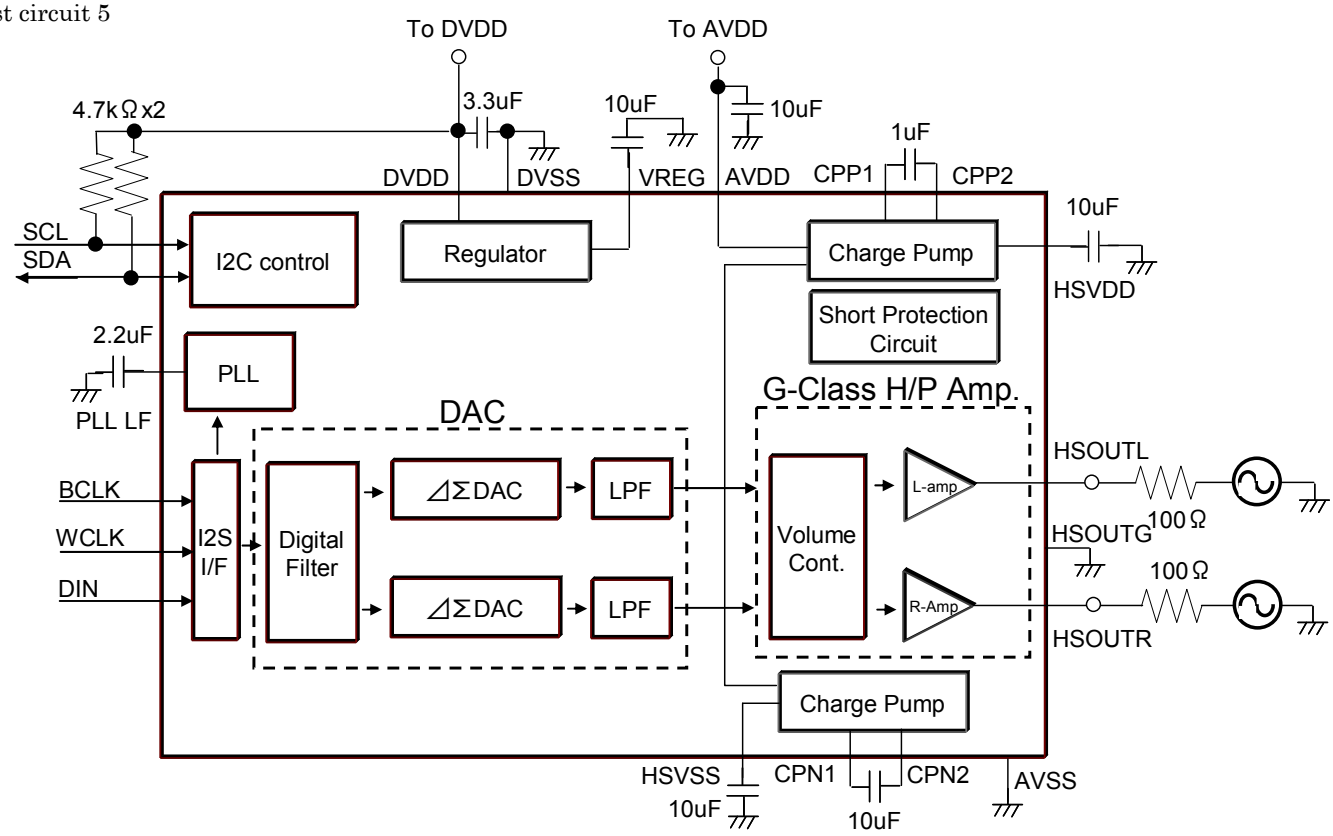
Test circuit 3 (RESD=15Ω+RL=16Ω)



Test circuit 4



Test circuit 5

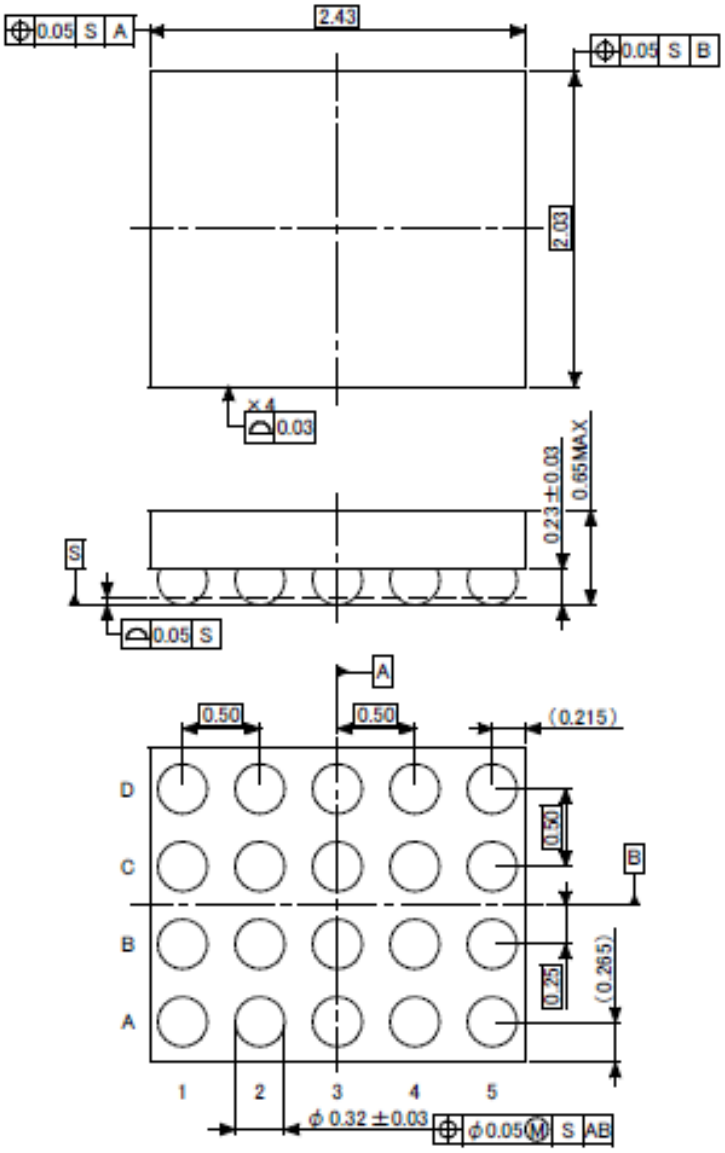


Components in the test circuits are only used to obtain and confirm the device characteristics.
These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

Package Dimensions

S-UFBGA20-0303-0.50A01

Unit : mm



- Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. For details on how to connect a protection circuit such as a current limiting resistor or back electromotive force adsorption diode, refer to individual IC datasheets or the IC databook. IC breakdown may cause injury, smoke or ignition.
- Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator. If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.
- Over current Protection Circuit

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