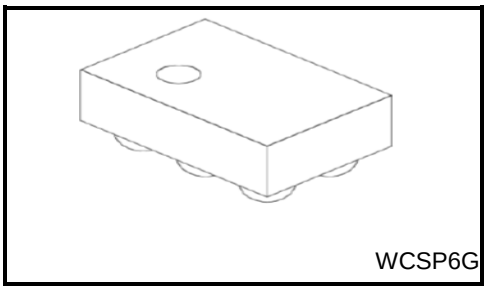
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TCK421G

Over Voltage Protection MOSFET Gate Driver IC

1. Description

TCK421G series is Over Voltage Protection Gate Driver IC for External N-channel MOSFET. This product support to MOSFET operating in wide voltage line from 2.7 V to 28 V with various Over Voltage Lock Out lineups. And this features low standby current, less than 1 μA, built in charge pump circuit and MOSFET gate-source protection circuit. Package is small and thin WCSP6G (1.2 mm x 0.8 mm (typ.), t: 0.35 mm(max)). Thus this is suitable for mobile, wearable system and power management circuit such as load switch application.



Weight : 0.61 mg (typ.)

2. Applications

Load switch circuit for mobile, wearable, and IoT equipment

3. Features

- Gate driver for N-channel Common Drain MOSFET
- Gate driver for N-channel Single High side MOSFET
- High maximum input voltage: $V_{IN\ max}$ = 40 V
- Wide input voltage operation: V_{IN} = 2.7 to 28 V
- Gate-Source protection circuit
- Over Voltage Lock Out : V_{IN_OVLO} = 23.26 V typ
- Under Voltage Lock Out : V_{IN_UVLO} = 2.0 V typ
- Built in Charge pump circuit: Gate source voltage V_{GS} = 10 V typ
- Low standby current : $I_{Q(OFF)}$ = 0.9 μA max at V_{IN} = 12 V

Start of commercial production
2021-11

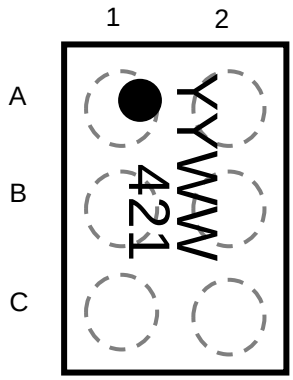
4. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Input voltage	V_{IN}	-0.3 to 40	V
Output voltage	V_{OUT}	-0.3 to 40	V
Control voltage	V_{CT}	-0.3 to 6	V
Ourput GATE voltage	$V_{GATE1,2}$	-0.3 to 40	V
Power dissipation	P_D	800 (Note 1)	mW
Operating temperature range	T_{opr}	-40 to 85	°C
Junction temperature	Tj	150	°C
Storage temperature	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Rating at mounting on a board: FR4 board. (40 mm × 40 mm × 1.6 mm, Cu 4 layer)

5. Top Marking, Pin Assignment (top view)



A1: VGATE1
B1: VGATE2
C1: VOUT
A2: VIN
B2: GND
C2: VCT

YYWW: Lot No.

421: TCK421G

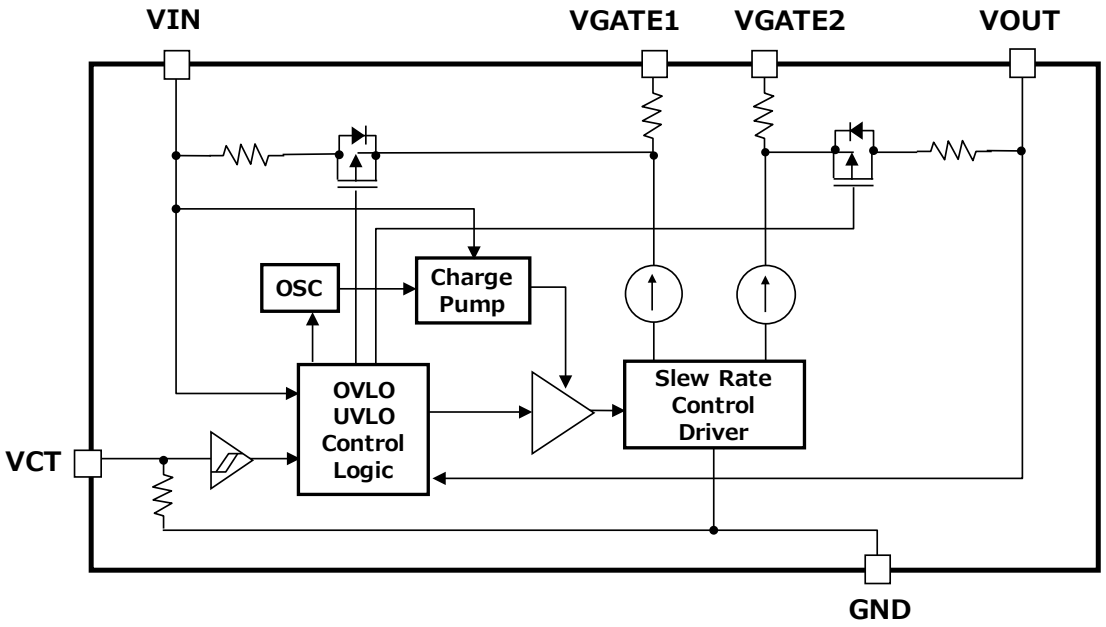
6. Operating Ranges

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Input operation voltage	V_{IN_opr}	2.7	—	28	V
CONTROL High-level input voltage	V_{IH}	1.2	—	5.5	V
CONTROL Low-level input voltage	V_{IL}	—	—	0.4	V

7. List of Products Number, OVLO and VGS

Product number	OVLO threshold, falling typ (V)	External MOSFET Gate-Source voltage (Control ON) typ (V)
TCK421G	23.26	10

8. Block Diagram



9. PIN Description

PIN	Name	Description
A1	VGATE1	Gate Driver Output for Gate 1 Or OPEN state (Non connection) for Single MOSFET use case
B1	VGATE2	Gate Driver Output for Gate 2
C1	VOUT	Monitoring Output voltage Connecting Output (Source 2) of Common Drain MOSFET Or Connecting Output (Source) of single MOSFET use case
A2	VIN	Input power supply voltage Connecting Output (Source 1) of Common Drain MOSFET Or Connecting Output (Drain) of single MOSFET use case
B2	GND	Ground
C2	VCT	Mode control input terminal VCT=High turn the external MOSFETs ON, VCT=Low, turn the external MOSFETs OFF

10. Operation Table

2.7V ≤ V_{IN} ≤ 28 V (Ta = -40 to 85°C)

VCT	VGATE1, VGATE2
High	Driver ON mode
Open	Driver OFF mode
Low	

11. Electrical Characteristics

11.1. DC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	Ta = 25℃			Ta = −40 to 85℃ (Note 2)		Unit
			Min.	Typ.	Max.	Min	Max	
VIN UVLO threshold, V_{OUT} falling	V_{IN_UVLO}		—	2.0	—	—	2.5	V
VIN UVLO hysteresis	V_{IN_UVhyst}		—	0.2	—	—	—	V
VIN OVLO threshold, V_{OUT} falling	V_{IN_OVLO}		—	23.26	—	22.34	24.05	V
VIN OVLO hysteresis	V_{IN_OVhyst}		—	0.12	—	—	—	V
Input quiescent current (ON state)	$I_{Q(ON)}$	V_{CT}: High, V_{IN} = 2.7 V	—	140	—	—	200	μA
		V_{CT}: High, V_{IN} = 4 V	—	130	—	—	420	μA
		V_{CT}: High, V_{IN} = 5 V	—	140	—	—	300	μA
		V_{CT}: High, V_{IN} = 9 V	—	170	—	—	460	μA
		V_{CT}: High, V_{IN} = 12 V	—	185	—	—	490	μA
		V_{CT}: High, V_{IN} = 20 V	—	220	—	—	560	μA
Standby current (OFF state)	$I_{Q(OFF)}$	V_{CT}: Low, V_{IN} = 2.7 V	—	0.14	—	—	0.3	μA
		V_{CT}: Low, V_{IN} = 4 V	—	0.25	—	—	0.4	μA
		V_{CT}: Low, V_{IN} = 5 V	—	0.28	—	—	0.5	μA
		V_{CT}: Low, V_{IN} = 9 V	—	0.42	—	—	0.7	μA
		V_{CT}: Low, V_{IN} = 12 V	—	0.52	—	—	0.9	μA
		V_{CT}: Low, V_{IN} = 20 V	—	0.80	—	—	1.3	μA
GATE Drive voltage (VGATE1-VIN) (VGATE2-VIN)	V_{GS} (Note 3)	V_{IN} = 2.7 V	—	9.2	—	8	10	V
		V_{IN} = 12 V	—	10	—	9	11	V
		V_{IN} = 20 V	—	10	—	9	11	V
Control pull down resistance	R_{CT}	V_{CT} = 5 V	—	550	—	—	—	kΩ

Note 2: This parameter is warranted by design
Note 3: V_{IN} is stable power supply condition

11.2. AC Characteristics (Ta = 25°C, V_{IN} = 5 V, $C_{GATE1,2}$ (Note 4) = 4000 pF)

Characteristics	Symbol	Test Condition (Figure 2,3)	Min.	Typ.	Max.	Unit
V_{GS} ON time	t_{ON}	Initial startup time V_{GATE2} – V_{OUT} = 1 V after V_{CT} = High, I_{OUT} = 0 mA	—	2.9	—	ms
V_{GS} OFF time	t_{OFF}	V_{GATE2} - V_{OUT} = 1 V, after V_{CT} = Low, I_{OUT} = 0 mA	—	52	—	μs

11.3. AC Characteristics (Ta = 25°C, V_{IN} = 20 V, $C_{GATE1,2}$ (Note 4) = 4000 pF)

Characteristics	Symbol	Test Condition (Figure 2,3)	Min.	Typ.	Max.	Unit
V_{GS} ON time	t_{ON}	Initial startup time V_{GATE2} – V_{OUT} = 1 V after V_{CT} = High, I_{OUT} = 0 mA	—	2.9	—	ms
V_{GS} OFF time	t_{OFF}	V_{GATE2} - V_{OUT} = 1 V, after V_{CT} = Low, I_{OUT} = 0 mA	—	36	—	μs

11.4. AC Characteristics (Ta = 25°C, $C_{GATE1,2}$ (Note 4) = 4000 pF)

Characteristics	Symbol	Test Condition (Figure 4,5)	Min.	Typ.	Max.	Unit
OVLO VGS turn OFF time	tOVP	V_{IN} > $V_{IN\_OVLO\ MAX}$, V_{IN} rising = 2 V/μs V_{GS} typ to V_{GS} (V_{GATE2}-V_{OUT}) = 1 V I_{OUT} = 0 mA	—	34	—	μs

Note 4: C_{GATE1} and C_{GATE2} are input capacitance connected to each VGATE1 and VGATE2 instead of external MOSFET

11.5. Timing Chart

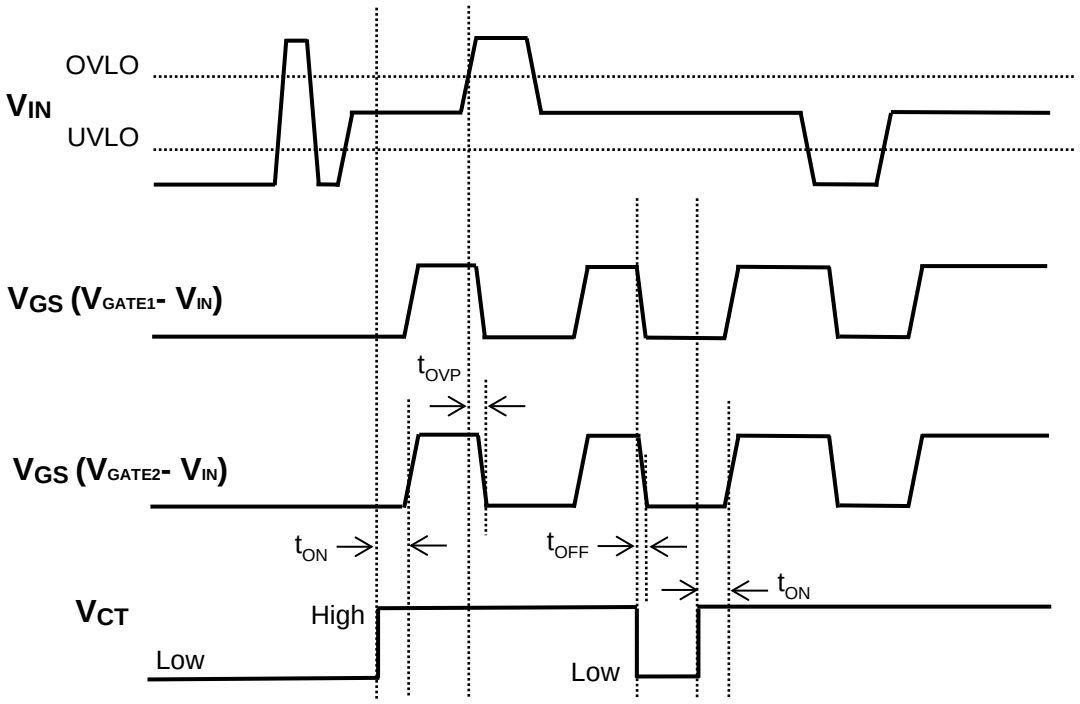


Fig.1 t_{ON}, t_{OFF}, t_{OVP}

Switching Waveform and Test circuit

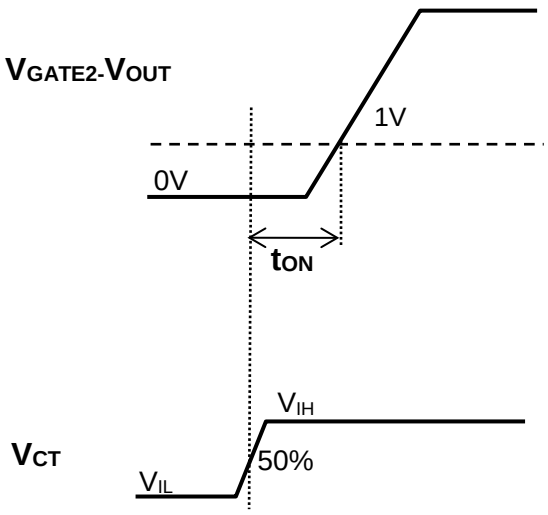


Fig.2 V_{GS} ON time Waveform

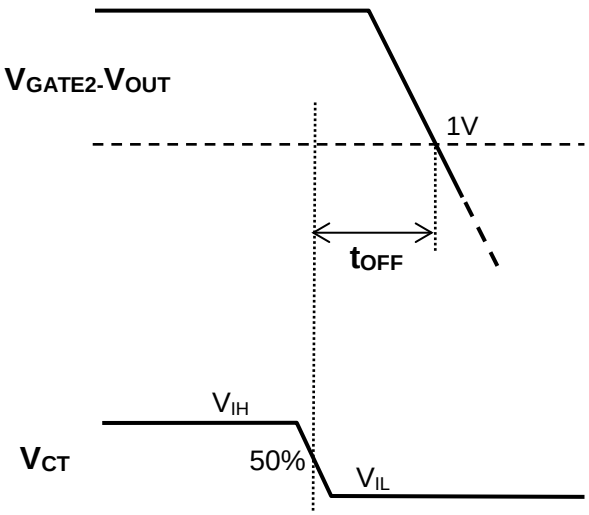


Fig.3 V_{GS} OFF time Waveform

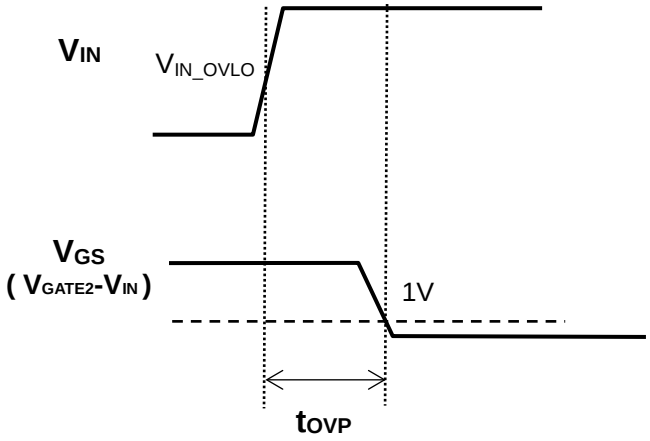


Fig.4 t_{OVP} Waveform

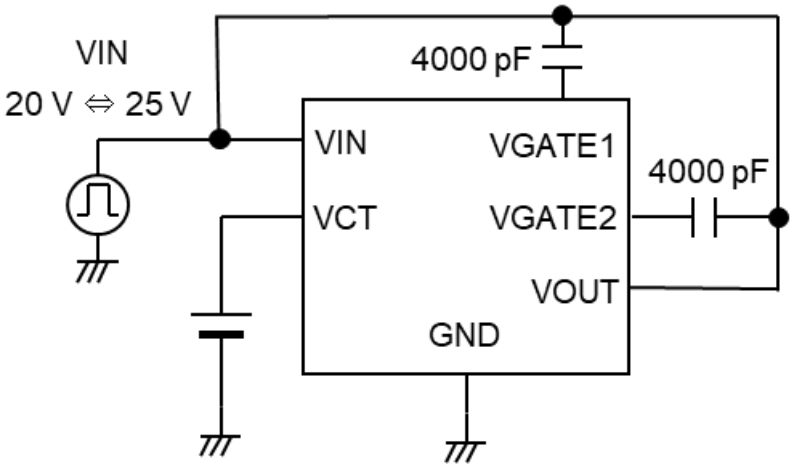
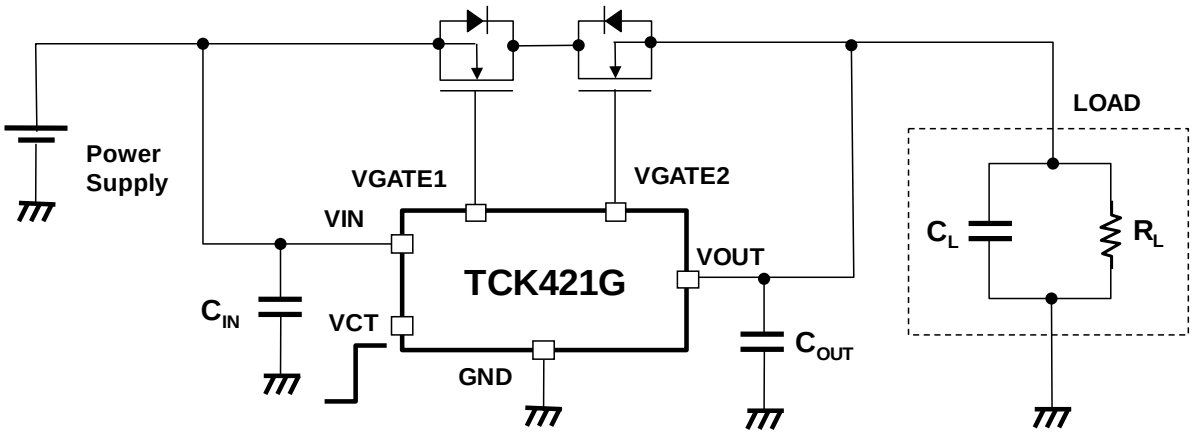


Fig.5 t_{OVP} test circuit

12. Application Note

12.1. Common Drain Connection N-channel MOSFET circuit example



1) Input and Output capacitor

An input capacitor (C_{IN}) and an output capacitor (C_{OUT}) are recommended for the stable operation. And it is effective to reduce voltage overshoot or undershoot due to sharp changes in output current and also for improved stability of the power supply. When used, place C_{IN} and C_{OUT} as close to V_{IN} pin to improve stability of the power supply.

2) VCT pin

VCT pin is pull down connection to GND. VCT High level voltage must be under 5.5V V_{IH} max.

3) VGATE1,2 pin and VOUT pin

VGATE1 pin is connected to Gate of VIN side MOSFET. VGATE2 pin is connected to Gate of VOUT side MOSFET. VOUT pin is connected to Source of VOUT side MOSFET. When the gate driver IC turns off state, VGATE1 terminal voltage is close to VIN voltage dropped by parasitic diode forward voltage. This circuit works to protect over voltage for VIN side MOSFET Gate-Source terminal. VOUT terminal works to protect VOUT side MOSFET as same circuit.

4) Turn on recovery time after Over Voltage Lock Out (OVLO)

Once VIN is in normal voltage range after OVLO, the turn on recovery time is similar V_{GS} ON time (t_{ON}).

5) Under Voltage Lock Out (UVLO) and Over Voltage Lock Out (OVLO)

UVLO and OVLO are designed in these products, but these are not designed to constantly ensure the suppression of the gate driver IC and external MOSFETs within operation limits. Depending on the condition during actual usage, it could affect the electrical characteristic specification and reliability. To select external MOSFETs, please consider enough electrical design margin. When using these products, please read through and understand the concept of dissipation for absolute maximum ratings from the above mention or our 'Semiconductor Reliability Handbook'. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommends inserting failsafe system into the design.

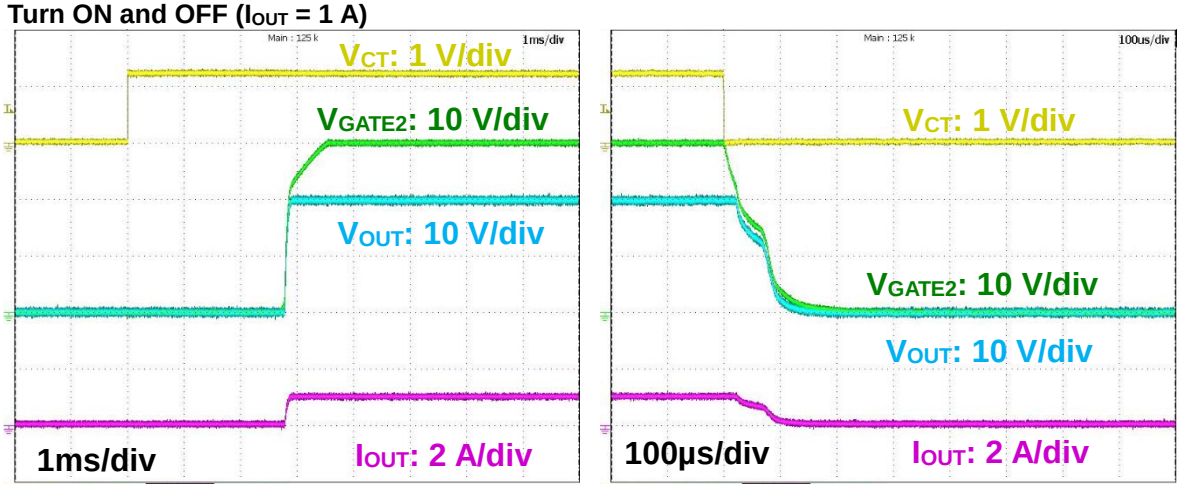
Common Drain Connection N-channel MOSFET Switching Waveform

Typical switching waveforms with TOSHIBA MOSFETs

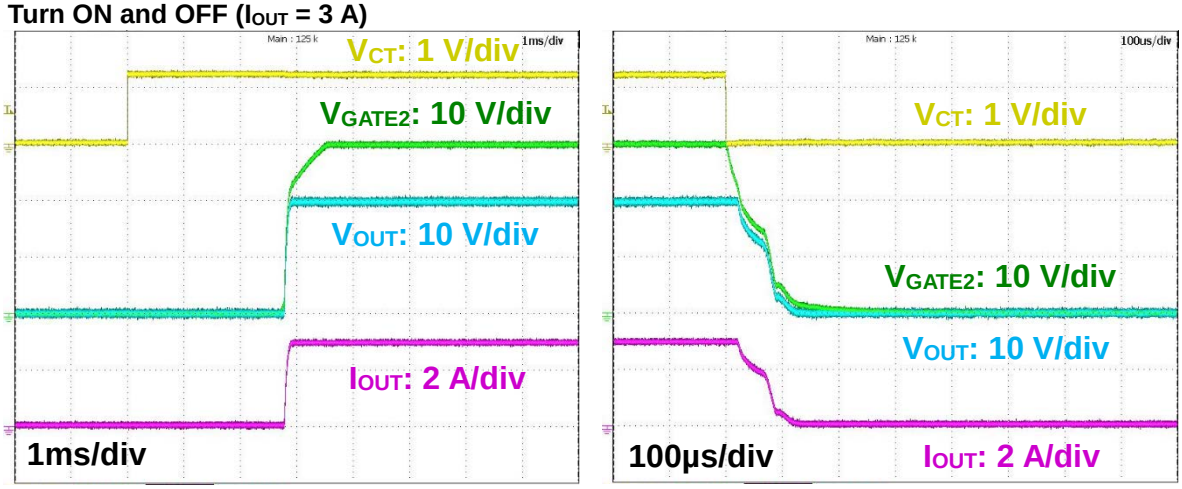
OVP Gate Driver IC	MOSFET		Test conditions	
	Part Number	Description	Turn ON and OFF	Over Voltage Lock Out
TCK421G	TPN1R603PL	Single N-channel MOSFET V_{DSS}: 30 V, V_{GSS}: ± 20 V $R_{DS(ON)}$: 1.2 mΩ typ at V_{GS} = 10 V Package: TSON Advance	V_{IN} = 20 V I_{OUT} = 1 A, 3 A C_{IN} = 1 µF C_{OUT} = 1 µF V_{CT} = 0 V ⇔ 1.2 V Ta = 25 °C	V_{IN} = 20 V ⇔ 25 V I_{OUT} = 1 A C_{IN} = 1 µF C_{OUT} = 1 µF V_{CT} = 1.2 V Ta = 25 °C
	TPHR6503PL1	Single N-channel MOSFET V_{DSS}: 30 V, V_{GSS}: ± 20 V $R_{DS(ON)}$: 0.41 mΩ typ at V_{GS} = 10 V Package: SOP Advance(N)		

TCK421G + TPN1R603PL x 2pcs

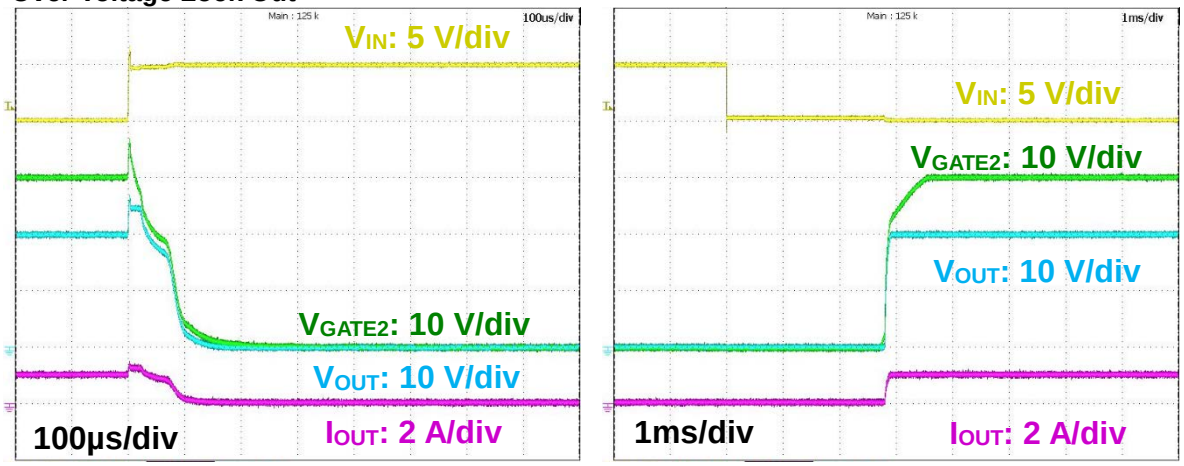
1. **Turn ON and OFF (I_{OUT} = 1 A)**



2. **Turn ON and OFF (I_{OUT} = 3 A)**

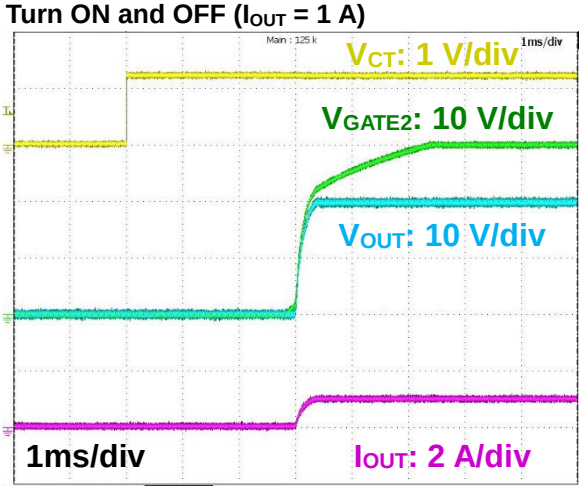


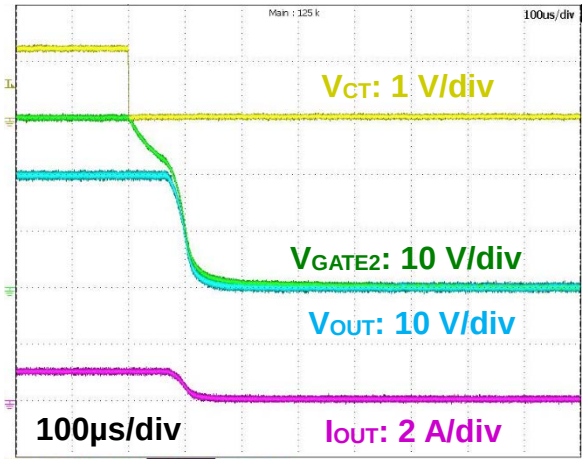
3. **Over Voltage Lock Out**



TCK421G + TPHR6503PL1 x 2pcs

1. **Turn ON and OFF (I_{OUT} = 1 A)**





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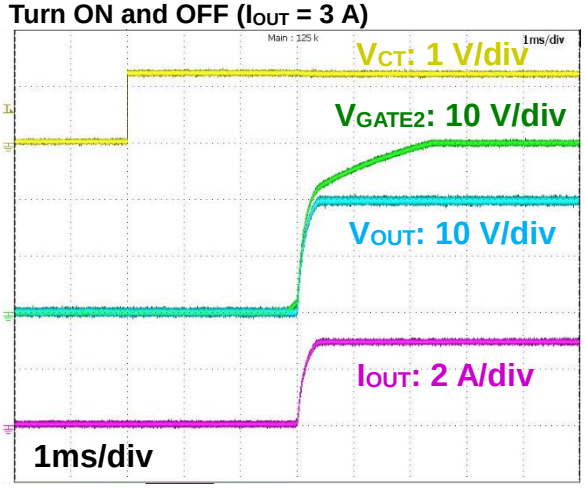

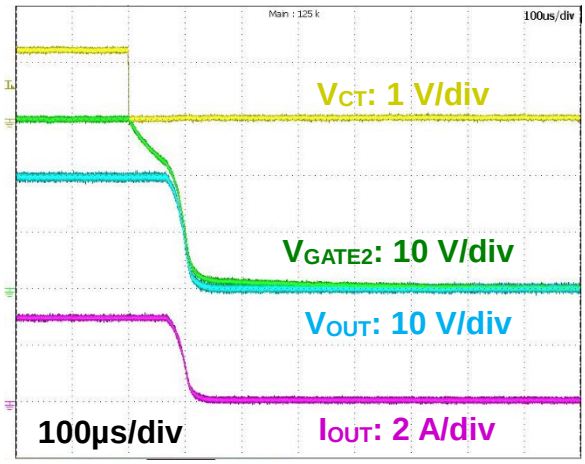

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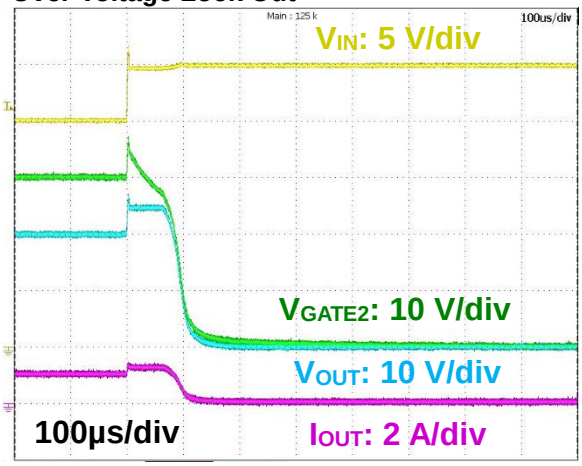
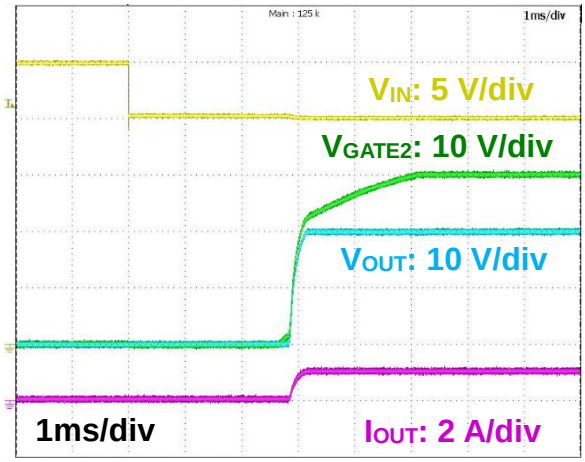
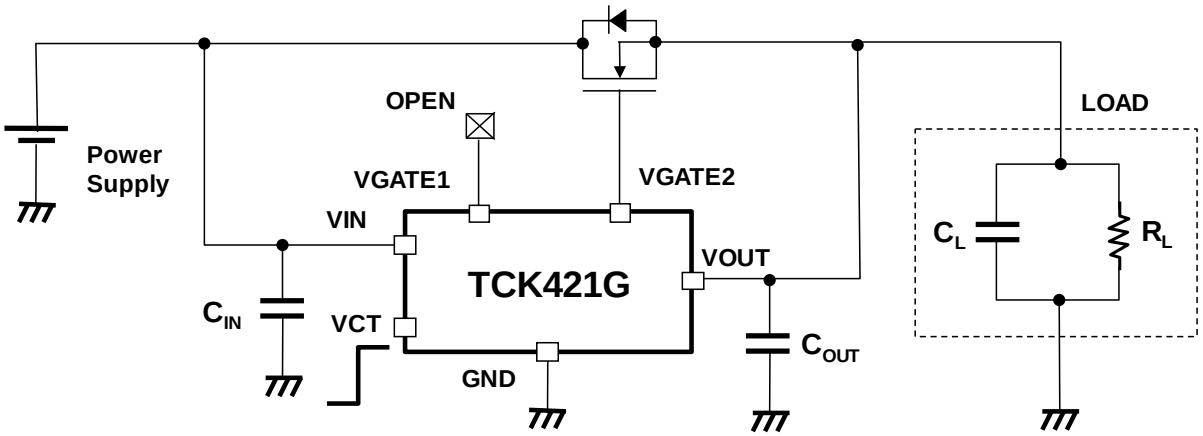




12.2. Single N-channel MOSFET circuit example



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4) Turn on recovery time after Over Voltage Lock Out

Once VIN is in normal voltage range after OVLO, the turn on recovery time is similar V_{GS} ON time (t_{ON}).

5) Under Voltage Lock Out (UVLO) and Over Voltage Lock Out (OVLO)

UVLO and OVLO are designed in these products, but these are not designed to constantly ensure the suppression of the gate driver IC and external MOSFETs within operation limits. Depending on the condition during actual usage, it could affect the electrical characteristic specification and reliability. To select external MOSFETs, please consider enough electrical design margin. When using these products, please read through and understand the concept of dissipation for absolute maximum ratings from the above mention or our 'Semiconductor Reliability Handbook'. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommends inserting failsafe system into the design.

Single N-channel MOSFET Switching Waveform

Typical switching waveforms with TOSHIBA MOSFETs

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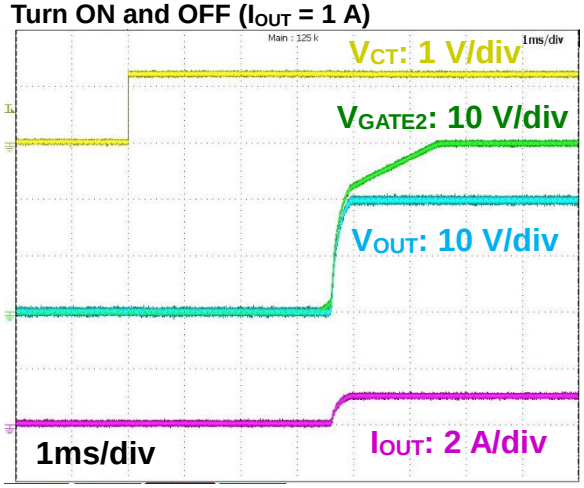
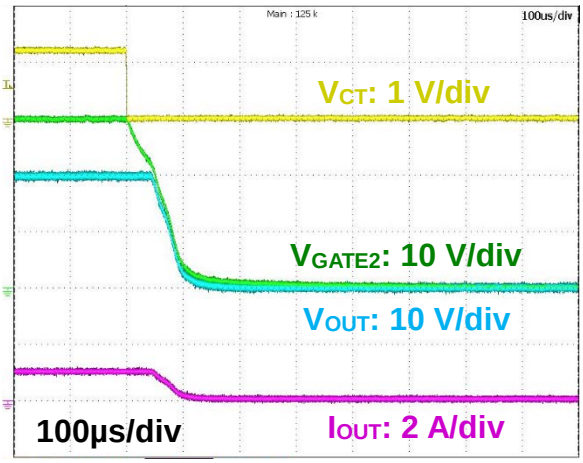
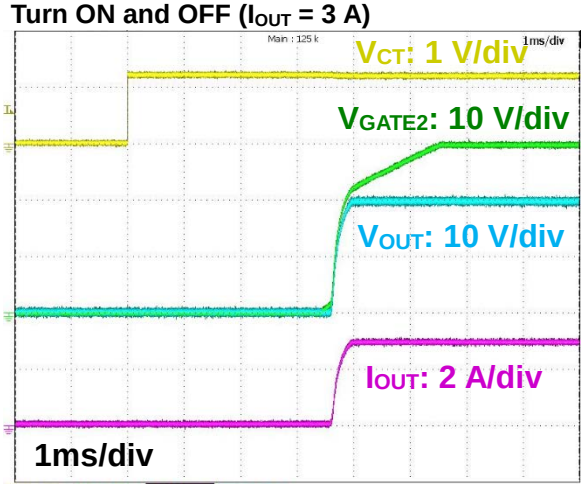
TCK421G + TPHR6503PL1

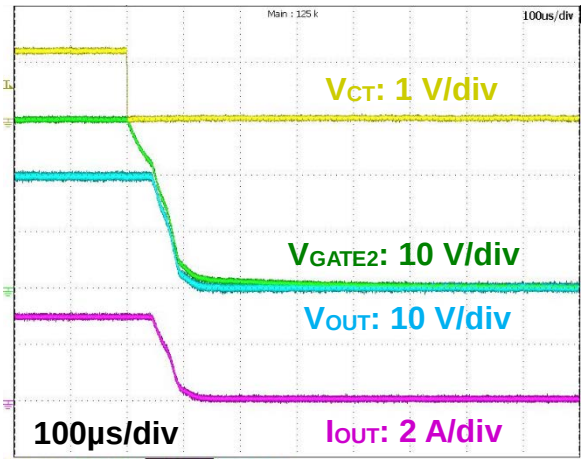
1. **Turn ON and OFF (I_{OUT} = 1 A)**



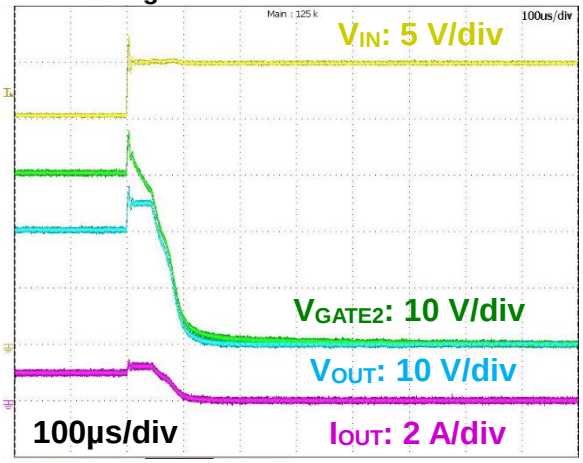


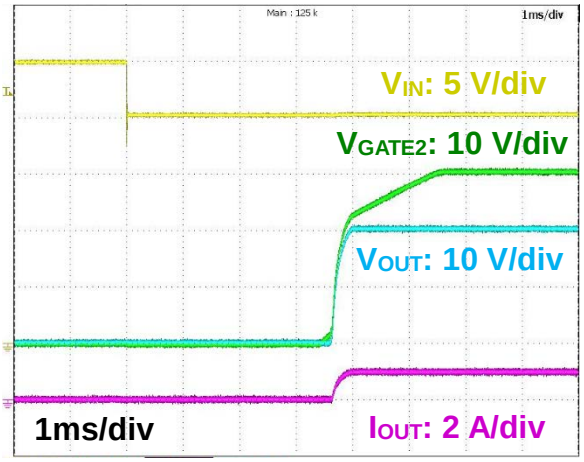
2. **Turn ON and OFF (I_{OUT} = 3 A)**





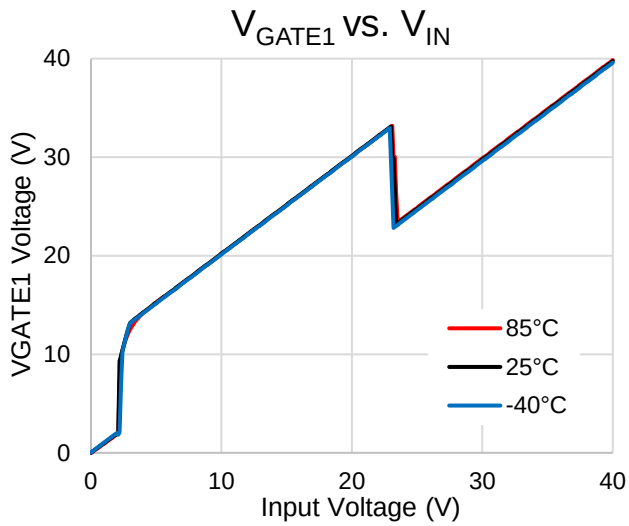
3. **Over Voltage Lock Out**

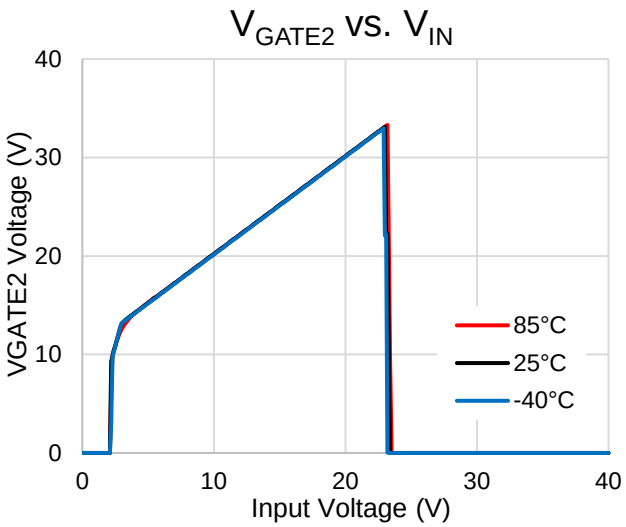




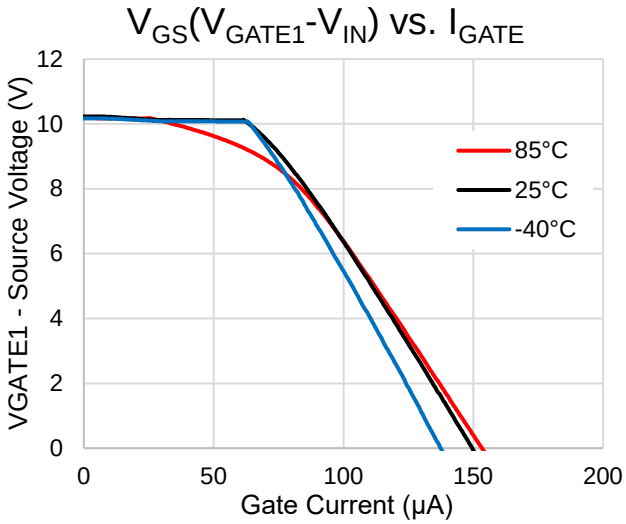
13. Representative Typical Characteristics

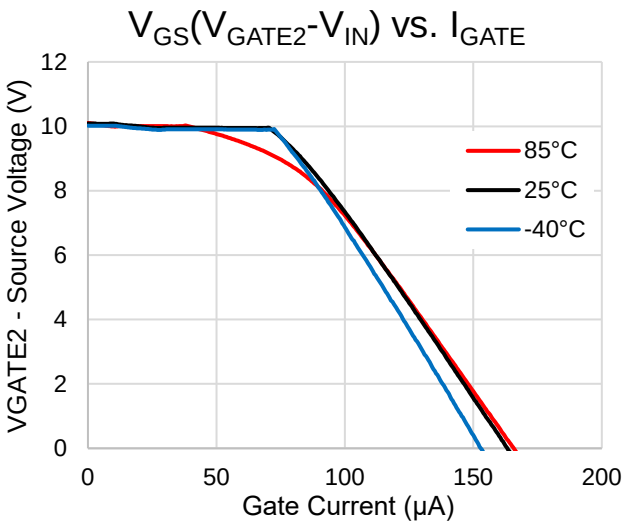
13.1. Gate voltage vs. Input voltage



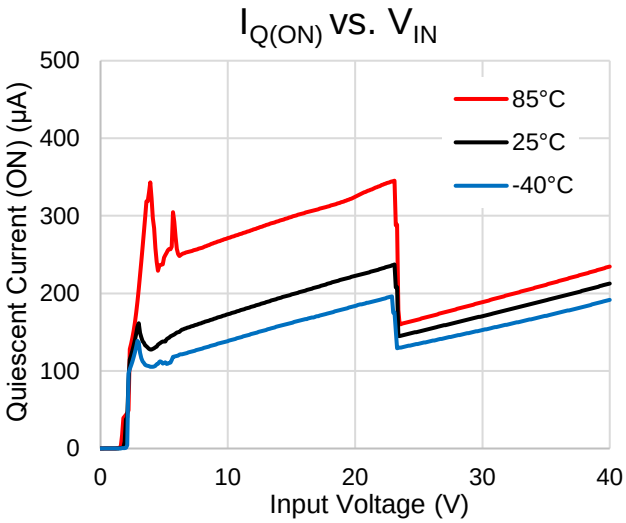


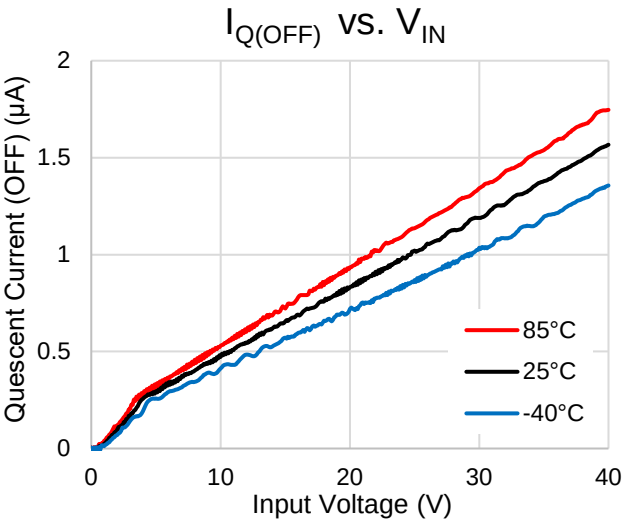
13.2. Gate voltage vs. Gate current





13.3. Quiescent current vs. Input voltage

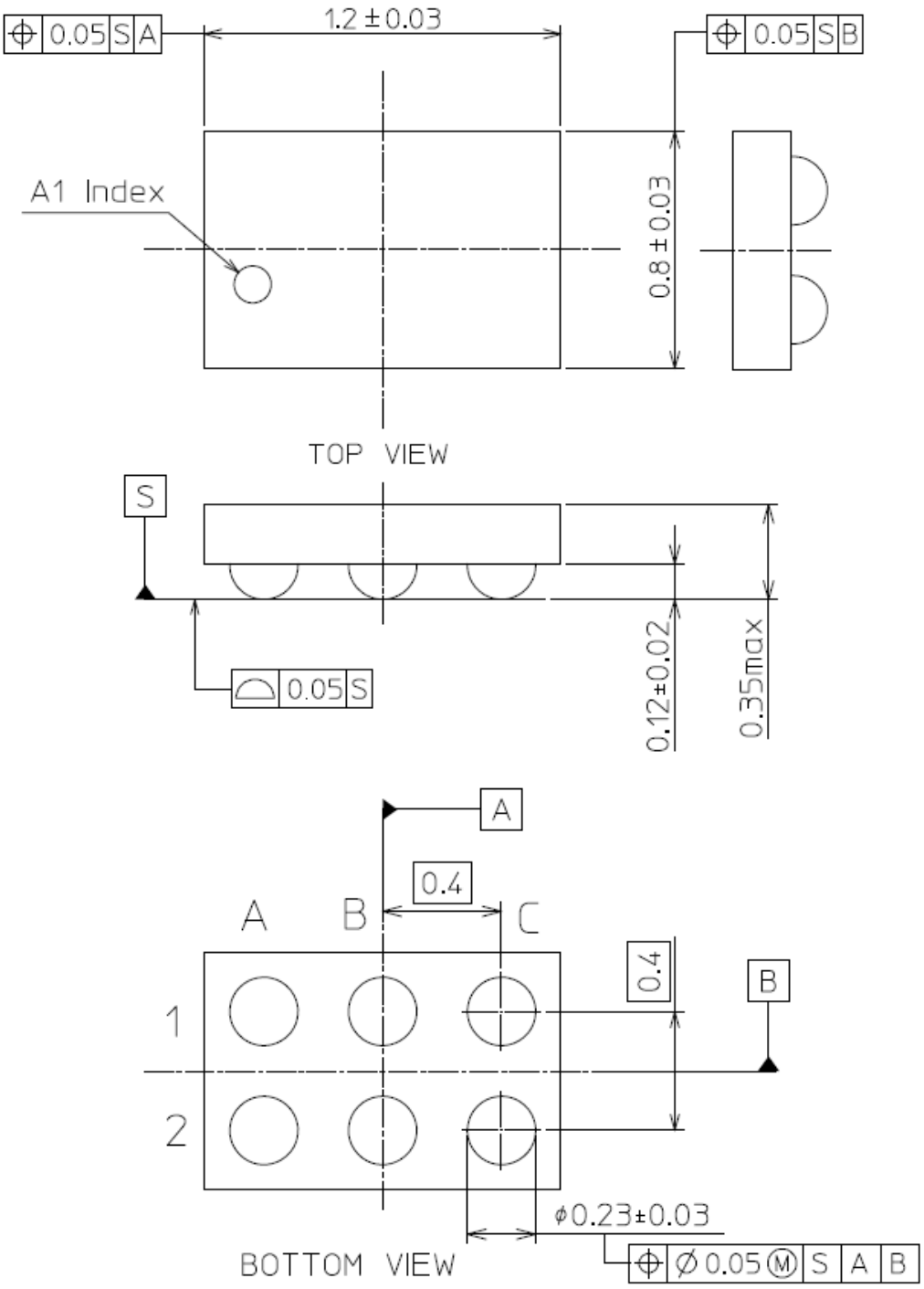




14. Package Information

WCSP6G

Unit: mm

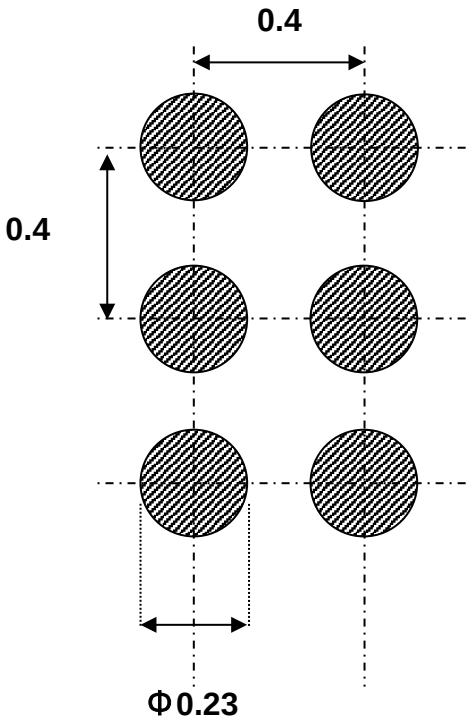


Weight: 0.61 mg (Typ.)

15. Land pattern dimensions for reference only

WCSP6G

Unit: mm



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