

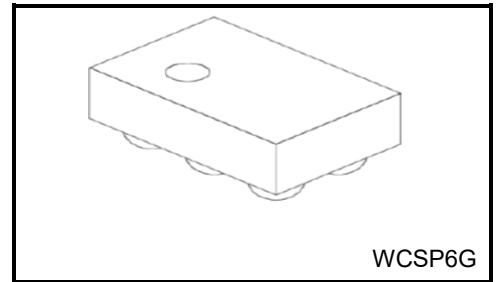
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

# TCK42xG Series

Over Voltage Protection MOSFET Gate Driver IC

## 1. Description

TCK42xG series is Over Voltage Protection Gate Driver IC for External N-channel MOSFET. This product support to MOSFET operating in wide voltage line from 2.7 V to 28 V with various Over Voltage Lock Out lineups. And this features low standby current, less than 1  $\mu$ A, built in charge pump circuit and MOSFET gate-source protection circuit. Package is very small and thin WCSP6G (1.2 mm x 0.8 mm (typ.), t: 0.35 mm (max)). Thus this is suitable for mobile, wearable system and power management circuit such as load switch application.



Weight : 0.61 mg ( typ.)

## 2. Applications

Load switch circuit for mobile, wearable, and IoT equipment

## 3. Features

- Gate driver for N-channel Common Drain MOSFET
- Gate driver for N-channel Single High side MOSFET
- High maximum input voltage:  $V_{IN\ max} = 40\ V$
- Wide input voltage operation:  $V_{IN} = 2.7\ to\ 28\ V$
- Gate-Source protection circuit
- Over Voltage Lock Out :  $V_{IN\_OVLO} = 6.31\ V, 10.83\ V, 14.29\ V, 23.26\ V\ and\ 27.73\ V\ typ$
- Under Voltage Lock Out :  $V_{IN\_UVLO} = 2.0\ V\ typ$
- Built in Charge pump circuit: Gate source voltage  $V_{GS} = 5.6\ V\ and\ 10\ V\ typ$
- Low standby current :  $I_{Q(OFF)} = 0.9\ \mu A\ max\ at\ V_{IN} = 12\ V$  (Except TCK424G, TCK425G)

Start of commercial production  
2021-11

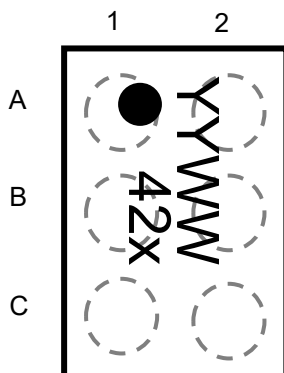
### 4. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Input voltage	V <sub>IN</sub>	-0.3 to 40	V
Output voltage	V <sub>OUT</sub>	-0.3 to 40	V
Control voltage	V <sub>CT</sub>	-0.3 to 6	V
Output GATE voltage	V <sub>GATE1,2</sub>	-0.3 to 40	V
Power dissipation	P <sub>D</sub>	800 (Note 1)	mW
Operating temperature range	T <sub>opr</sub>	-40 to 85	°C
Junction temperature	T <sub>j</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Rating at mounting on a board: FR4 board. ( 40 mm × 40 mm × 1.6 mm, Cu 4 layer )

### 5. Top Marking, Pin Assignment (top view)



A1: VGATE1  
 B1: VGATE2  
 C1: VOUT  
 A2: VIN  
 B2: GND  
 C2: VCT

YYWW: Lot No.

42x: Device name code  
 420: TCK420G  
 421: TCK421G  
 422: TCK422G  
 423: TCK423G  
 424: TCK424G  
 425: TCK425G

### 6. Operating Ranges

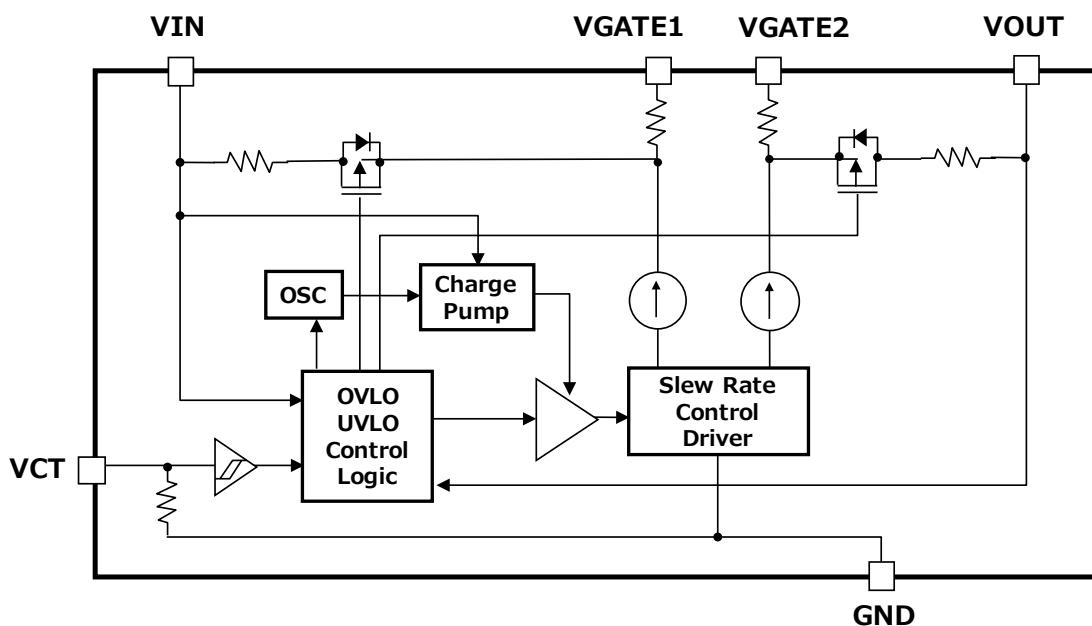
Characteristics	Symbol	Min.	Typ.	Max.	Unit
Input operation voltage	$V_{IN\_opr}$ (Note 2)	2.7	—	28	V
CONTROL High-level input voltage	$V_{IH}$	1.2	—	5.5	V
CONTROL Low-level input voltage	$V_{IL}$	—	—	0.4	V

Note 2:  $V_{IN\_opr} < V_{IN\_OVLO\ Max}$  of each product

### 7. List of Products Number, OVLO and VGS

Product number	OVLO threshold, falling typ (V)	External MOSFET Gate-Source voltage (Control ON) typ (V)
TCK420G	27.73	10
TCK421G	23.26	10
TCK422G	14.29	10
TCK423G	14.29	5.6
TCK424G	10.83	5.6
TCK425G	6.31	5.6

### 8. Block Diagram



### 9. PIN Description

PIN	Name	Description
A1	VGATE1	Gate Driver Output for Gate 1 Or OPEN state (Non connection) for Single MOSFET use case
B1	VGATE2	Gate Driver Output for Gate 2
C1	VOUT	Monitoring Output voltage Connecting Output (Source 2) of Common Drain MOSFET Or Connecting Output (Source) of single MOSFET use case
A2	VIN	Input power supply voltage Connecting Output (Source 1) of Common Drain MOSFET Or Connecting Output (Drain) of single MOSFET use case
B2	GND	Ground
C2	VCT	Mode control input terminal VCT=High turn the external MOSFETs ON, VCT=Low, turn the external MOSFETs OFF

### 10. Operation Table

$2.7V \leq V_{IN} \leq 28V$  ( $T_a = -40$  to  $85^\circ C$ )

VCT	VGATE1, VGATE2
High	Driver ON mode
Open	Driver OFF mode
Low	

### 11. Electrical Characteristics

#### 11.1. DC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C (Note 3)		Unit			
			Min.	Typ.	Max.	Min.	Max.				
VIN UVLO threshold, VOUT falling	VIN_UVLO	—	—	2.0	—	—	2.5	V			
VIN UVLO hysteresis	VIN_UVhyst	—	—	0.2	—	—	—	V			
VIN OVLO threshold, VOUT falling	TCK420G	VIN_OVLO	—	27.73	—	26.50	28.50	V			
	TCK421G		—	23.26	—	22.34	24.05	V			
	TCK422G TCK423G		—	14.29	—	13.61	14.91	V			
	TCK424G		—	10.83	—	10.35	11.47	V			
	TCK425G		—	6.31	—	5.76	6.87	V			
VIN OVLO hysteresis	TCK420G	VIN_OVhyst	—	0.17	—	—	—	V			
	TCK421G TCK422G TCK423G TCK424G TCK425G		—	0.12	—	—	—	V			
	Input quiescent current (ON state)		TCK420G TCK421G TCK422G	IQ(ON)	VCT: High, VIN = 2.7 V	—	140	—	—	200	μA
					VCT: High, VIN = 4 V	—	130	—	—	420	μA
					VCT: High, VIN = 5 V	—	140	—	—	300	μA
VCT: High, VIN = 9 V		—			170	—	—	460	μA		
VCT: High, VIN = 12 V		—			185	—	—	490	μA		
VCT: High, VIN = 20 V (Except TCK422G)		—	220		—	—	560	μA			
TCK423G TCK424G TCK425G		VCT: High, VIN = 2.7 V	—		75	—	—	130	μA		
		VCT: High, VIN = 4 V	—		95	—	—	150	μA		
		VCT: High, VIN = 5 V	—		100	—	—	160	μA		
		VCT: High, VIN = 9 V (Except TCK425G)	—		125	—	—	200	μA		
	VCT: High, VIN = 12 V (TCK423G only)	—	140	—	—	225	μA				
Standby current (OFF state)	IQ(OFF)	VCT: Low, VIN = 2.7 V	—	0.14	—	—	0.3	μA			
		VCT: Low, VIN = 4 V	—	0.25	—	—	0.4	μA			
		VCT: Low, VIN = 5 V	—	0.28	—	—	0.5	μA			
		VCT: Low, VIN = 9 V (Except TCK425G)	—	0.42	—	—	0.7	μA			
		VCT: Low, VIN = 12 V (Except TCK424G, TCK425G)	—	0.52	—	—	0.9	μA			
		VCT: Low, VIN = 20 V (TCK420G and TCK421G)	—	0.80	—	—	1.3	μA			

### 11.1. DC Characteristics (Ta = -40 to 85°C) (continued)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C (Note 3)		Unit	
			Min.	Typ.	Max.	Min.	Max.		
GATE Drive voltage (VGATE1-VIN) (VGATE2-VOUT)	TCK420G TCK421G TCK422G	VGS (Note 4)	VIN = 2.7 V	—	9.2	—	8	10	V
			VIN = 5 V	—	10	—	9	11	V
			VIN = 9 V	—	10	—	9	11	V
			VIN = 12 V	—	10	—	9	11	V
			VIN = 20 V (Except TCK422G)	—	10	—	9	11	V
			VIN = 24 V (TCK420G only)	—	10	—	9	11	V
	TCK423G TCK424G TCK425G		VIN = 2.7 V	—	5.6	—	4.9	6.3	V
			VIN = 5 V	—	5.6	—	5.0	6.3	V
			VIN = 9 V (Except TCK425G)	—	5.6	—	5.0	6.3	V
			VIN = 12 V (TCK423G only)	—	5.6	—	5.0	6.3	V
Control pull down resistance	RCT	VCT = 5 V	—	550	—	—	—	kΩ	

Note 3: This parameter is warranted by design

Note 4: VIN is stable power supply condition

### 11.2. AC Characteristics (Ta = 25°C, VIN = 5 V, CGATE1,2 (Note 5) = 4000 pF)

Characteristics		Symbol	Test Condition (Figure 2,3,4)	Min.	Typ.	Max.	Unit
VGS ON time		tON	Initial startup time VGATE2 - VOUT = 1 V after VCT = High, IOUT = 0 mA	—	2.9	—	ms
VGS OFF time	TCK420G TCK421G TCK422G	tOFF	VGATE2 - VOUT = 1 V, after VCT = Low, IOUT = 0 mA	—	52	—	μs
	TCK423G TCK424G TCK425G			—	23	—	μs

### 11.3. AC Characteristics (Ta = 25°C, VIN = 12 V, CGATE1,2 (Note 5) = 4000 pF)

Characteristics		Symbol	Test Condition (Figure 2,3,4)	Min.	Typ.	Max.	Unit
VGS ON time		tON	Initial startup time VGATE2 - VOUT = 1 V after VCT = High, IOUT = 0 mA	—	2.9	—	ms
VGS OFF time	TCK420G TCK421G TCK422G	tOFF	VGATE2 - VOUT = 1 V, after VCT = Low, IOUT = 0 mA	—	44	—	μs
	TCK423G			—	16.4	—	μs

### TCK420G, TCK421G

### 11.4. AC Characteristics (Ta = 25°C, VIN = 20 V, CGATE1,2 (Note 5) = 4000 pF)

Characteristics		Symbol	Test Condition (Figure 2,3,4)	Min.	Typ.	Max.	Unit
VGS ON time		tON	Initial startup time VGATE2 - VOUT = 1 V after VCT = High, IOUT = 0 mA	—	2.9	—	ms
VGS OFF time		tOFF	VGATE2 - VOUT = 1 V, after VCT = Low, IOUT = 0 mA	—	36	—	μs

### TCK420G

### 11.5. AC Characteristics (Ta = 25°C, VIN = 24 V, CGATE1,2 (Note 5) = 4000 pF)

Characteristics		Symbol	Test Condition (Figure 2,3,4)	Min.	Typ.	Max.	Unit
VGS ON time		tON	Initial startup time VGATE2 - VOUT = 1 V after VCT = High, IOUT = 0 mA	—	2.9	—	ms
VGS OFF time		tOFF	VGATE2 - VOUT = 1 V, after VCT = Low, IOUT = 0 mA	—	32	—	μs

### 11.6. AC Characteristics (Ta = 25°C, C<sub>GATE1,2</sub> (Note 5) = 4000 pF)

Characteristics		Symbol	Test Condition (Figure 5,6)	Min.	Typ.	Max.	Unit
OVLO V <sub>GS</sub> turn OFF time	TCK420G	t <sub>OVLP</sub>	V <sub>IN</sub> = 24 to 29 V, V <sub>IN</sub> rising = 2 V/μs V <sub>GS</sub> typ to V <sub>GS</sub> (V <sub>GATE2</sub> -V <sub>IN</sub> ) = 1 V I <sub>OUT</sub> = 0 mA	—	31	—	μs
	TCK421G		V <sub>IN</sub> = 20 to 25 V, V <sub>IN</sub> rising = 2 V/μs V <sub>GS</sub> typ to V <sub>GS</sub> (V <sub>GATE2</sub> -V <sub>IN</sub> ) = 1 V I <sub>OUT</sub> = 0 mA	—	34	—	μs
	TCK422G		V <sub>IN</sub> = 12 to 15 V, V <sub>IN</sub> rising = 2 V/μs V <sub>GS</sub> typ to V <sub>GS</sub> (V <sub>GATE2</sub> -V <sub>IN</sub> ) = 1 V I <sub>OUT</sub> = 0 mA	—	41	—	μs
	TCK423G		V <sub>IN</sub> = 12 to 15 V, V <sub>IN</sub> rising = 2 V/μs V <sub>GS</sub> typ to V <sub>GS</sub> (V <sub>GATE2</sub> -V <sub>IN</sub> ) = 1 V I <sub>OUT</sub> = 0 mA	—	16	—	μs
	TCK424G		V <sub>IN</sub> = 9 to 12 V, V <sub>IN</sub> rising = 2 V/μs V <sub>GS</sub> typ to V <sub>GS</sub> (V <sub>GATE2</sub> -V <sub>IN</sub> ) = 1 V I <sub>OUT</sub> = 0 mA	—	18	—	μs
	TCK425G		V <sub>IN</sub> = 5 to 8 V, V <sub>IN</sub> rising = 2 V/μs V <sub>GS</sub> typ to V <sub>GS</sub> (V <sub>GATE2</sub> -V <sub>IN</sub> ) = 1 V I <sub>OUT</sub> = 0 mA	—	19	—	μs

Note 5: C<sub>GATE1</sub> and C<sub>GATE2</sub> are input capacitance connected to each VGATE1 and VGATE2 instead of external MOSFET



### 11.7. Timing Chart

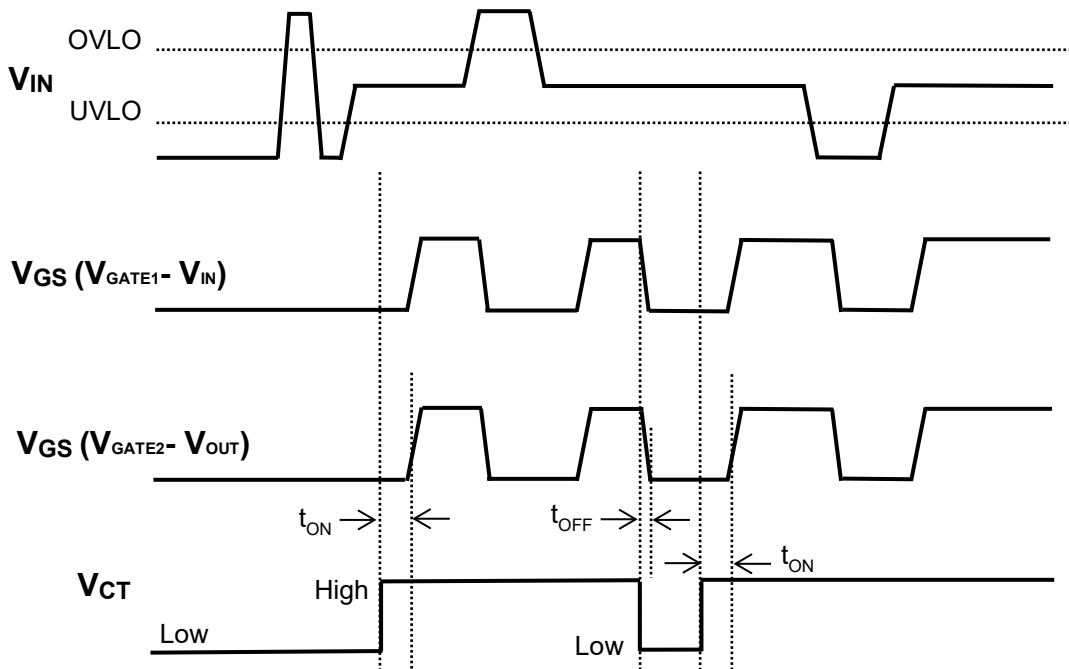


Fig.1 t<sub>ON</sub>, t<sub>OFF</sub>

### 11.8. Switching Waveform and Test circuit

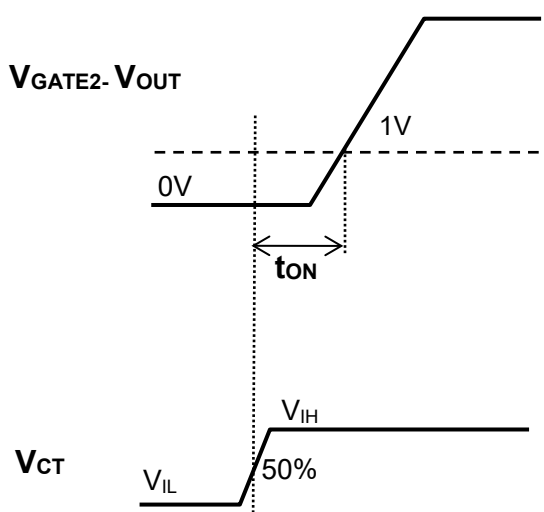


Fig.2 V<sub>GS</sub> ON time Waveform

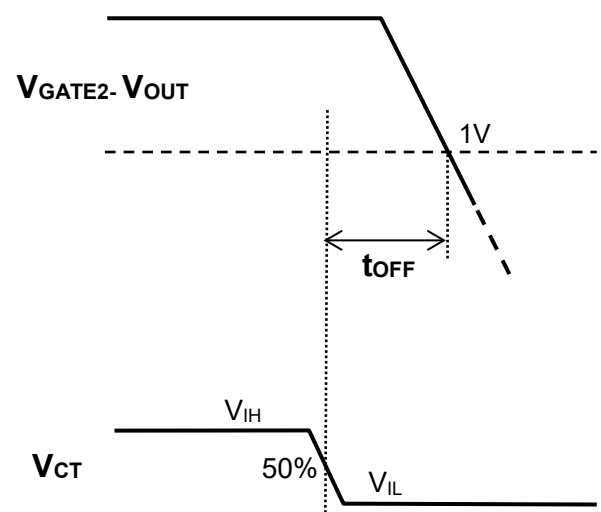
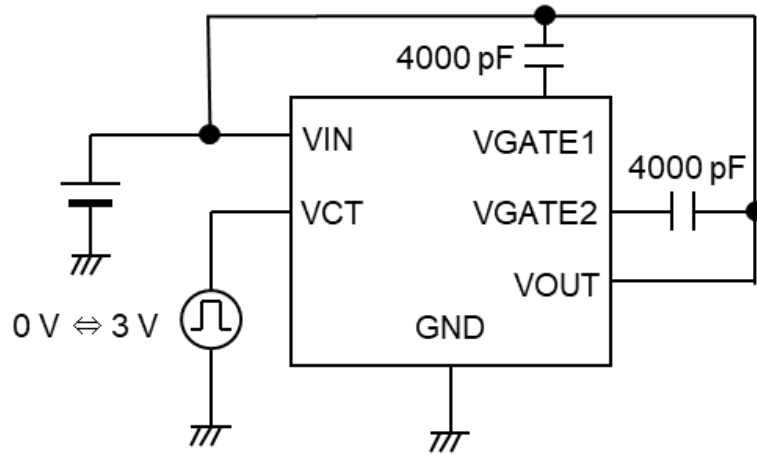
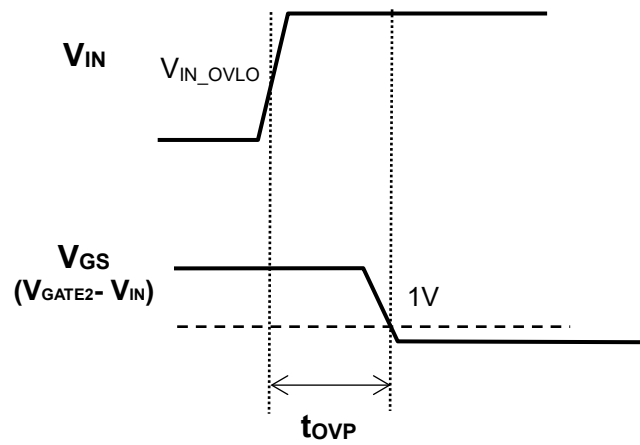


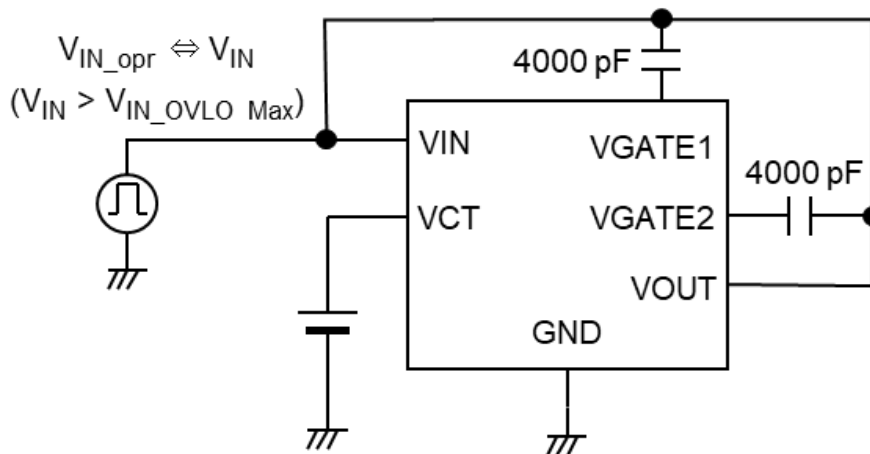
Fig.3 V<sub>GS</sub> OFF time Waveform



**Fig.4 V<sub>GS</sub> ON and OFF time test circuit**



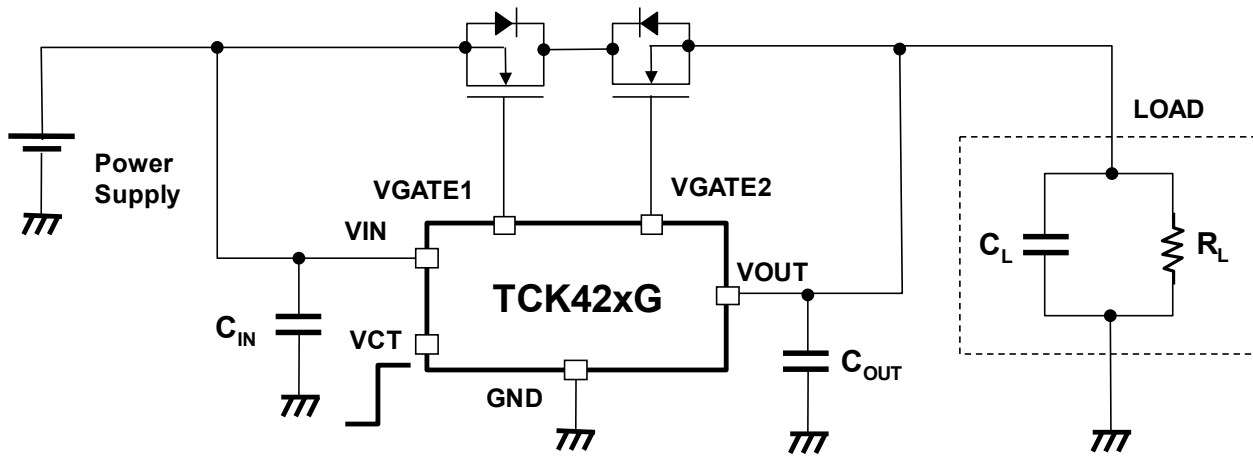
**Fig.5 toVP Waveform**



**Fig.6 toVP test circuit**

### 12. Application Note

#### 12.1. Common Drain Connection N-channel MOSFET circuit example



1. Input and Output capacitor  
An input capacitor ( $C_{IN}$ ) and an output capacitor ( $C_{OUT}$ ) are recommended for the stable operation. And it is effective to reduce voltage overshoot or undershoot due to sharp changes in output current and also for improved stability of the power supply. When used, place  $C_{IN}$  and  $C_{OUT}$  as close to  $V_{IN}$  pin and  $V_{OUT}$  pin to improve stability of the power supply.
2. VCT pin  
VCT pin is pull down connection to GND. VCT High level voltage must be under 5.5V  $V_{IH}$  max.
3. VGATE1,2 pin and VOUT pin  
VGATE1 pin is connected to Gate of  $V_{IN}$  side MOSFET. VGATE2 pin is connected to Gate of  $V_{OUT}$  side MOSFET. VOUT pin is connected to Source of  $V_{OUT}$  side MOSFET. When the gate driver IC turns off state, VGATE1 terminal voltage is close to  $V_{IN}$  voltage dropped by parasitic diode forward voltage. This circuit works to protect over voltage for  $V_{IN}$  side MOSFET Gate-Source terminal. VOUT terminal works to protect  $V_{OUT}$  side MOSFET as same circuit.
4. Turn on recovery time after Over Voltage Lock Out (OVLO)  
Once  $V_{IN}$  is in normal voltage range after OVLO, the turn on recovery time is similar  $V_{GS}$  ON time ( $t_{ON}$ ).
5. Under Voltage Lock Out (UVLO) and Over Voltage Lock Out (OVLO)  
UVLO and OVLO are designed in these products, but these are not designed to constantly ensure the suppression of the gate driver IC and external MOSFETs within operation limits. Depending on the condition during actual usage, it could affect the electrical characteristic specification and reliability. To select external MOSFETs, please consider enough electrical design margin. When using these products, please read through and understand the concept of dissipation for absolute maximum ratings from the above mention or our 'Semiconductor Reliability Handbook'. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommends inserting failsafe system into the design.

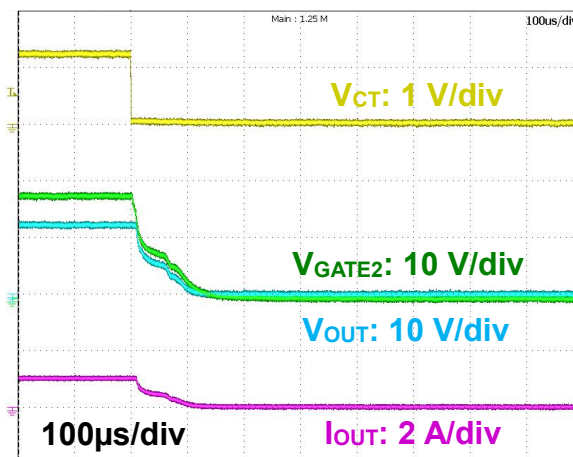
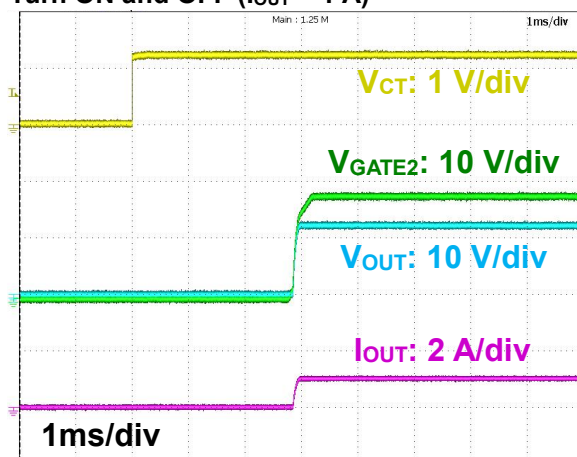
### Common Drain Connection N-channel MOSFET Switching Waveform

#### Typical switching waveforms with TOSHIBA MOSFETs

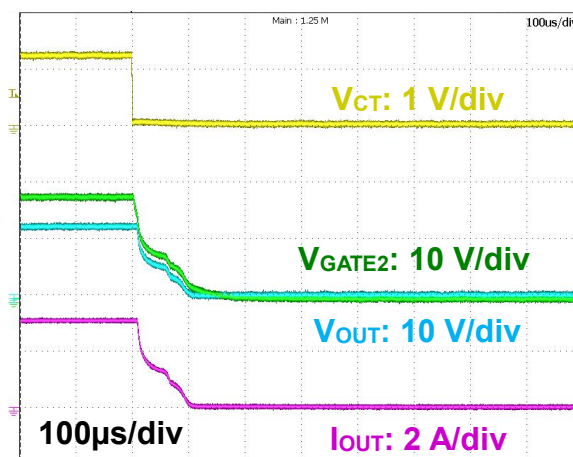
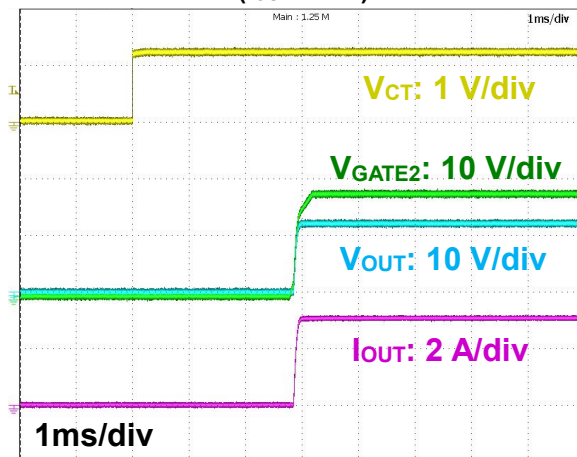
OVP Gate Driver IC	MOSFET		Test conditions	
	Part Number	Description	Turn ON and OFF	Over Voltage Lock Out
TCK423G ( $V_{GS} = 5.6\text{ V}$ )	TPN1R603PL	Single N-channel MOSFET $V_{DSS}: 30\text{ V}$ , $V_{GSS}: \pm 20\text{ V}$ $R_{DS(ON)}: 1.2\text{ m}\Omega$ typ at $V_{GS} = 10\text{ V}$ Package: TSON Advance	$V_{IN} = 12\text{ V}$ (TCK423G) $V_{IN} = 20\text{ V}$ (TCK421G) $I_{OUT} = 1\text{ A}, 3\text{ A}$ $C_{IN} = 1\text{ }\mu\text{F}$ $C_{OUT} = 1\text{ }\mu\text{F}$ $V_{CT} = 0\text{ V} \Leftrightarrow 1.2\text{ V}$ $T_a = 25\text{ }^\circ\text{C}$	$V_{IN} = 12\text{ V} \Leftrightarrow 15\text{ V}$ (TCK423G) $V_{IN} = 20\text{ V} \Leftrightarrow 25\text{ V}$ (TCK421G) $I_{OUT} = 1\text{ A}$ $C_{IN} = 1\text{ }\mu\text{F}$ $C_{OUT} = 1\text{ }\mu\text{F}$ $V_{CT} = 1.2\text{ V}$ $T_a = 25\text{ }^\circ\text{C}$
TCK421G ( $V_{GS} = 10\text{ V}$ )	TPHR6503PL1	Single N-channel MOSFET $V_{DSS}: 30\text{ V}$ , $V_{GSS}: \pm 20\text{ V}$ $R_{DS(ON)}: 0.41\text{ m}\Omega$ typ at $V_{GS} = 10\text{ V}$ Package: SOP Advance(N)		

#### TCK423G + TPN1R603PL x 2pcs

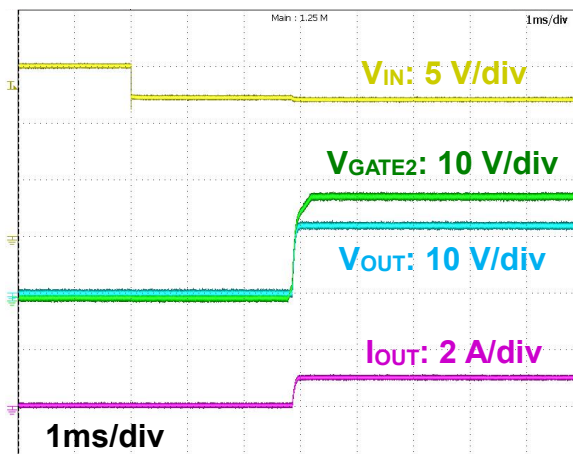
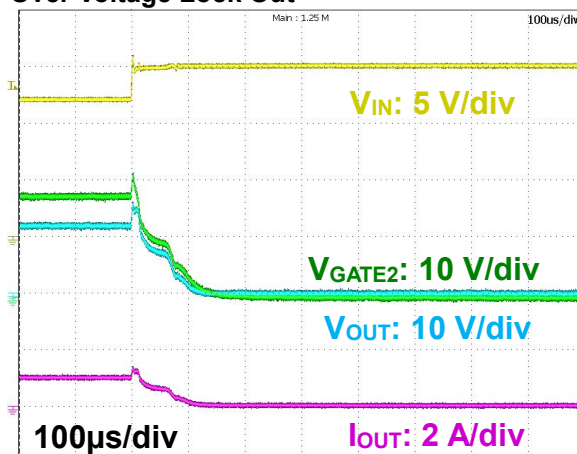
##### 1. Turn ON and OFF ( $I_{OUT} = 1\text{ A}$ )



##### 2. Turn ON and OFF ( $I_{OUT} = 3\text{ A}$ )

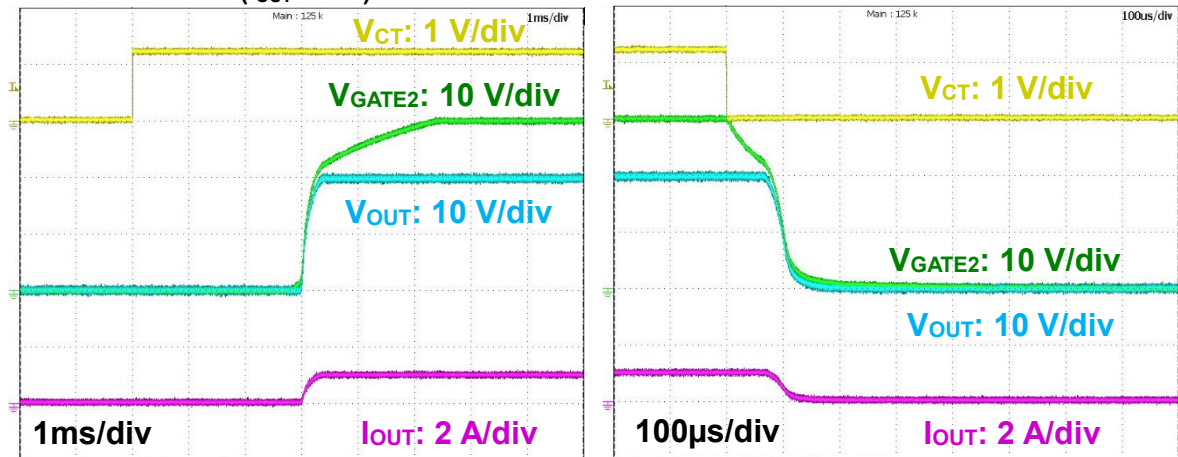


##### 3. Over Voltage Lock Out

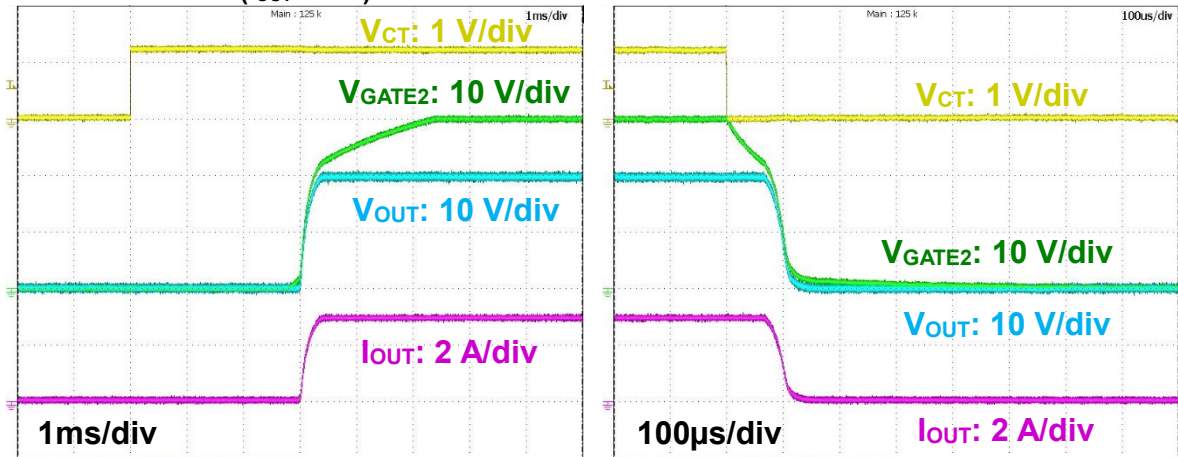


TCK421G + TPHR6503PL1 x 2pcs

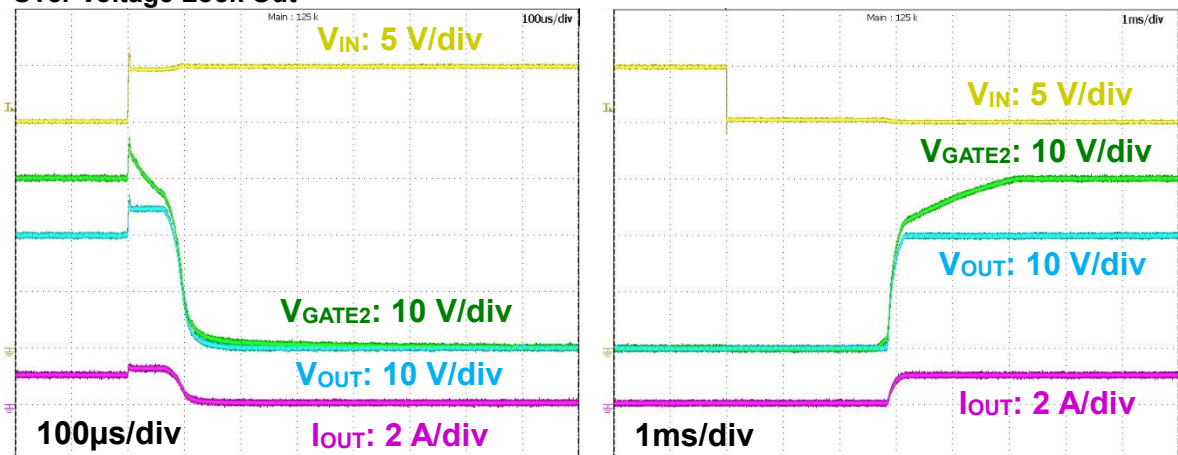
1. Turn ON and OFF ( $I_{OUT} = 1\text{ A}$ )



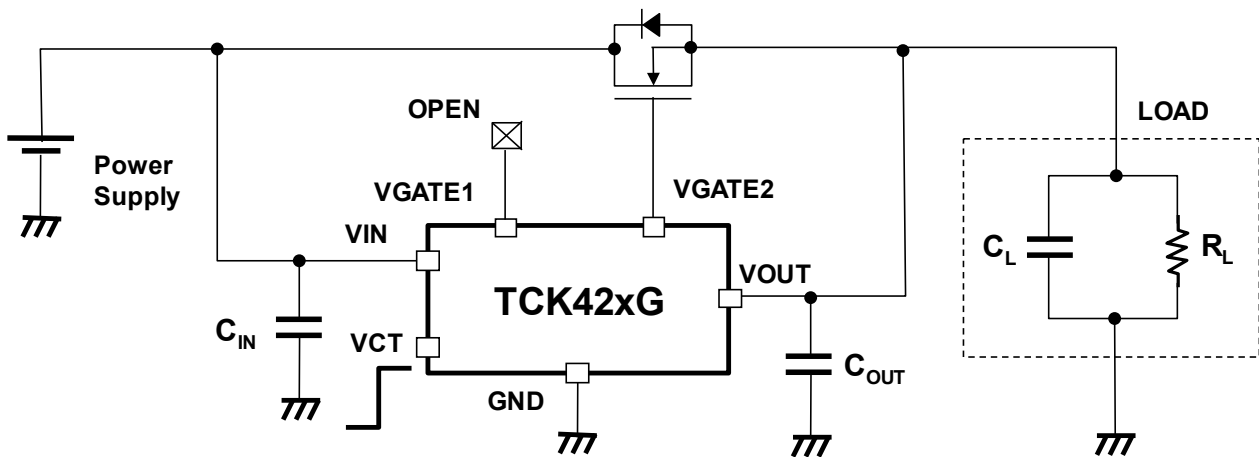
2. Turn ON and OFF ( $I_{OUT} = 3\text{ A}$ )



3. Over Voltage Lock Out



### 12.2. Single N-channel MOSFET circuit example



- Input and Output capacitor**  
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- VCT pin**  
 VCT pin is pull down connection to GND. VCT High level voltage must be under 5.5V  $V_{IH}$  max.
- VGATE1,2 pin and VOUT pin**  
 VGATE1 pin is OPEN state/Non connection. VGATE2 pin is connected to Gate of MOSFET. VOUT pin is connected to Source of MOSFET. When the gate driver IC turns off state, VGATE2 terminal voltage is close to VOUT voltage dropped by parasitic diode forward voltage. This circuit works to protect over voltage for MOSFET Gate-Source terminal.
- Turn on recovery time after Over Voltage Lock Out**  
 Once  $V_{IN}$  is in normal voltage range after OVLO, the turn on recovery time is similar  $V_{GS}$  ON time ( $t_{ON}$ ).
- Under Voltage Lock Out (UVLO) and Over Voltage Lock Out (OVLO)**  
 UVLO and OVLO are designed in these products, but these are not designed to constantly ensure the suppression of the gate driver IC and external MOSFETs within operation limits. Depending on the condition during actual usage, it could affect the electrical characteristic specification and reliability. To select external MOSFETs, please consider enough electrical design margin. When using these products, please read through and understand the concept of dissipation for absolute maximum ratings from the above mention or our 'Semiconductor Reliability Handbook'. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommends inserting failsafe system into the design.

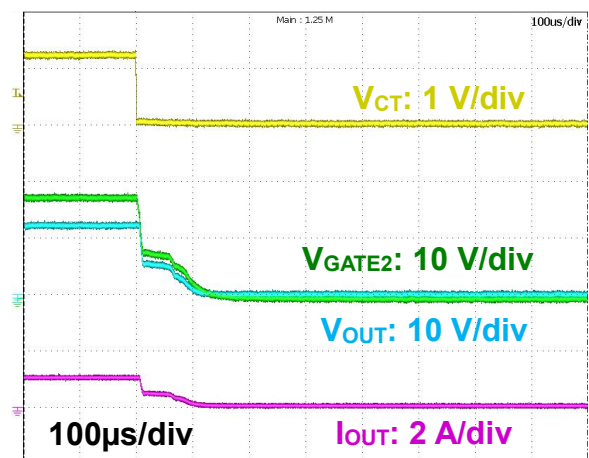
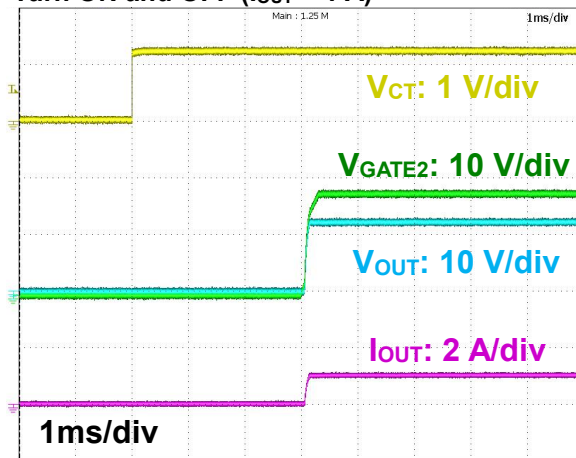
### Single N-channel MOSFET Switching Waveform

Typical switching waveforms with TOSHIBA MOSFETs

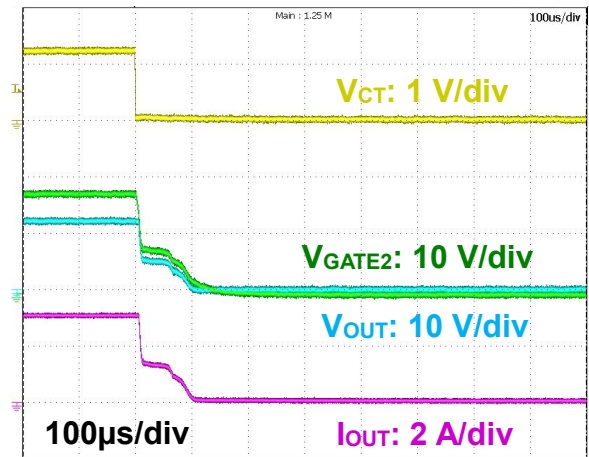
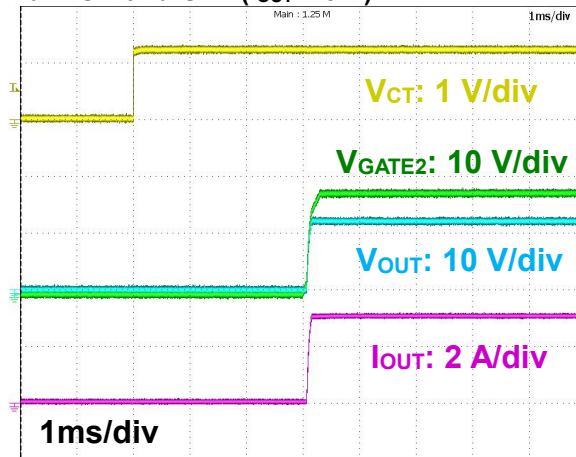
OVP Gate Driver IC	MOSFET		Test conditions	
	Part Number	Description	Turn ON and OFF	Over Voltage Lock Out
TCK423G ( $V_{GS} = 5.6\text{ V}$ )	TPN1R603PL	Single N-channel MOSFET $V_{DS} = 30\text{ V}$ , $V_{GS} = \pm 20\text{ V}$ $R_{DS(ON)} = 1.2\text{ m}\Omega$ typ at $V_{GS} = 10\text{ V}$ Package: TSON Advance	$V_{IN} = 12\text{ V}$ (TCK423G) $V_{IN} = 20\text{ V}$ (TCK421G) $I_{OUT} = 1\text{ A}, 3\text{ A}$ $C_{IN} = 1\text{ }\mu\text{F}$ $C_{OUT} = 1\text{ }\mu\text{F}$ $V_{CT} = 0\text{ V} \Leftrightarrow 1.2\text{ V}$ $T_a = 25\text{ }^\circ\text{C}$	$V_{IN} = 12\text{ V} \Leftrightarrow 15\text{ V}$ (TCK423G) $V_{IN} = 20\text{ V} \Leftrightarrow 25\text{ V}$ (TCK421G) $I_{OUT} = 1\text{ A}$ $C_{IN} = 1\text{ }\mu\text{F}$ $C_{OUT} = 1\text{ }\mu\text{F}$ $V_{CT} = 1.2\text{ V}$ $T_a = 25\text{ }^\circ\text{C}$
TCK421G ( $V_{GS} = 10\text{ V}$ )	TPHR6503PL1	Single N-channel MOSFET $V_{DS} = 30\text{ V}$ , $V_{GS} = \pm 20\text{ V}$ $R_{DS(ON)} = 0.41\text{ m}\Omega$ typ at $V_{GS} = 10\text{ V}$ Package: SOP Advance(N)		

#### TCK423G + TPN1R603L

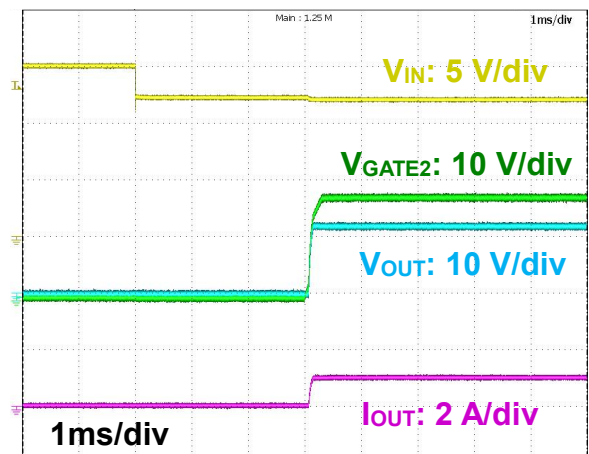
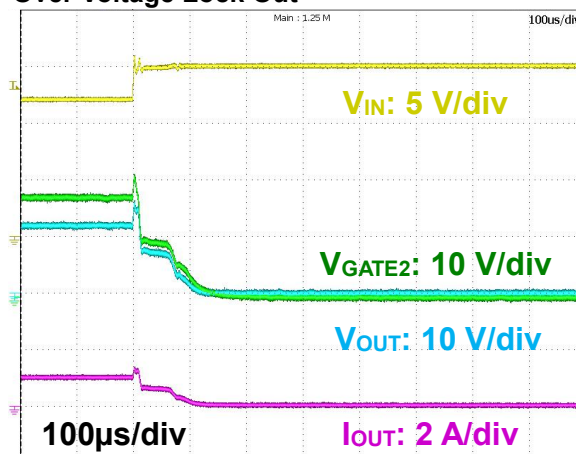
##### 1. Turn ON and OFF ( $I_{OUT} = 1\text{ A}$ )



##### 2. Turn ON and OFF ( $I_{OUT} = 3\text{ A}$ )

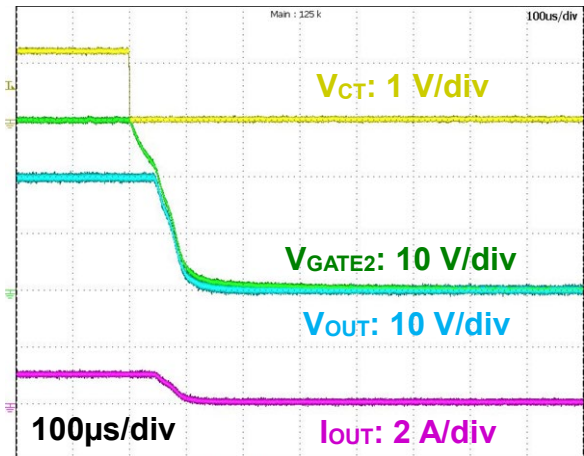
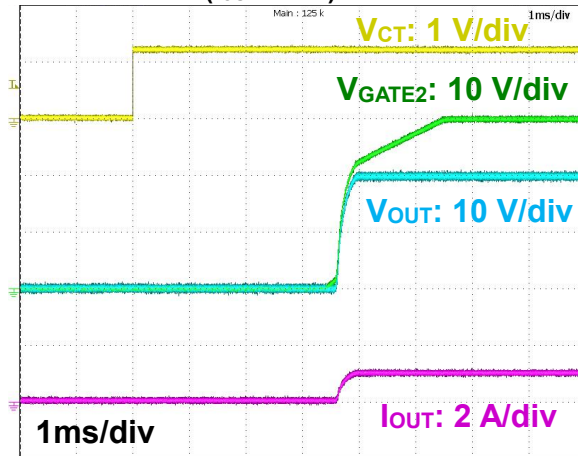


##### 3. Over Voltage Lock Out

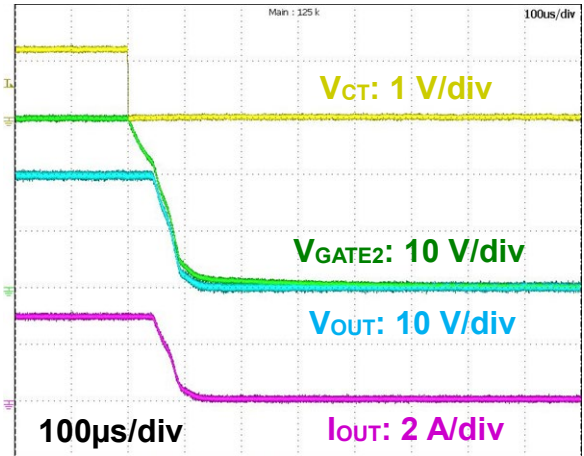
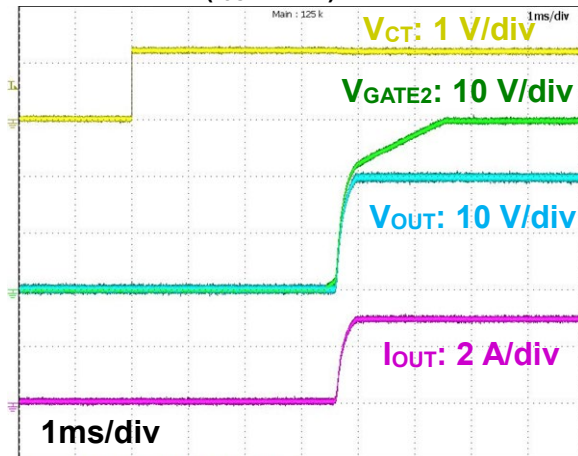


### TCK421G + TPHP6503PL1

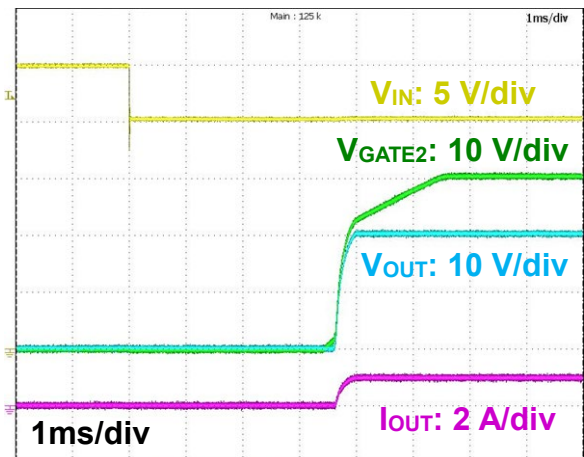
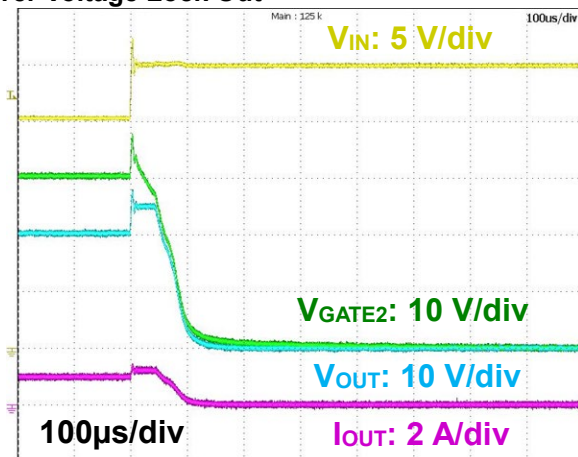
#### 6. Turn ON and OFF ( $I_{OUT} = 1\text{ A}$ )



#### 7. Turn ON and OFF ( $I_{OUT} = 3\text{ A}$ )



#### 8. Over Voltage Lock Out

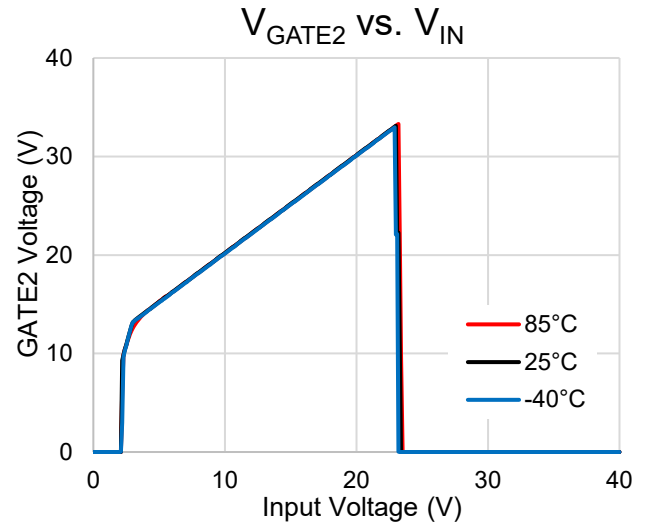
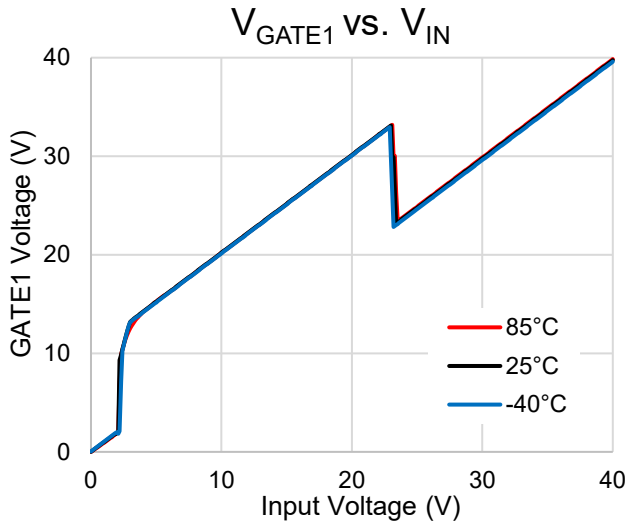




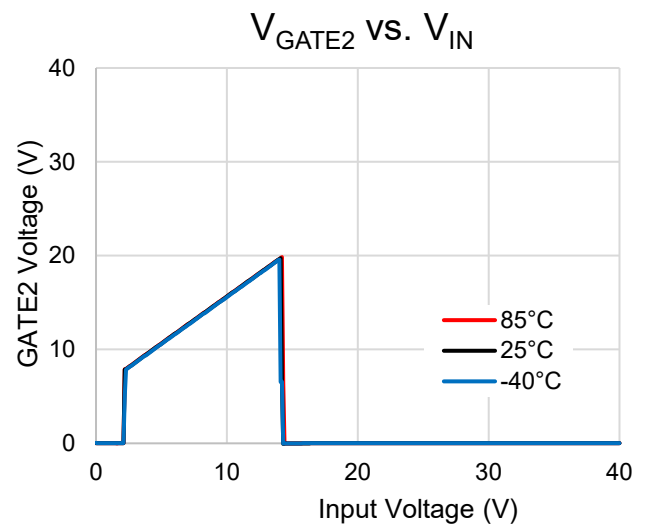
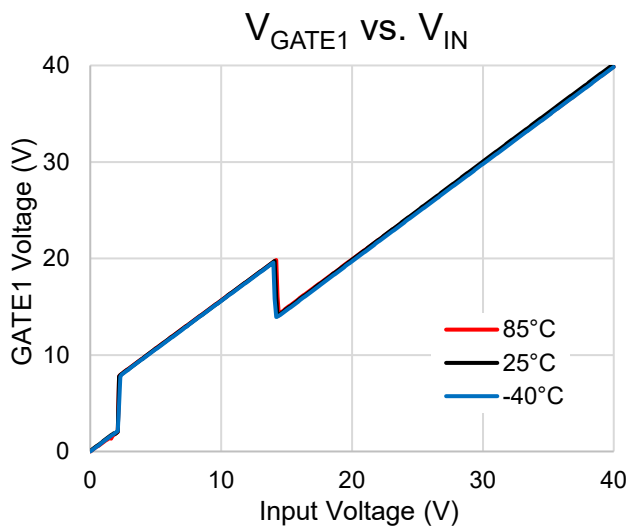
### 13. Representative Typical Characteristics

#### 13.1. Gate voltage vs. Input voltage

$V_{GS} = 10\text{ V}$  (TCK421G)



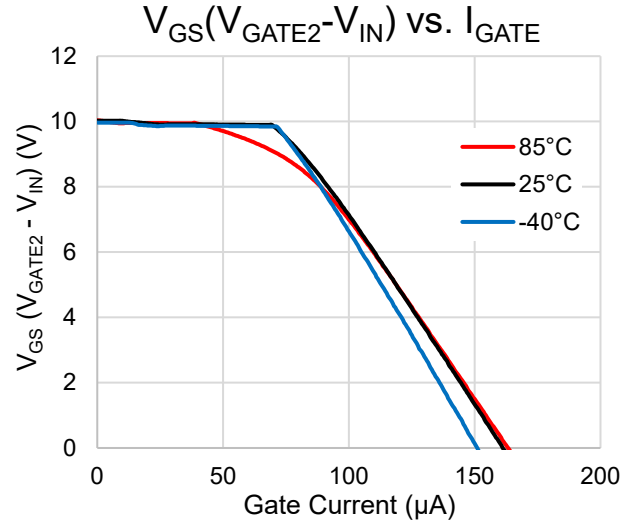
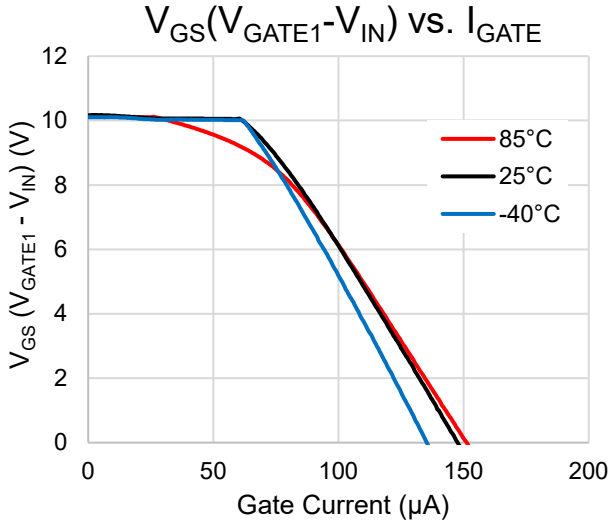
$V_{GS} = 5.6\text{ V}$  (TCK423G)



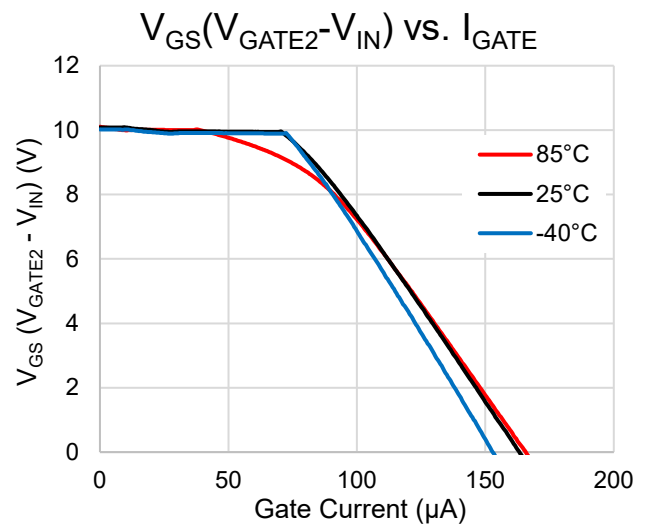
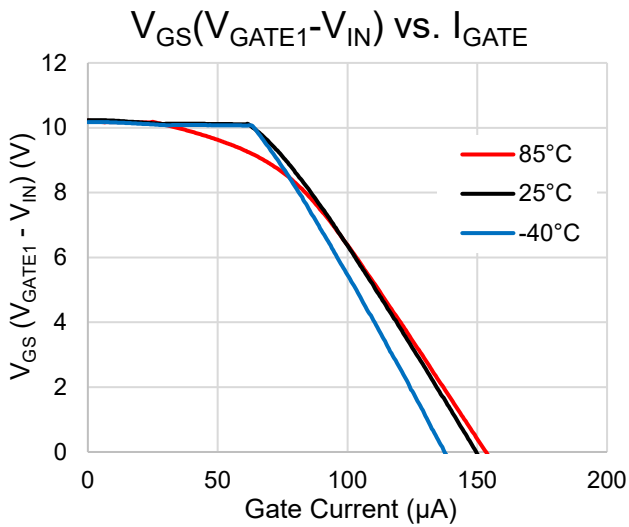
### 13.2. Gate voltage vs. Gate current

#### 1. $V_{GS} = 10V$ (TCK421G)

$V_{IN} = 20 V$

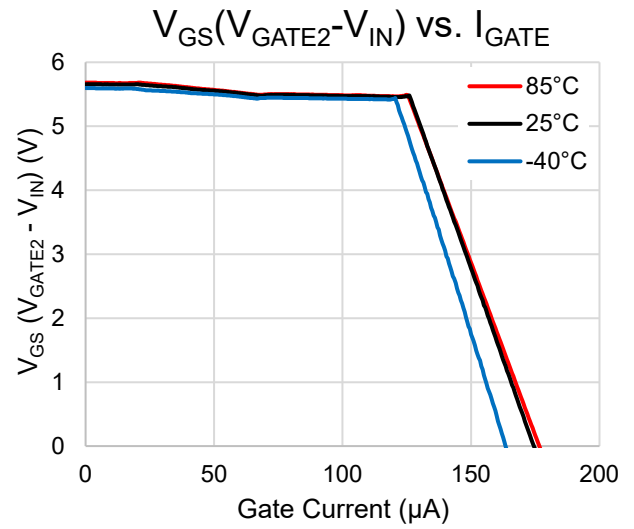
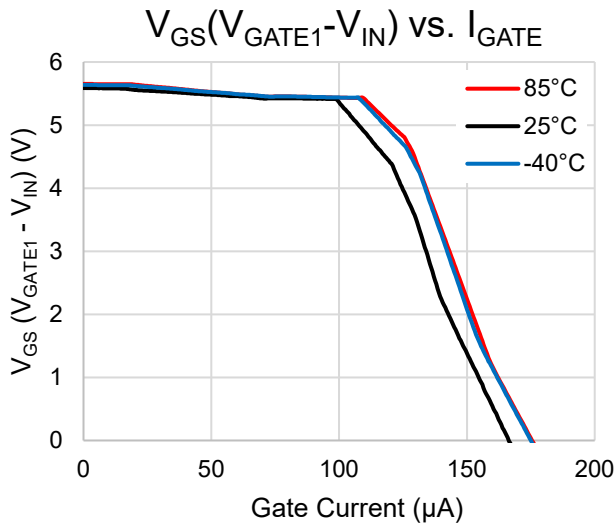


$V_{IN} = 12 V$

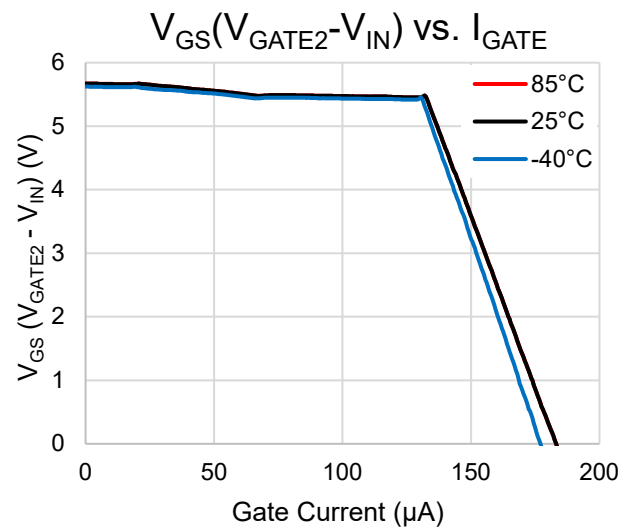
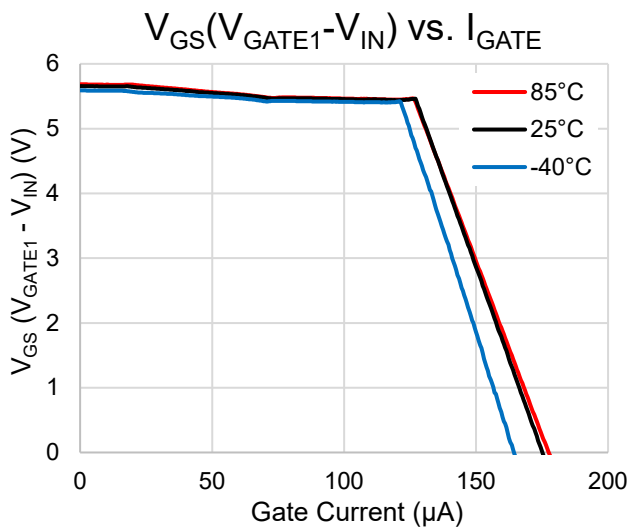


### 2. $V_{GS} = 5.6\text{ V}$ (TCK423G)

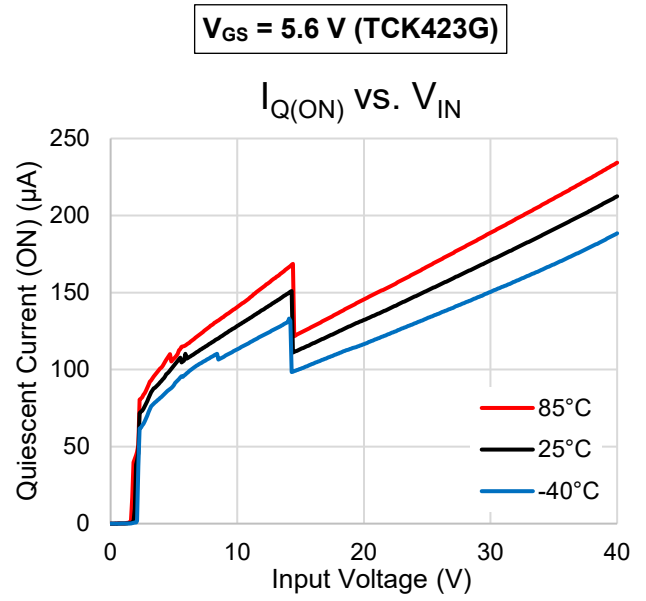
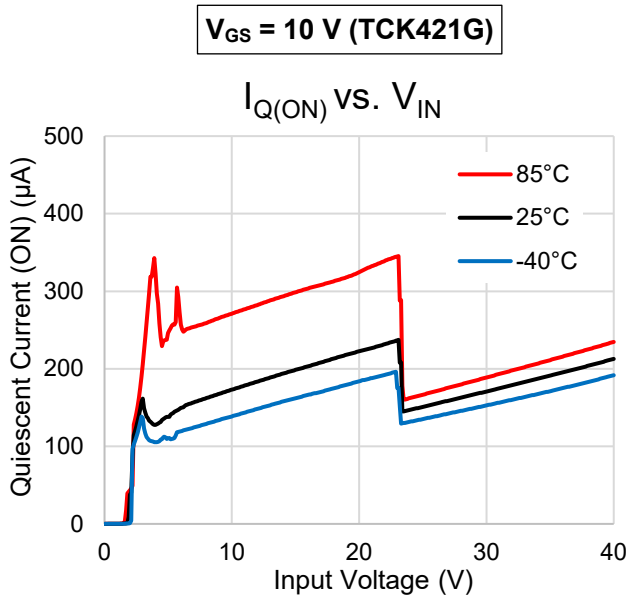
$V_{IN} = 12\text{ V}$



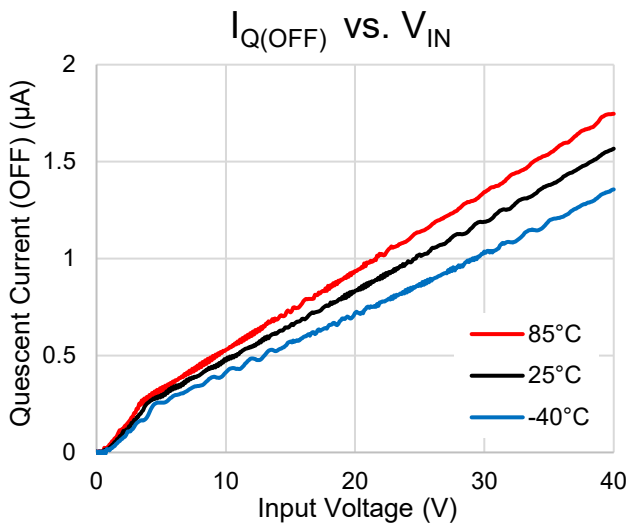
$V_{IN} = 9\text{ V}$



### 13.3. Quiescent current vs. Input voltage



### 13.4. Standby current vs. Input voltage (Note 6)

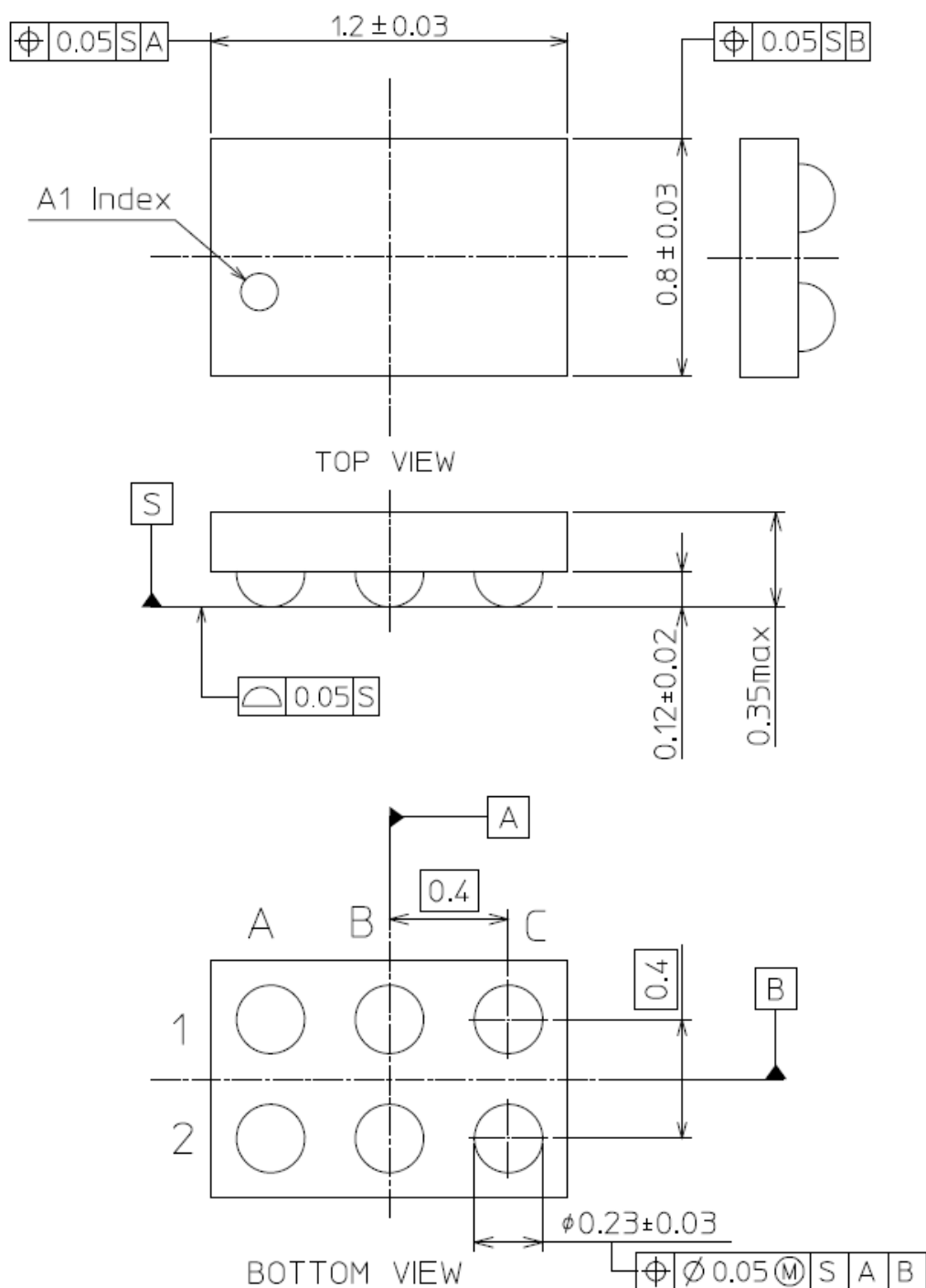


Note 6: Common characteristic of  $V_{GS} = 10\text{ V}$  and  $5.6\text{ V}$

### 14. Package Information

WCSP6G

Unit: mm

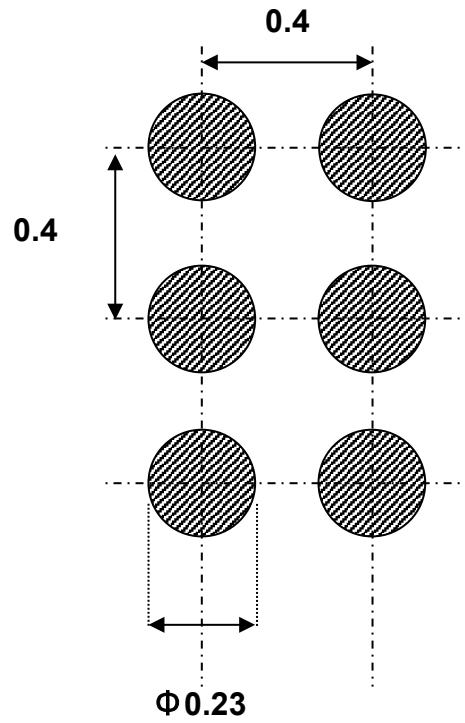


Weight: 0.61 mg (Typ.)

### 15. Land pattern dimensions for reference only

WCSP6G

Unit: mm



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