MOSFETs Silicon N-Channel MOS (DTMOSIV)

TK100L60W

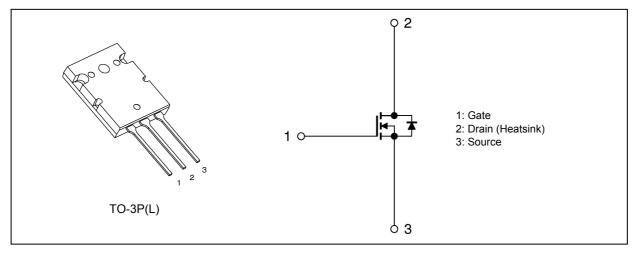
1. Applications

Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 0.015 \Omega$ (typ.) by used to Super Junction Structure : DTMOS
- (2) Easy to control Gate switching
- (3) Enhancement mode: V_{th} = 2.7 to 3.7 V (V_{DS} = 10 V, I_D = 5 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25^{\circ}C$ unless otherwise specified)

| Characteristics | Symbol | Rating | Unit | |
|-------------------------------------|----------|------------------|------------|-------|
| Drain-source voltage | | V _{DSS} | 600 | V |
| Gate-source voltage | | V _{GSS} | ±30 | |
| Drain current (DC) | (Note 1) | Ι _D | 100 | A |
| Drain current (pulsed) | (Note 1) | I _{DP} | 400 | 1 |
| Power dissipation (T _c = | 25°C) | PD | 797 | W |
| Single-pulse avalanche energy | (Note 2) | E _{AS} | 1582 | mJ |
| Avalanche current | | I _{AR} | 25 | A |
| Reverse drain current (DC) | (Note 1) | I _{DR} | 100 | |
| Reverse drain current (pulsed) | (Note 1) | I _{DRP} | 400 | 1 |
| Channel temperature | | T _{ch} | 150 | °C |
| Storage temperature | | T _{stg} | -55 to 150 |] |
| Mounting torque | | TOR | 0.8 | N · m |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production 2012-10 2013-12-25

5. Thermal Characteristics

| Characteristics | Symbol | Max | Unit |
|---------------------------------------|-----------------------|-------|------|
| Channel-to-case thermal resistance | R _{th(ch-c)} | 0.157 | °C/W |
| Channel-to-ambient thermal resistance | R _{th(ch-a)} | 35.7 | |

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 4.43 mH, R_G = 25 Ω , I_{AR} = 25 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

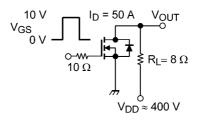
6. Electrical Characteristics

6.1. Static Characteristics (Ta = 25°C unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Тур. | Max | Unit |
|--------------------------------|----------------------|--|-----|-------|-------|------|
| Gate leakage current | I _{GSS} | V_{GS} = ±30 V, V_{DS} = 0 V | _ | _ | ±5 | μA |
| Drain cut-off current | I _{DSS} | V _{DS} = 600 V, V _{GS} = 0 V | _ | _ | 10 | |
| Drain-source breakdown voltage | V _{(BR)DSS} | I _D = 10 mA, V _{GS} = 0 V | 600 | _ | — | V |
| Gate threshold voltage | V _{th} | V _{DS} = 10 V, I _D = 5 mA | 2.7 | — | 3.7 | |
| Drain-source on-resistance | R _{DS(ON)} | V _{GS} = 10 V, I _D = 50 A | | 0.015 | 0.018 | Ω |

6.2. Dynamic Characteristics ($T_a = 25^{\circ}C$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Тур. | Max | Unit |
|--------------------------------|--------------------|---|-----|-------|-----|------|
| Input capacitance | C _{iss} | V _{DS} = 300 V, V _{GS} = 0 V, f = 100 kHz | _ | 15000 | _ | pF |
| Reverse transfer capacitance | C _{rss} |] | | 50 | _ | |
| Output capacitance | C _{oss} |] | _ | 320 | _ | |
| Effective output capacitance | C _{o(er)} | V_{DS} = 0 to 400 V, V_{GS} = 0 V | _ | 530 | _ | |
| Gate resistance | r _g | V _{DS} = OPEN, f = 1 MHz | _ | 1.8 | _ | Ω |
| Switching time (rise time) | t _r | See Figure 6.2.1 | _ | 130 | _ | ns |
| Switching time (turn-on time) | t _{on} |] | | 230 | _ | |
| Switching time (fall time) | t _f |] | | 125 | _ | |
| Switching time (turn-off time) | t _{off} |] | | 690 | | |
| MOSFET dv/dt ruggedness | dv/dt | V _{DD} = 0 to 400 V, I _D = 25 A | 50 | _ | _ | V/ns |



$$\label{eq:buty} \begin{split} & \text{Duty} \leq 1\%, \ t_w = 10 \ \mu s \\ & \text{Fig. 6.2.1} \quad \text{Switching Time Test Circuit} \end{split}$$

6.3. Gate Charge Characteristics ($T_a = 25^{\circ}C$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Тур. | Max | Unit |
|---|------------------|---|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | Qg | $V_{DD} \approx 400 \text{ V}, V_{GS} \text{ = } 10 \text{V}, \text{I}_{D} \text{ = } 100 \text{A}$ | _ | 360 | — | nC |
| Gate-source charge 1 | Q _{gs1} | | _ | 78 | _ | |
| Gate-drain charge | Q _{gd} | | _ | 140 | _ | |

6.4. Source-Drain Characteristics ($T_a = 25^{\circ}C$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Тур. | Max | Unit |
|-------------------------------|------------------|---|-----|------|------|------|
| Diode forward voltage | V _{DSF} | I _{DR} = 100 A, V _{GS} = 0 V | _ | _ | -1.7 | V |
| Reverse recovery time | t _{rr} | I _{DR} = 50 A, V _{GS} = 0 V | _ | 580 | — | ns |
| Reverse recovery charge | Q _{rr} | -dI _{DR} /dt = 50 A/μs | _ | 9 | — | μC |
| Peak reverse recovery current | l _{rr} | | _ | 30 | _ | А |
| Diode dv/dt ruggedness | dv/dt | I_{DR} = 50 A, V_{GS} = 0 V, V_{DD} = 400 V | 15 | _ | _ | V/ns |

7. Marking (Note)

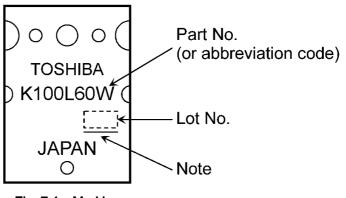


Fig. 7.1 Marking

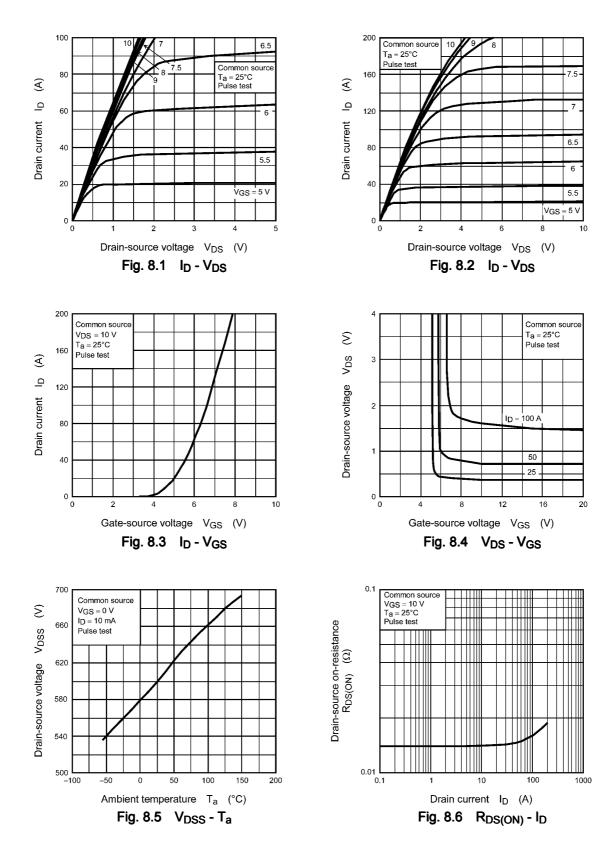
Note: A line under a Lot No. identifies the indication of product Labels. Not underlined: [[Pb]]/INCLUDES > MCV

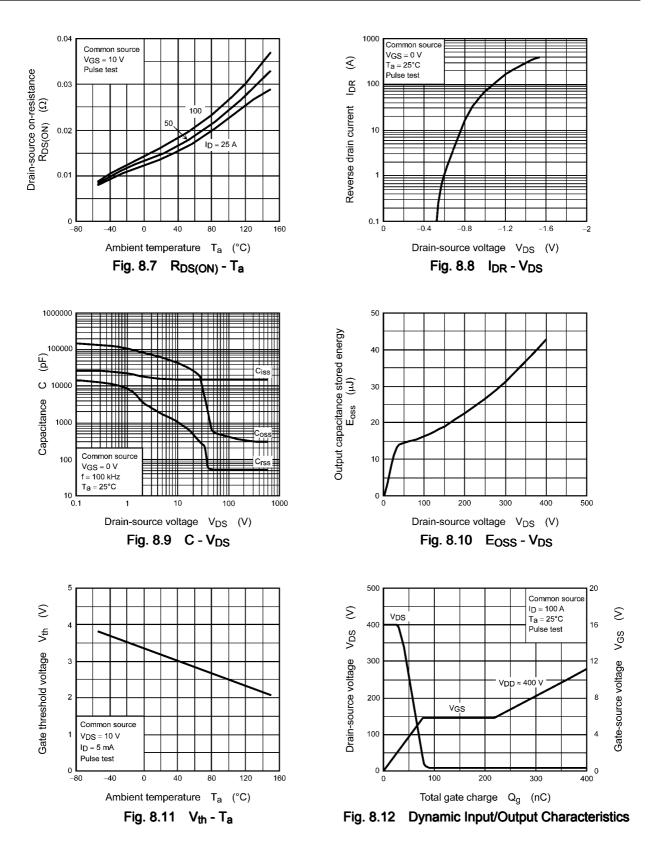
Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

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8. Characteristics Curves (Note)





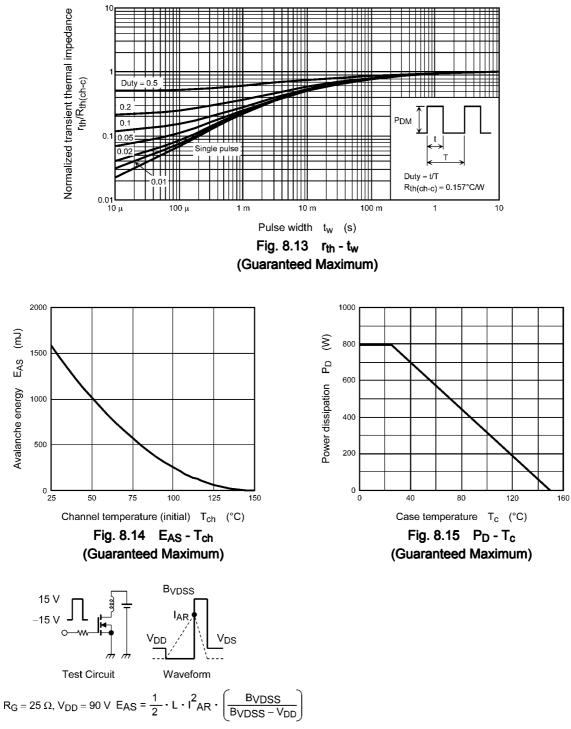
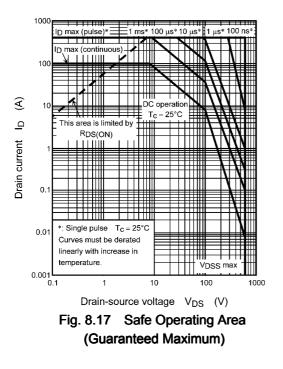


Fig. 8.16 Test Circuit/Waveform



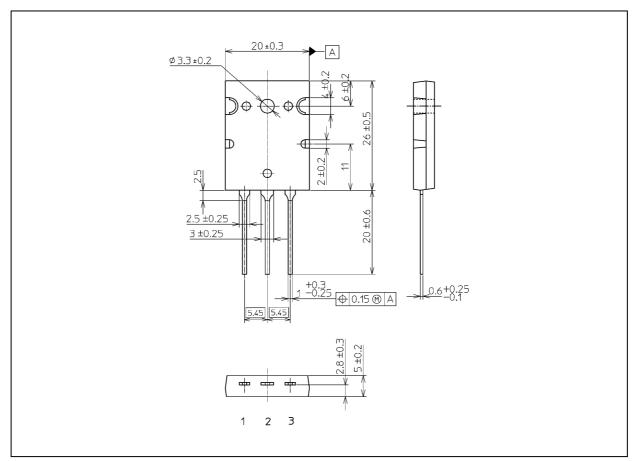
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



TK100L60W

Package Dimensions

Unit: mm



Weight: 9.75 g (typ.)

| Package Name(s) | | | |
|--------------------|--|--|--|
| TOSHIBA: 2-21F1S | | | |
| Nickname: TO-3P(L) | | | |

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