

MOSFETs Silicon N-channel MOS (U-MOS X-H)

## TK5R1A08QM

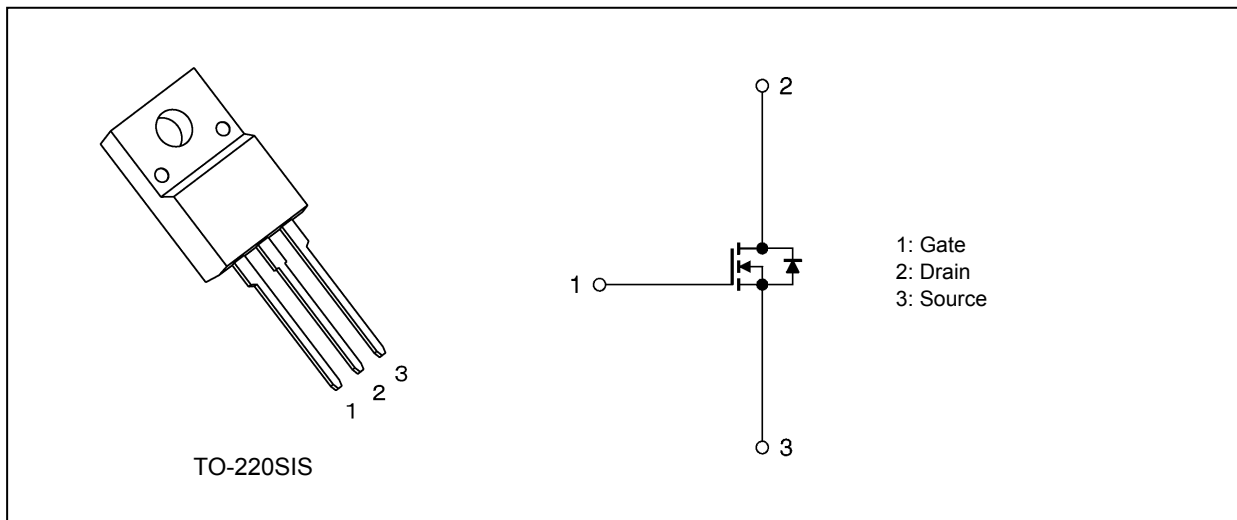
### 1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

### 2. Features

- (1) High-speed switching
- (2) Small gate charge:  $Q_{SW} = 17 \text{ nC}$  (typ.)
- (3) Small output charge:  $Q_{OSS} = 66 \text{ nC}$  (typ.)
- (4) Low drain-source on-resistance:  $R_{DS(ON)} = 4.1 \text{ m}\Omega$  (typ.) ( $V_{GS} = 10 \text{ V}$ )
- (5) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 80 \text{ V}$ )
- (6) Enhancement mode:  $V_{th} = 2.5 \text{ to } 3.5 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.7 \text{ mA}$ )

### 3. Packaging and Internal Circuit



Start of commercial production

2021-01

### 4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ °C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	80	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	
Drain current (DC) ( $T_c = 25\text{ °C}$ ) (Note 1)	$I_D$	70	A
Drain current (DC) (Silicon limit) (Note 1), (Note 2)	$I_D$	71	
Drain current (pulsed) ( $t = 100\text{ }\mu\text{s}$ ) (Note 1)	$I_{DP}$	320	
Power dissipation ( $T_c = 25\text{ °C}$ )	$P_D$	45	W
Single-pulse avalanche energy (Note 3)	$E_{AS}$	36	mJ
Single-pulse avalanche current (Note 3)	$I_{AS}$	70	A
Channel temperature	$T_{ch}$	175	°C
Storage temperature	$T_{stg}$	-55 to 175	
Isolation voltage (RMS) ( $t = 1.0\text{ s}$ )	$V_{ISO(RMS)}$	2000	V
Mounting torque	TOR	0.6	N · m

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance ( $T_c = 25\text{ °C}$ )	$R_{th(ch-c)}$	3.33	°C/W
Channel-to-ambient thermal resistance ( $T_a = 25\text{ °C}$ )	$R_{th(ch-a)}$	62.5	

Note 1: Ensure that the channel temperature does not exceed 175 °C.

Note 2: Limited 70 A by package capability.

Note 3:  $V_{DD} = 64\text{ V}$ ,  $T_{ch} = 25\text{ °C}$  (initial),  $L = 5.8\text{ }\mu\text{H}$ ,  $I_{AS} = 70\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

### 6. Electrical Characteristics

#### 6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 0.1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	80	—	—	V
Drain-source breakdown voltage (Note 4)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	60	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 0.7\text{ mA}$	2.5	—	3.5	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 6\text{ V}, I_D = 32\text{ A}$	—	5.2	7.1	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	—	4.1	5.1	

Note 4: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

#### 6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	3980	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	55	—	
Output capacitance	$C_{oss}$		—	1000	—	
Gate resistance	$r_g$	—	—	1.6	2.4	$\Omega$
Switching time (rise time)	$t_r$	See Fig. 6.2.1	—	47	—	ns
Switching time (turn-on time)	$t_{on}$		—	65	—	
Switching time (fall time)	$t_f$		—	51	—	
Switching time (turn-off time)	$t_{off}$		—	101	—	

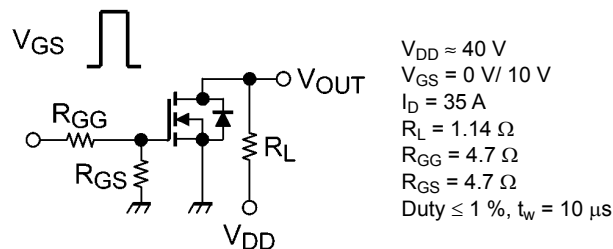


Fig. 6.2.1 Switching Time Test Circuit

#### 6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	—	54	—	nC
		$V_{DD} \approx 40\text{ V}, V_{GS} = 6\text{ V}, I_D = 32\text{ A}$	—	32	—	
Gate-source charge 1	$Q_{gs1}$	$V_{DD} \approx 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	—	14	—	
Gate-drain charge	$Q_{gd}$		—	12	—	
Gate switch charge	$Q_{SW}$		—	17	—	
Output charge	$Q_{oss}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	66	—	

### 6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 5)	$I_{DRP}$	$t = 100\ \mu\text{s}$	—	—	320	A
Diode forward voltage	$V_{DSF}$	$I_{DR} = 35\ \text{A}, V_{GS} = 0\ \text{V}$	—	—	-1.2	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 17.5\ \text{A}, V_{GS} = 0\ \text{V},$ $-di_{DR}/dt = 100\ \text{A}/\mu\text{s}$	—	45	—	ns
Reverse recovery charge	$Q_{rr}$		—	48	—	nC

Note 5: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

### 7. Marking (Note)

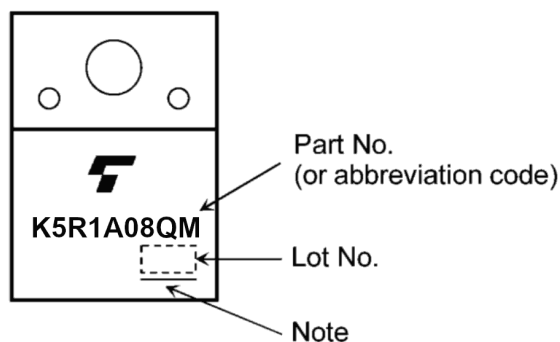


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined:  $[[\text{Pb}]]/\text{INCLUDES} > \text{MCV}$

Underlined:  $[[\text{G}]]/\text{RoHS COMPATIBLE}$  or  $[[\text{G}]]/\text{RoHS } [[\text{Pb}]]$

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

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### 8. Characteristics Curves (Note)

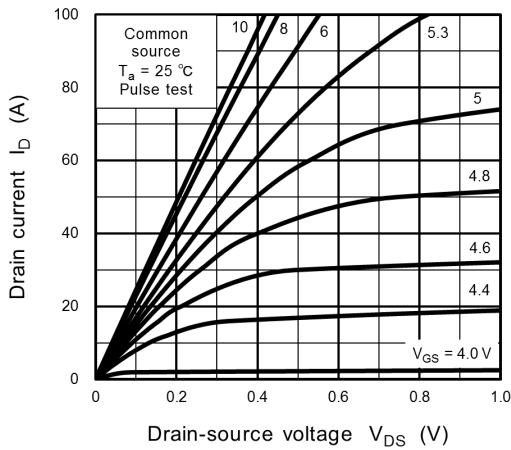


Fig. 8.1  $I_D - V_{DS}$

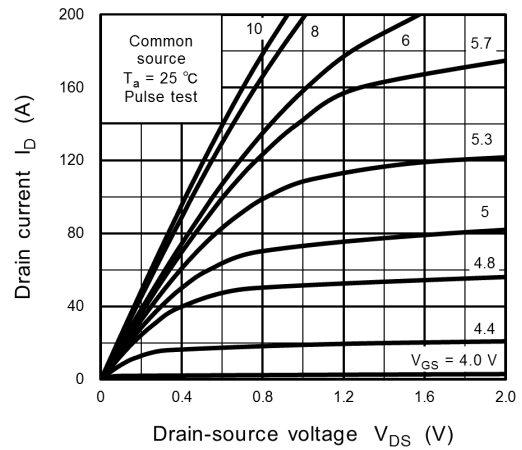


Fig. 8.2  $I_D - V_{DS}$

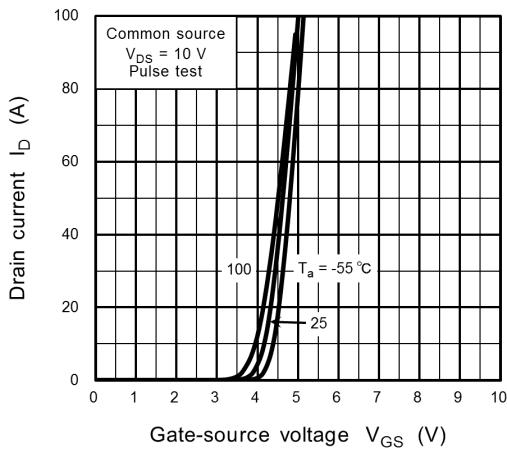


Fig. 8.3  $I_D - V_{GS}$

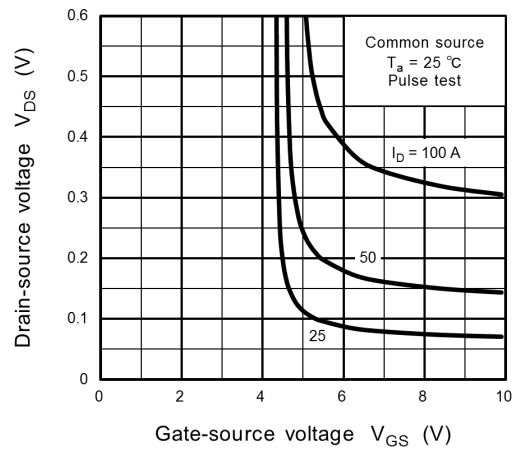


Fig. 8.4  $V_{DS} - V_{GS}$

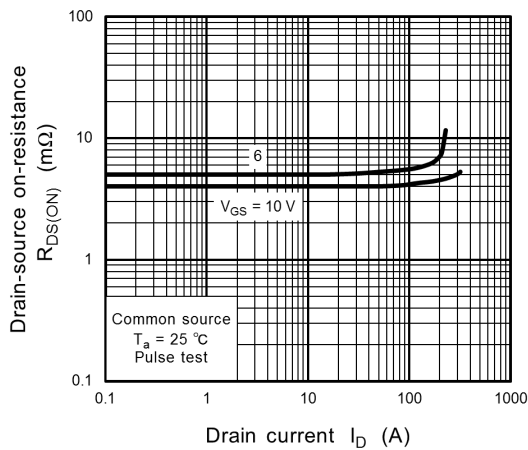


Fig. 8.5  $R_{DS(ON)} - I_D$

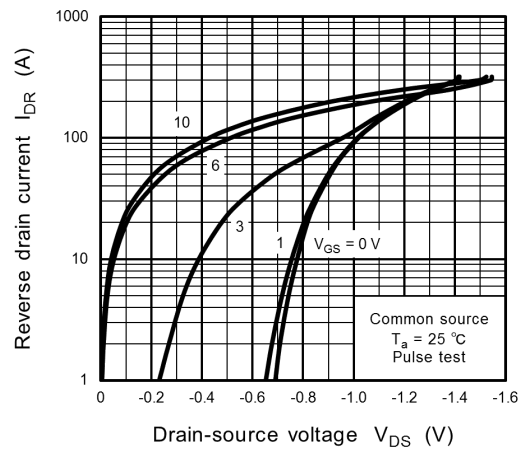
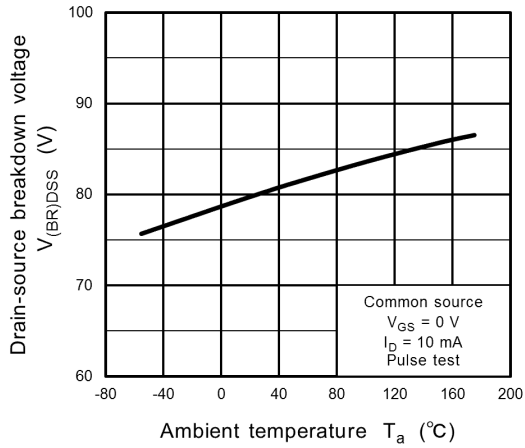
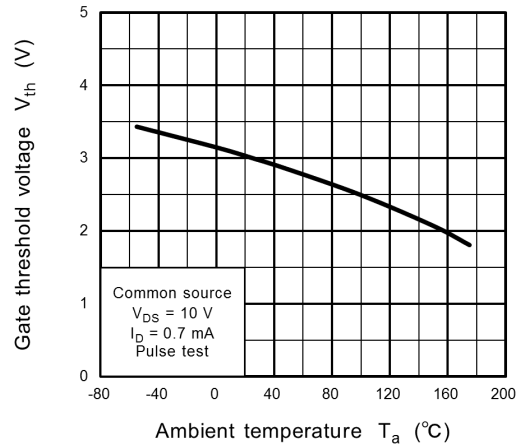


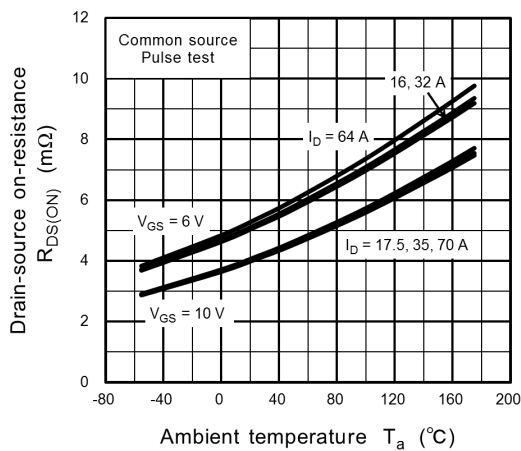
Fig. 8.6  $I_{DR} - V_{DS}$



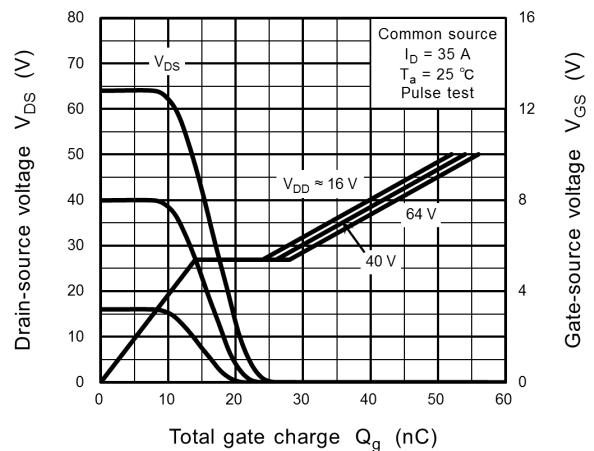
**Fig. 8.7**  $V_{(BR)DSS} - T_a$



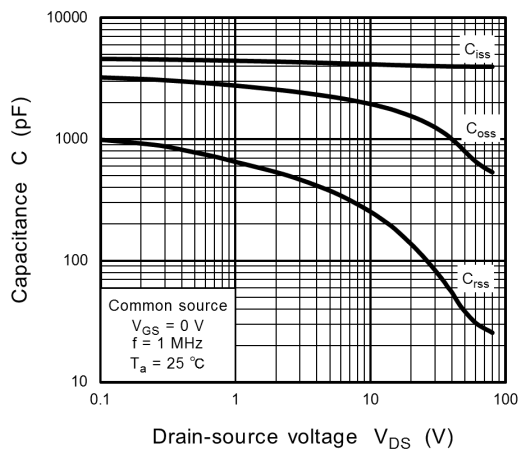
**Fig. 8.8**  $V_{th} - T_a$



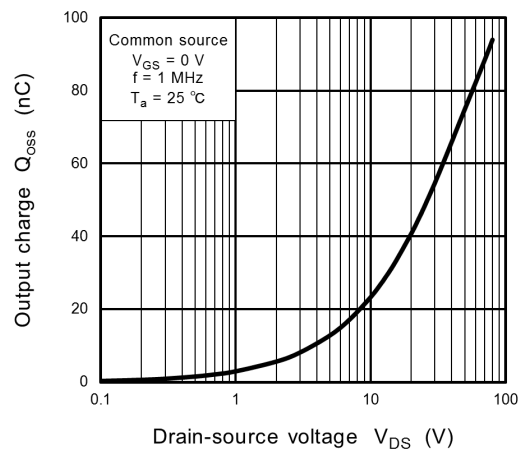
**Fig. 8.9**  $R_{DS(ON)} - T_a$



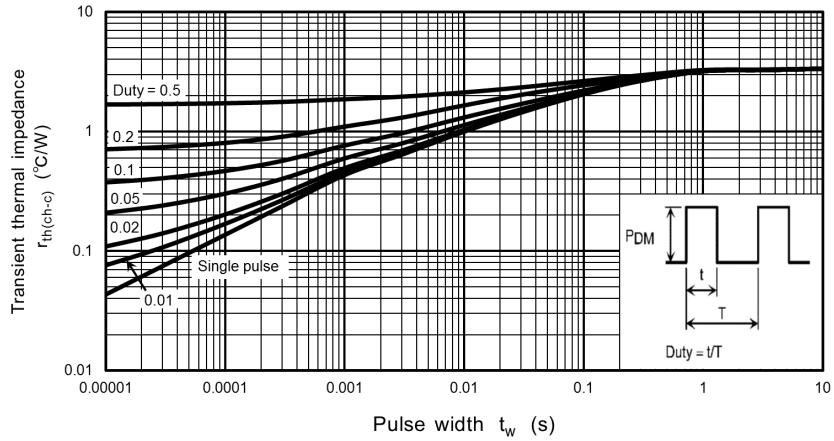
**Fig. 8.10** Dynamic Input/Output Characteristics



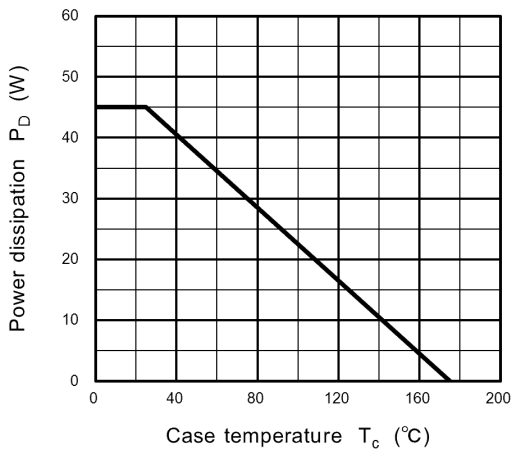
**Fig. 8.11** Capacitance -  $V_{DS}$



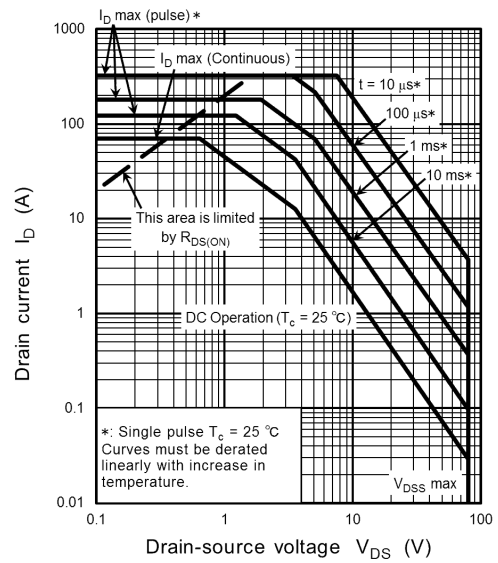
**Fig. 8.12**  $Q_{oss} - V_{DS}$



**Fig. 8.13  $r_{th} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.14  $P_D - T_c$**   
(Guaranteed Maximum)



**Fig. 8.15 Safe Operating Area**  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.





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