

# TLP105

- Isolated bus drivers
- High-speed line receivers
- Microprocessor system interfaces

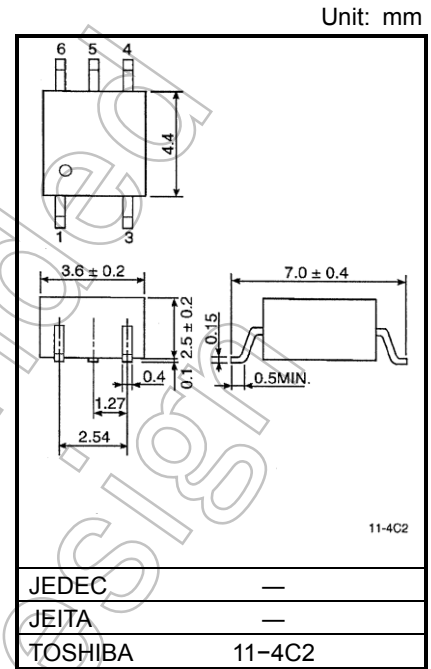
The Toshiba TLP105 consists of an infrared emitting diode optically coupled to a high-gain, high-speed photodetector. The TLP105 is housed in a 6-pin MFSOP. With a totem-pole output, the TLP105 is capable of both sinking and sourcing current. The TLP105 has an internal Faraday shield, which provides a guaranteed common-mode transient immunity of  $\pm 10$  kV/ $\mu$ s. The TLP105 has a noninverting output. An inverting-output version, the TLP108, is also available.

- Buffer logic type (totem-pole output)
- Guaranteed Performance Over Temperature:  $-40$  to  $100^{\circ}\text{C}$
- Power Supply Voltage: 4.5 to 20 V
- Input Threshold Current:  $I_{FLH} = 1.6$  mA (max)
- Switching Time ( $t_{pLH}/t_{pHL}$ ): 250 ns (max)
- Common mode transient immunity:  $\pm 10$  kV/ $\mu$ s
- Isolation Voltage: 3750 Vrms
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved: EN 60747-5-5 (Note 1)

Note 1 : When a VDE approved type is needed, please designate the **Option(V4)**.

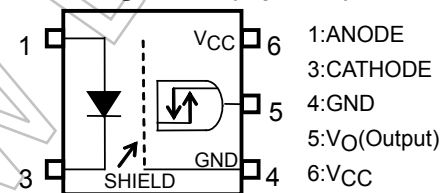
**Truth Table**

Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

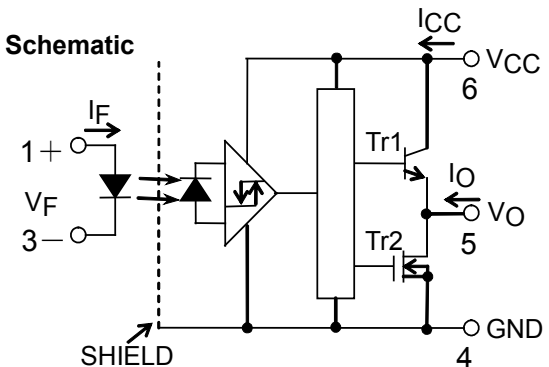


Weight: 0.09 g (typ.)

**Pin Configuration (top View)**



**Schematic**



**0.1  $\mu$ F bypass capacitor must be connected between pin 6 and 4.**

Start of commercial production  
2008-05

## Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON	$I_{F(ON)}$	2	—	10	mA
Input Voltage, OFF	$V_{F(OFF)}$	0	—	0.8	V
Supply Voltage*	$V_{CC}$	4.5	—	20	V
Operating Temperature	$T_{opr}$	-40	—	100	°C
Fan-out (TTL Load)	N	—	—	4	—

\* This item denotes operating range, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	$I_F$	20	mA
	Forward Current Derating ( $T_a \geq 83^\circ\text{C}$ )	$\Delta I_F / ^\circ\text{C}$	-0.48	mA/°C
	Peak Transient Forward Current (Note1)	$I_{FPT}$	1	A
	Reverse Voltage	$V_R$	5	V
	Input Power Dissipation	$P_o$	40	mW
	Input Power Dissipation derating ( $T_a \geq 83^\circ\text{C}$ )	$\Delta P_D / ^\circ\text{C}$	-0.95	mW/°C
DETECTOR	Output Current 1 ( $T_a \leq 25^\circ\text{C}$ )	$I_{O1}$	25/-15	mA
	Output Current 2 ( $T_a \leq 100^\circ\text{C}$ )	$I_{O2}$	5/-5	mA
	Output Current Derating ( $T_a \geq 25^\circ\text{C}$ )	$\Delta I_O / ^\circ\text{C}$	-0.26/-0.13	mA/°C
	Peak Output Current (Note2)	$I_{OP}$	50/-50	mA
	Output Voltage	$V_O$	-0.5 to 20	V
	Output Power Dissipation	$P_o$	75	mW
	Output Power Dissipation Derating ( $T_a \geq 25^\circ\text{C}$ )	$\Delta P_o / ^\circ\text{C}$	-0.75	mW/°C
	Supply Voltage	$V_{CC}$	-0.5 to 20	V
Operating Temperature Range		$T_{opr}$	-40 to 100	°C
Storage Temperature Range		$T_{sta}$	-55 to 125	°C
Lead Solder Temperature (10 s)		$T_{sol}$	260	°C
Isolation Voltage (AC, 60 s, R.H. $\leq 60\%$ ) (Note3)		$BV_s$	3750	$V_{rms}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width  $\leq 1 \mu\text{s}$ , 300 pps.

Note 2: Pulse width  $\leq 5 \mu\text{s}$ , duty cycle  $\leq 0.025$

Note 3: Device considered a two terminal device: pins 1 and 3 shorted together and pins 4, 5 and 6 shorted together.

## Electrical Characteristics

(Unless otherwise specified, Ta = -40 to 100°C, VCC = 4.5 to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT	
Input Forward Voltage	V <sub>F</sub>	—	I <sub>F</sub> = 10 mA, Ta = 25 °C	1.45	1.57	1.75	V	
Temperature Coefficient of Forward Voltage	ΔV <sub>F</sub> /ΔTa	—	I <sub>F</sub> = 10 mA	—	-2.0	—	mV/°C	
Input Reverse Current	I <sub>R</sub>	—	V <sub>R</sub> = 5 V, Ta = 25° C	—	—	10	μA	
Input Capacitance	C <sub>T</sub>	—	V = 0 V, f = 1 MHz, Ta = 25 °C	—	100	-	pF	
Logic Low Output Voltage	V <sub>OL</sub>	1	I <sub>OL</sub> = 3.5 mA, V <sub>F</sub> = 0.8 V	—	0.2	0.6	V	
Logic High Output Voltage	V <sub>OH</sub>	2	I <sub>OH</sub> = -2.6 mA, I <sub>F</sub> = 5 mA	V <sub>CC</sub> = 4.5 V	2.7	4.0	—	V
				V <sub>CC</sub> = 20 V	17.4	19.0	—	
Logic Low Supply Current	I <sub>CCL</sub>	3	V <sub>F</sub> = 0 V	V <sub>CC</sub> = 20 V	—	—	3.0	mA
				V <sub>CC</sub> = 5.5 V	—	—	3.0	
Logic High Supply Current	I <sub>CCH</sub>	4	I <sub>F</sub> = 5 mA	V <sub>CC</sub> = 20 V	—	—	3.0	mA
				V <sub>CC</sub> = 5.5 V	—	—	3.0	
Logic Low Short Circuit Output Current (Note 1)	I <sub>OSL</sub>	5	V <sub>F</sub> = 0 V	V <sub>CC</sub> = V <sub>O</sub> = 5.5 V	15	80	—	mA
				V <sub>CC</sub> = V <sub>O</sub> = 20 V	20	90	—	
Logic High Short Circuit Output Current (Note 1)	I <sub>OSH</sub>	6	I <sub>F</sub> = 5 mA, V <sub>O</sub> = GND	V <sub>CC</sub> = 5.5 V	-5	-15	—	mA
				V <sub>CC</sub> = 20 V	-10	-20	—	
Input Current Logic High Output	I <sub>FLH</sub>	—	I <sub>O</sub> = -2.6 mA, V <sub>O</sub> > 2.4 V	—	0.4	1.6	mA	
Input Voltage Logic Low Output	V <sub>FHL</sub>	—	I <sub>O</sub> = 3.5 mA, V <sub>O</sub> < 0.4 V	0.8	—	—	V	
Input Current Hysteresis	I <sub>HYS</sub>	—	V <sub>CC</sub> = 5 V	—	0.05	—	mA	

\*All typical values are at Ta = 25 °C

Note 1: Duration of output short circuit time should not exceed 10 ms.

Note : A ceramic capacitor (0.1 μA) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

## Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C <sub>S</sub>	V <sub>S</sub> = 0 V, f = 1 MHz	—	0.8	—	pF
Isolation resistance	R <sub>S</sub>	R.H. ≤ 60 %, V <sub>S</sub> = 500 V	1×10 <sup>12</sup>	10 <sup>14</sup>	—	Ω
Isolation voltage	BV <sub>S</sub>	AC, 60 s	3750	—	—	V <sub>rms</sub>

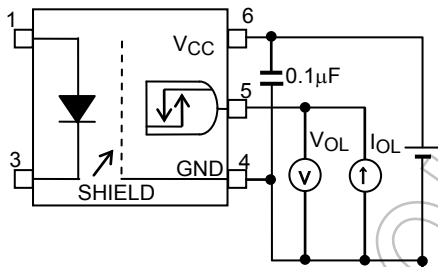
## Switching Characteristics

(Unless otherwise specified,  $T_a = -40$  to  $100^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $20\text{ V}$ )

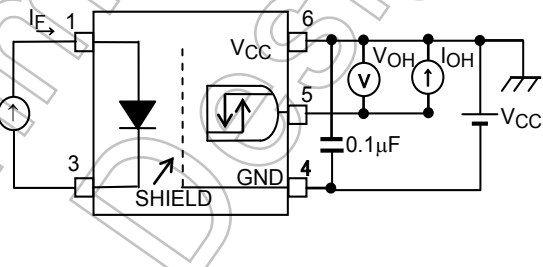
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time to Logic High output	$t_{pLH}$	7, 8	$I_F = 0 \rightarrow 3\text{ mA}$	30	150	250	ns
Propagation Delay Time to Logic Low output	$t_{pHL}$		$I_F = 3 \rightarrow 0\text{ mA}$	30	150	250	ns
Switching Time Dispersion between ON and OFF	$ t_{pHL} - t_{pLH} $		—	—	—	220	ns
Rise Time (10 – 90 %)	$t_r$		$I_F = 0 \rightarrow 3\text{ mA}$ , $V_{CC} = 5\text{ V}$	—	30	75	ns
Fall Time (90 – 10 %)	$t_f$		$I_F = 3 \rightarrow 0\text{ mA}$ , $V_{CC} = 5\text{ V}$	—	30	75	ns
Common Mode transient Immunity at High Level Output	$CM_H$	9	$V_{CM} = 1000\text{ V}_{p-p}$ , $I_F = 5\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $T_a = 25^\circ\text{C}$	-10000	—	—	$\text{V}/\mu\text{s}$
Common Mode transient Immunity at Low Level Output	$CM_L$		$V_{CM} = 1000\text{ V}_{p-p}$ , $I_F = 0\text{ mA}$ , $V_{CC} = 20\text{ V}$ , $T_a = 25^\circ\text{C}$	10000	—	—	$\text{V}/\mu\text{s}$

\*All typical values are at  $T_a = 25^\circ\text{C}$

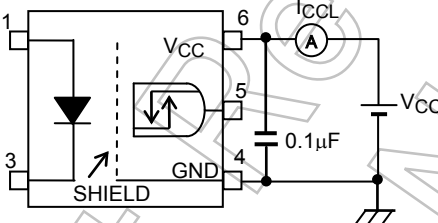
**Test Circuit 1: VOL**



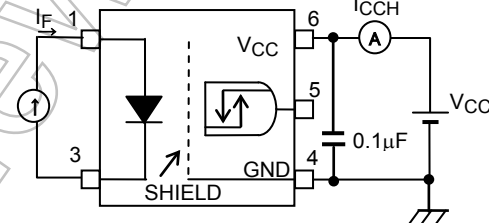
**Test Circuit 2: VOH**



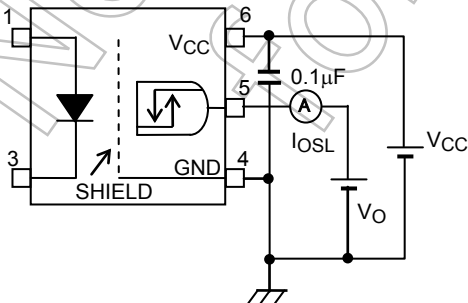
**Test Circuit 3: ICCL**



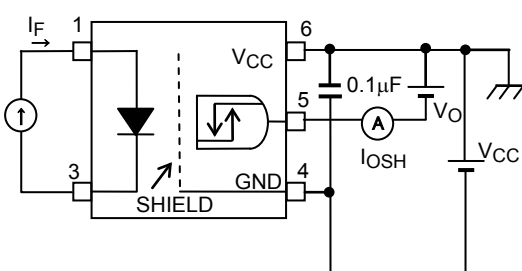
**Test Circuit 4: ICCH**



**Test Circuit 5: IOSL**

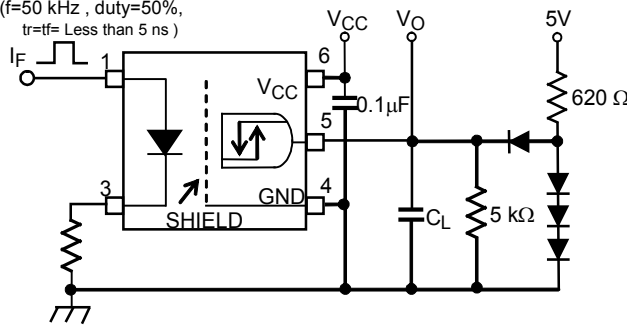


**Test Circuit 6: IOSH**

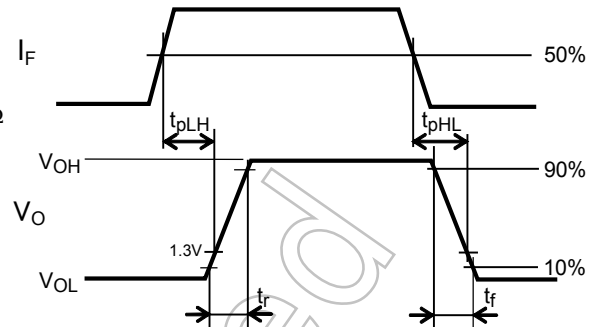


## Test Circuit 7: Switching Time Test Circuit

$I_F=3\text{ mA}$  (P.G)  
 ( $f=50\text{ kHz}$ , duty=50%,  
 $t_r=t_f$ = Less than 5 ns)

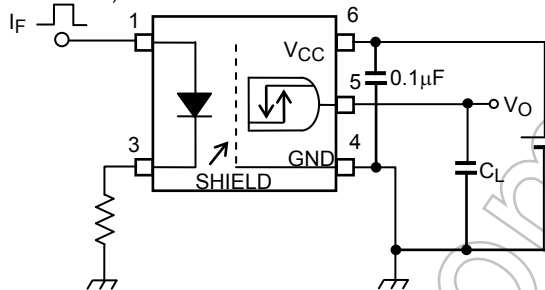


$C_L$  is approximately 15 pF which includes probe and stray capacitance.  
 P.G.: Pulse generator

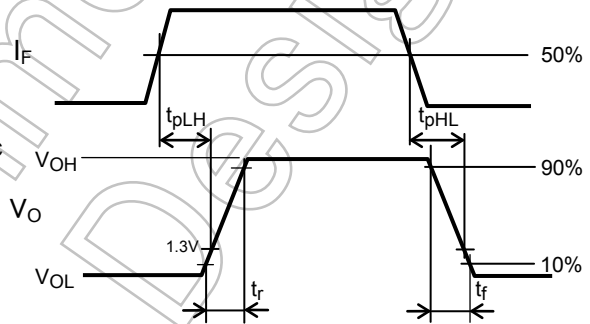


## Test Circuit 8: Switching Time Test Circuit

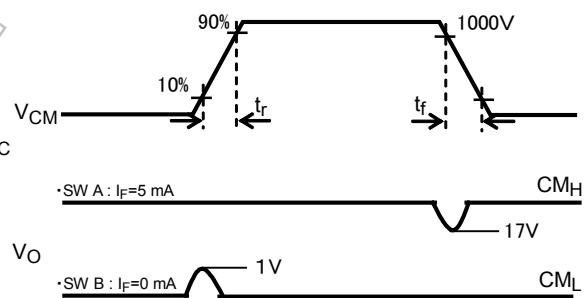
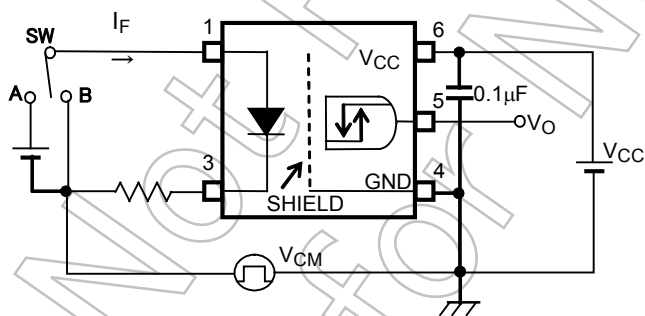
$I_F=3\text{ mA}$  (P.G)  
 ( $f=50\text{ kHz}$ , duty=50%,  
 $t_r=t_f$ = Less than 5 ns)



$C_L$  is approximately 15 pF which includes probe and stray capacitance.  
 P.G.: Pulse generator



## Test Circuit 9: Common Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{t_f(\mu s)} \quad CM_L = \frac{800(V)}{t_r(\mu s)}$$

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