

TLP2116

- Plasma Display Panels (PDP)
- High-Speed Interfaces
- Factory Automation (FA)

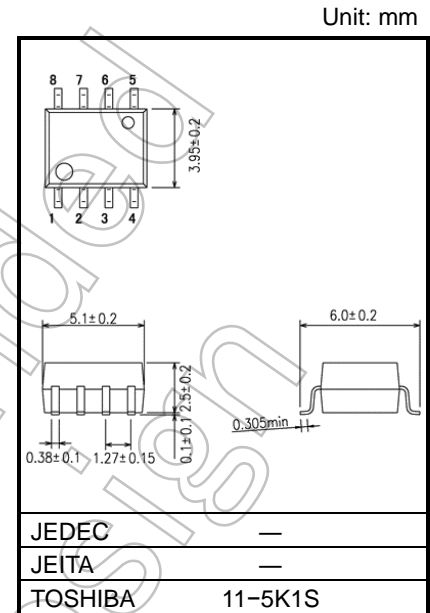
The TOSHIBA TLP2116 dual photocoupler consists of a pair of an infrared emitting diodes optically coupled to integrated high gain and high-speed photodetectors.

- Inverter logic (totem-pole output)
- Package: SO8
- Guaranteed performance over temperature : -40 to 100°C
- Power supply voltage: 4.5 to 5.5 V
- Input thresholds current: $I_{FHL} = 5 \text{ mA (max)}$
- Propagation delay time (tpHL/tpLH): 75 ns (max)
- Switching speed: 15 MBd (typ.) (NRZ)
- Common mode transient immunity: $\pm 10 \text{ kV}/\mu\text{s}$
- Isolation voltage: 2500 Vrms
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A

File No.E67349

- VDE-approved: EN 60747-5-5 (Note 1)

Note 1 : When a VDE approved type is needed,
Please designate the **Option(V4)**.

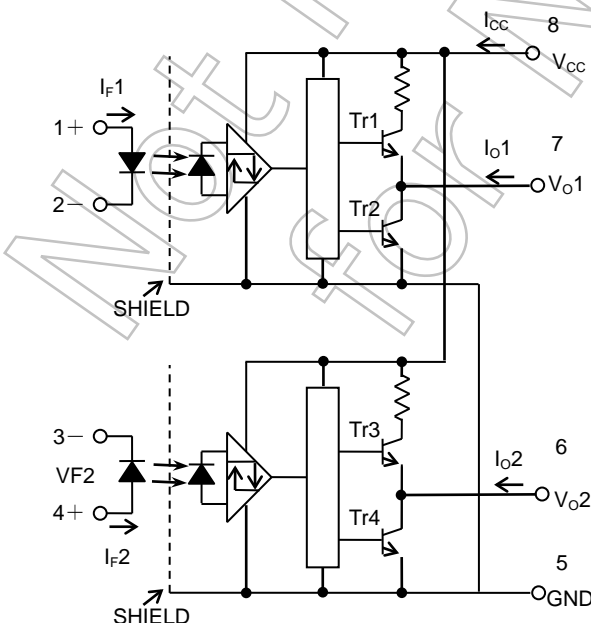


Weight: 0.11 g (typ.)

Truth Table

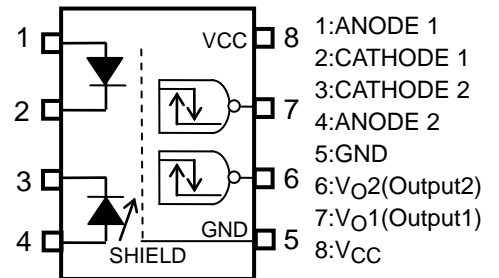
Input	LED1(2)	Tr1(3)	Tr2(4)	Output 1(2)
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Schematic



A bypass capacitor of 0.1 μF must be connected between pins 8 and 5.

Pin Configuration (Top View)



Start of commercial production
2008-02

Absolute Maximum Ratings (Ta=25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Each Channel)	I_F	20	mA
	Forward current derating (Ta ≥ 85°C) (Each Channel)	$\Delta I_F / \Delta T_a$	-0.5	mA/°C
	Peak transient forward current (Each Channel) (Note 1)	I_{FPT}	1	A
	Reverse voltage (Each Channel)	V_R	5	V
	Input Power Dissipation (Each Channel)	P_D	40	mW
	Input Power Dissipation Derating (Each Channel) (Ta ≥ 85°C)	$\Delta P_D / ^\circ C$	-1.0	mW/°C
DETECTOR	Output current (Each Channel)	I_O	10	mA
	Output voltage (Each Channel)	V_O	6	V
	Supply voltage	V_{CC}	6	V
	Output power dissipation (Each Channel)	P_O	40	mW
	Output Power Dissipation Derating (Ta ≥ 85°C) (Each Channel)	$\Delta P_O / ^\circ C$	-1.0	mW/°C
Operating temperature range		T_{opr}	-40 to 100	°C
Storage temperature range		T_{stg}	-55 to 125	°C
Lead solder temperature (10 s)		T_{sol}	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %, (Note 2)		BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width $PW \leq 1 \mu s$, 300 pps.

Note 2: This device is regarded as a two terminal device: pins 1, 2, 3 and 4 are shorted together, as are pins 5, 6, 7 and 8.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current, ON (Each Channel)	$I_{F(ON)}$	8	—	18	mA
Input voltage, OFF (Each Channel)	$V_{F(OFF)}$	0	—	0.8	V
Supply voltage(*) (Note 3)	V_{CC}	4.5	5.0	5.5	V
Operating temperature	T_{opr}	-40	—	100	°C

(*) This item denotes operating ranges, not meaning of recommended operating conditions.

Note 3: The detector of this product requires power supply voltage (VCC) of 4.5 V or higher for stable operation. If the VCC is lower than this value, ICCH may increase, or output may be unstable. Be sure to use the product after checking the supply current, and the operation of a power-on/-off.

Note: A ceramic capacitor (0.1 μF) should be connected from pin 8 (VCC) to pin 5 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Electrical Characteristics

(Unless otherwise specified, Ta = -40 to 100°C, Vcc = 4.5 to 5.5V)

Characteristic	Symbol	Conditions	Min	Typ.	Max	Unit
Input forward voltage (Each Channel)	V _F	I _F = 10 mA, Ta = 25 °C	1.3	1.65	1.75	V
Temperature coefficient of forward voltage (Each Channel)	ΔV _F /ΔTa	I _F = 10 mA	—	-2.0	—	mV/°C
Input reverse current (Each Channel)	I _R	V _R = 5 V, Ta = 25 °C	—	—	10	μA
Input capacitance (Each Channel)	C _T	V = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
Logic low output voltage (Each Channel)	V _{OL}	I _{OL} = 1.6 mA, I _F = 12 mA, V _{CC} = 5 V	—	—	0.4	V
Logic high output voltage (Each Channel)	V _{OH}	I _{OH} = -0.02 mA, V _F = 1.05 V, V _{CC} = 5 V	4.0	—	—	V
Logic low supply current	I _{CCL}	I _F = 12 mA	—	—	10.0	mA
Logic high supply current	I _{CCH}	V _F = 0 V (Note 3)	—	—	10.0	mA
Input current logic low output (Each Channel)	I _{FHL}	I _O = 1.6 mA, V _O < 0.4 V	—	—	5	mA
Input voltage logic high output (Each Channel)	V _{FLH}	I _O = -0.02 mA, V _O > 4.0 V	0.8	—	—	V

*All typical values are at Ta=25°C, V_{CC}=5 V unless otherwise specified

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Capacitance input to output	C _S	V _S = 0 V, f = 1 MHz (Note 2)	—	0.8	—	pF
Isolation resistance	R _S	R.H. ≤ 60%, V _S = 500 V (Note 2)	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 60 s (Note 2)	2500	—	—	V _{rms}

Switching Characteristics

(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 5.5V)(Each Channel)

Characteristic	Symbol	Test Circuit	Conditions	Min	Typ.	Max	Unit	
Propagation delay time to logic low output	t_{pHL}	1	$I_F = 0 \rightarrow 12 \text{ mA}$	$R_{IN} = 100 \Omega$ $C_L = 15 \text{ pF}$ (Note 5)	—	—	75	ns
Propagation delay time to logic high output	t_{pLH}		$I_F = 12 \rightarrow 0 \text{ mA}$		—	—	75	ns
Propagation delay time to logic low output	t_{pHL}	2	$V_{IN} = 0 \rightarrow 5 \text{ V}$ ($I_F = 0 \rightarrow 8 \text{ mA}$)	$R_{IN} = 430 \Omega$ $C_{IN} = 27 \text{ pF}$ $C_L = 15 \text{ pF}$ (Note 5)	—	—	75	ns
Propagation delay time to logic high output	t_{pLH}		$V_{IN} = 5 \rightarrow 0 \text{ V}$ ($I_F = 8 \rightarrow 0 \text{ mA}$)		—	—	75	ns
Switching time dispersion between ON and OFF	$ t_{pHL} - t_{pLH} $	1	$I_F = 12 \text{ mA}$, $R_{IN} = 100 \Omega$, $C_L = 15 \text{ pF}$ (Note 5)		—	—	30	ns
Output fall time (90 - 10%)	t_f		$I_F = 0 \rightarrow 12 \text{ mA}$	$R_{IN} = 100 \Omega$ $C_L = 15 \text{ pF}$ (Note 5)	—	15	—	ns
Output rise time (10 - 90%)	t_r		$I_F = 12 \rightarrow 0 \text{ mA}$		—	15	—	ns
Common mode transient immunity at high level output	CMH	3	$V_{CM} = 1000 \text{ Vp-p}$, $I_F = 0 \text{ mA}$, $V_O(\text{min}) = 4 \text{ V}$, $T_a = 25^\circ\text{C}$		10000	—	—	V/ μs
Common mode transient immunity at low level output	CM _L		$V_{CM} = 1000 \text{ Vp-p}$, $I_F = 12 \text{ mA}$, $V_O(\text{max}) = 0.4 \text{ V}$, $T_a = 25^\circ\text{C}$		-10000	—	—	V/ μs

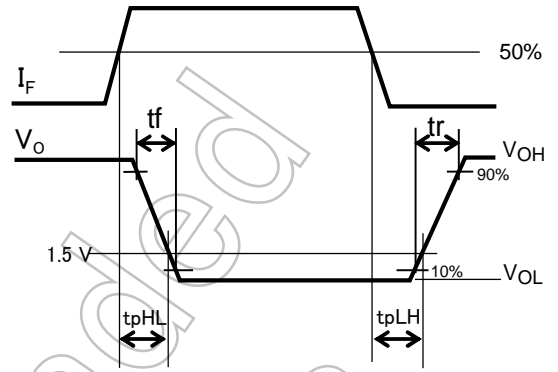
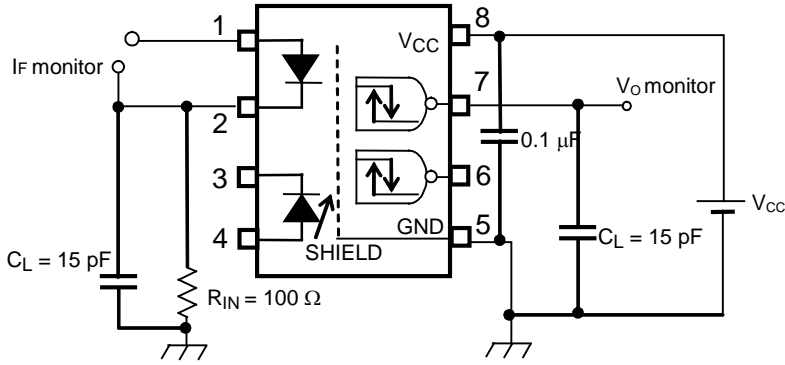
*All typical values are at $T_a = 25^\circ\text{C}$

Note 5: C_L is approximately 15 pF which includes probe and Jig/stray wiring capacitance.

Not Recommended for New Design

Test Circuit 1: Switching Time Test Circuit

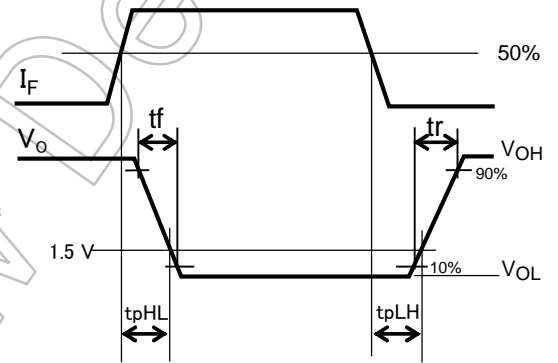
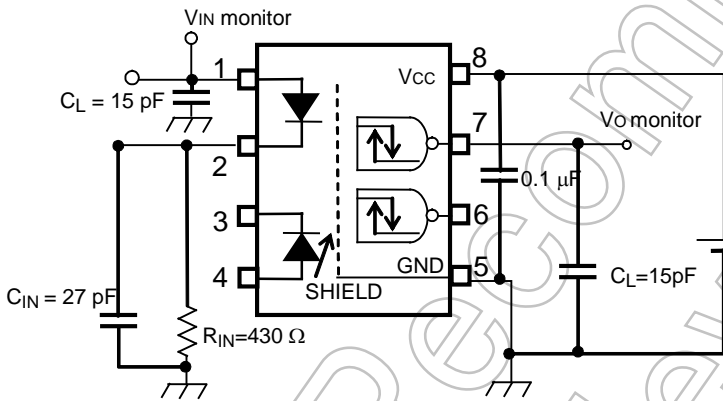
$I_F=12\text{ mA (P.G)}$
 $(f=5\text{ MHz, duty}=50\%,$
 less than $t_r = t_f = 5\text{ ns})$



C_L is capacitance of the probe and JIG.
 (P.G): Pulse Generator

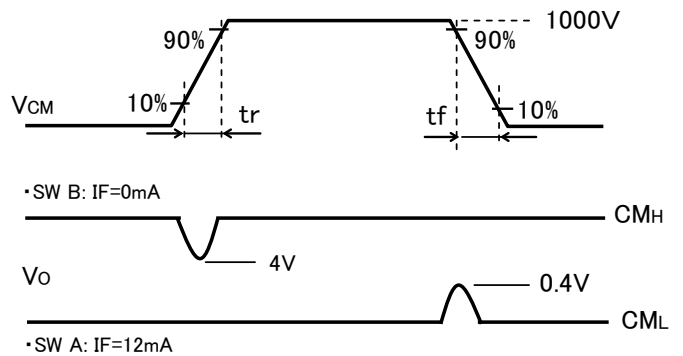
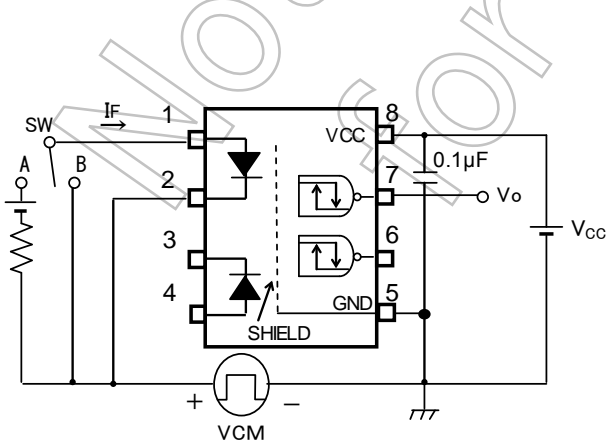
Test Circuit 2: Switching Time Test Circuit

$V_{IN}=5V\text{ (P.G)}$
 $(f=5\text{ MHz, duty}=50\%,$
 less than $t_r = t_f = 5\text{ ns})$



C_L is capacitance of the probe and JIG.
 (P.G): Pulse Generator

Test Circuit 3: Common-Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{tr(\mu s)} \quad CM_L = -\frac{800(V)}{tf(\mu s)}$$

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