TOSHIBA Photocoupler IRED & Photo-IC

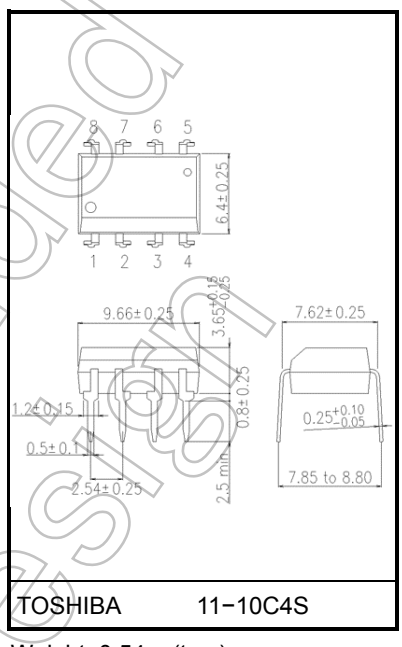
TLP2200

Isolated Bus Driver
High Speed Line Receiver
Microprocessor System Interfaces
MOS FET Gate Driver
Direct Replacement for HCPL−2200

The TOSHIBA TLP2200 consists of an infrared emitting diode and integrated high gain, high speed photodetector.
This unit is 8−lead DIP package.
The detector has a three state output stage that eliminates the need for pull−up resistor, and built−in Schmitt trigger. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1000V / μs.

- Input current: I_F = 1.6 mA
- Power supply voltage: V_{CC} = 4.5 to 20 V
- Switching speed: 2.5MBd guaranteed
- Common mode transient immunity: ±1000V / μs (min)
- Guaranteed performance over temperature: 0 to 85°C
- Isolation voltage: 2500 Vrms (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
  File No.E67349

Unit: mm



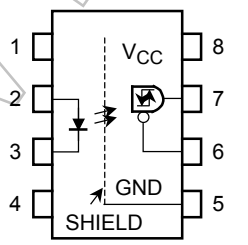
TOSHIBA 11−10C4S

Weight: 0.54 g (typ.)

Truth Table (positive logic)

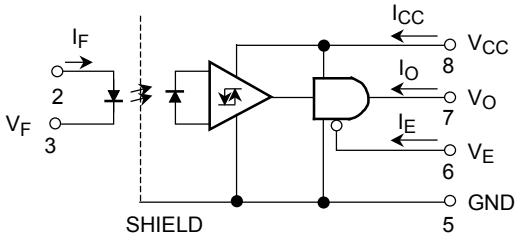
Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

Pin Configuration (top view)



1: N.C.
2: Anode
3: Cathode
4: N.C.
5: GND
6: V_E (enable)
7: V_O (output)
8: V_{CC}

Schematic



Start of commercial production
1986-07

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current, on	$I_{F(ON)}$	1.6	—	5	mA
Input current, off	$I_{F(OFF)}$	0	—	0.1	mA
Supply voltage	V_{CC}	4.5	—	20	V
Enable voltage high	V_{EH}	2.0	—	20	V
Enable voltage low	V_{EL}	0	—	0.8	V
Fan out (TTL load)	N	—	—	4	—
Operating temperature	T_{opr}	0	—	85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Absolute Maximum Ratings (no derating required up to 70°C)

Characteristic			Symbol	Rating	Unit
LED	Forward current		I_F	10	mA
	Peak transient forward current	(Note 1)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Input Power Dissipation		P_D	45	mW
	Input power dissipation derating (Ta ≥ 70°C)		$\Delta P_D/\Delta Ta$	-0.86	mW/°C
Detector	Output current		I_O	25	mA
	Supply voltage		V_{CC}	−0.5 to 20	V
	Output voltage		V_O	−0.5 to 20	V
	Three state enable voltage		V_E	−0.5 to 20	V
	Output Power Dissipation		P_O	100	mW
	Output Power Dissipation Derating (Ta ≥ 70°C)		ΔP_O /°C	-1.9	mW/°C
	Total package power dissipation	(Note 2)	P_T	210	mW
Operating temperature range			T_{opr}	−40 to 85	°C
Storage temperature range			T_{stg}	−55 to 125	°C
Lead solder temperature (10 s) (**)			T_{sol}	260	°C
Isolation voltage (AC 60 s, R.H. ≤ 60 %,Ta = 25°C)		(Note 3)	BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Pulse width 1 μs, 300 pps.

(Note 2) Derate 4.5 mW / °C above 70 °C ambient temperature.

(Note 3) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5,6,7 and 8 shorted together

(**) 1.6 mm below seating plane.

Electrical Characteristics (unless otherwise specified, Ta = 0 to 85 °C, V_{CC} = 4.5 to 20 V, $I_{F(ON)}$ = 1.6 to 5 mA, $I_{F(OFF)}$ = 0 to 0.1 mA, V_{EL} = 0 to 0.8 V, V_{EH} = 2.0 to 20 V)

Characteristic	Symbol	Test Condition		Min	Typ.*	Max	Unit
Output leakage current (V_O > V_{CC})	I_{OHH}	I_F = 5 mA, V_{CC} = 4.5 V	V_O = 5.5 V	—	—	100	μA
			V_O = 20 V	—	2	500	
Logic low output voltage	V_{OL}	I_{OL} = 6.4 mA (4 TTL load)		—	0.32	0.5	V
Logic high output voltage	V_{OH}	I_{OH} = −2.6 mA		2.4	3.4	—	V
Logic low enable current	I_{EL}	V_E = 0.4 V		—	−0.13	−0.32	mA
Logic high enable current	I_{EH}	V_E = 2.7 V		—	—	20	μA
		V_E = 5.5 V		—	—	100	
		V_E = 20 V		—	0.01	250	
Logic low enable voltage	V_{EL}	—		—	—	0.8	V
Logic high enable voltage	V_{EH}	—		2.0	—	—	V
Logic low supply current	I_{CCL}	I_F = 0 mA, V_E = don't care	V_{CC} = 5.5 V	—	5	6.0	mA
			V_{CC} = 20 V	—	5.6	7.5	
Logic high supply current	I_{CCH}	I_F = 5 mA, V_E = don't care	V_{CC} = 5.5 V	—	2.5	4.5	mA
			V_{CC} = 20 V	—	2.8	6.0	
High impedance state output current	I_{OZL}	I_F = 5 mA, V_E = 2 V	V_O = 0.4 V	—	1	−20	μA
	I_{OZH}	I_F = 0 mA, V_E = 2 V	V_O = 2.4 V	—	—	20	
			V_O = 5.5 V	—	—	100	
			V_O = 20 V	—	0.01	500	
Logic low short circuit output current (Note 4)	I_{OSL}	I_F = 0 mA	V_O = V_{CC} = 5.5 V	25	55	—	mA
			V_O = V_{CC} = 20 V	40	80	—	
Logic high short circuit output current (Note 4)	I_{OSH}	I_F = 5 mA, V_O = GND	V_{CC} = 5.5 V	−10	−25	—	mA
			V_{CC} = 20 V	−25	−60	—	
Input current hysteresis	I_{HYS}	V_{CC} = 5 V		—	0.05	—	mA
Input forward voltage	V_F	I_F = 5 mA, Ta = 25 °C		—	1.55	1.7	V
Temperature coefficient of forward voltage	ΔV_F / ΔTa	I_F = 5 mA		—	−2.0	—	mV / °C
Input reverse breakdown voltage	BV_R	I_R = 10 μA, Ta = 25 °C		5	—	—	V
Input capacitance	C_{IN}	V_F = 0 V, f = 1 MHz, Ta = 25 °C		—	45	—	pF
Resistance (input−output)	R_{I-O}	V_{I-O} = 500 V R.H. ≤ 60 % (Note 3)		5×10^{10}	10^{14}	—	Ω
Capacitance (input−output)	C_{I-O}	V_{I-O} = 0 V, f = 1 MHz (Note 3)		—	0.6	—	pF

(**) All typ. values are at Ta = 25 °C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

Switching Characteristics

(unless otherwise specified, Ta = 0 to 85 °C, V_{CC} = 4.5 to 20 V, $I_{F(ON)}$ = 1.6 to 5 mA, $I_{F(OFF)}$ = 0 to 0.1 mA)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to logic high output level (Note 5)	t_{pLH}	1	Without peaking capacitor C_1	—	235	—	ns
			With peaking capacitor C_1	—	—	400	
Propagation delay time to logic low output level (Note 5)	t_{pHL}		Without peaking capacitor C_1	—	250	—	ns
			With peaking capacitor C_1	—	—	400	
Output rise time (10−90%)	t_r		—	—	35	—	ns
Output fall time (90−10%)	t_f			—	20	—	ns
Common mode transient immunity at logic high output (Note 6)	CM_H	3	I_F = 1.6 mA, V_{CM} = 50 V, Ta = 25 °C	−1000	—	—	V / μs
Common mode transient immunity at logic low output (Note 6)	CM_L		I_F = 0 mA, V_{CM} = 50 V, Ta = 25 °C	1000	—	—	V / μs

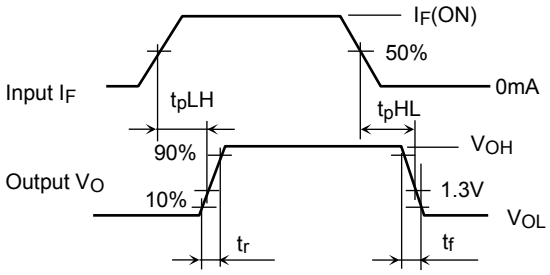
(*) All typ. values are at Ta = 25 °C, V_{CC} = 5 V, $I_{F(ON)}$ = 3 mA unless otherwise specified.

(Note 4) Duration of output short circuit time should not exceed 10ms.

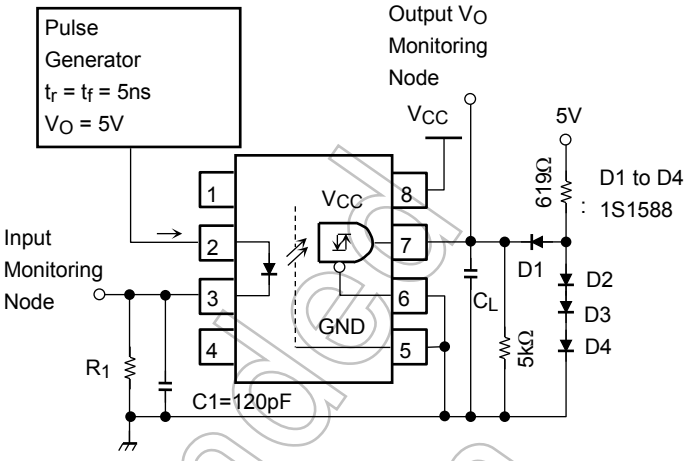
(Note 5) The t_{pLH} propagation delay is measured from the 50 % point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse.
The t_{pHL} propagation delay is measured from the 50 % point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.

(Note 6) CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V).
CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).

Test Circuit 1 t_{pHL}, t_{pLH}, t_r and t_f

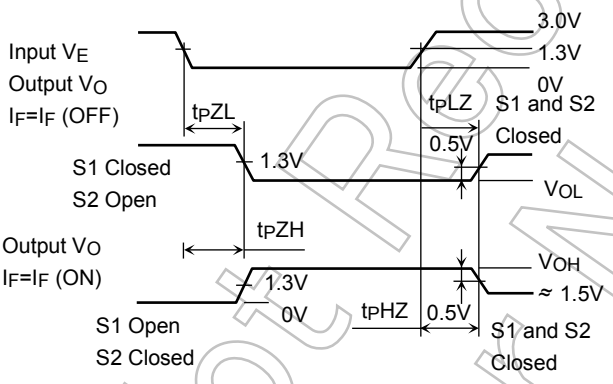


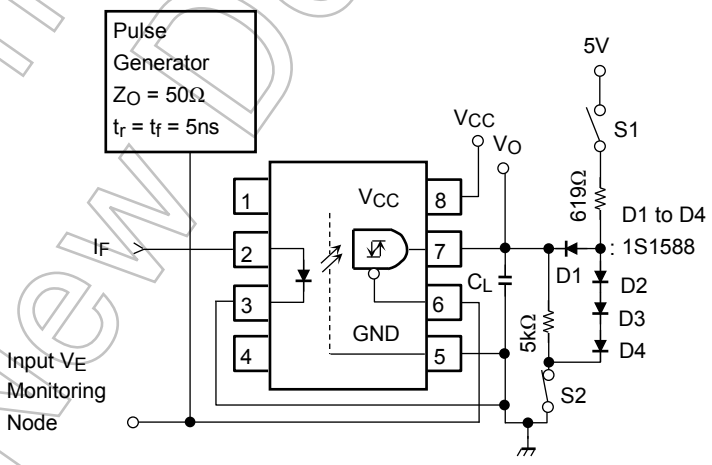
R_1	2.15kΩ	1.1kΩ	681Ω
$I_{F(ON)}$	1.6mA	3mA	5mA



C_1 is peaking capacitor. The probe and jig capacitances are included in C_1.
C_L is approximately 15pF which includes probe and stray wiring capacitance.

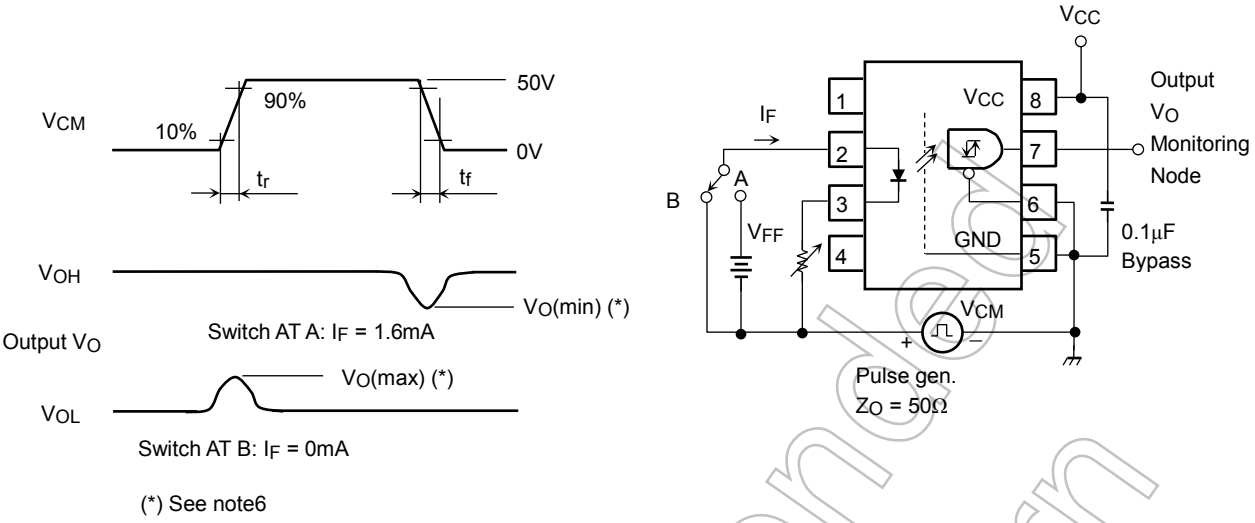
Test Circuit 2 t_{pHZ}, t_{pZH}, t_{pLZ} and t_{pZL}





C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 3 Common Mode Transient Immunity



(*) See note6

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