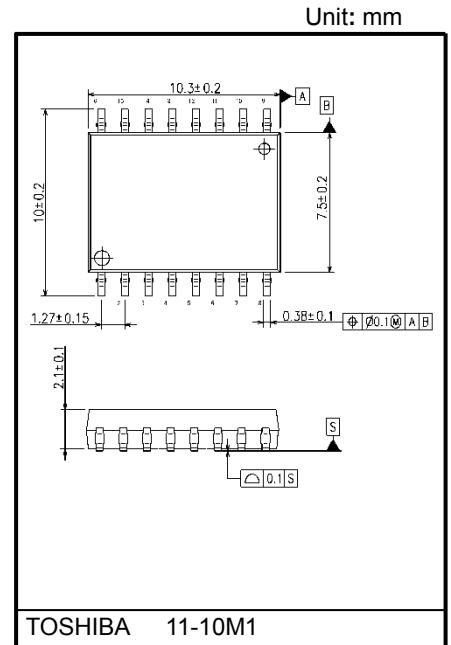


TLP5214

Isolated IGBT/Power MOSFET gate drive
 AC and brushless DC motor drives
 Industrial Inverters and Uninterruptible Power Supply (UPS)

The TLP5214 is a highly integrated 4.0A output current IGBT gate drive photo-coupler housed in a long creepage and clearance SO16L package.
 The TLP5214, a smart gate driver photocoupler, includes functions of IGBT desaturation detection, isolated fault status feedback, soft IGBT turn-off, active Miller clamping and under voltage lockout (UVLO).
 This photocoupler is suitable for driving IGBT and power MOSFET used in inverter applications.
 The TLP5214 consists two infrared LEDs and two high-gain and high-speed ICs. They realize high current, high-speed output control and output fault status feedback.

- Peak output current: ± 4.0 A (max)
- Guaranteed performance over temperature: -40°C to 110°C
- Supply current: 3.5 mA (max)
- Power supply voltage: 15 V to 30 V
- Threshold input current: $I_{FLH} = 6$ mA (max)
- Switching time (t_{PLH} / t_{PHL}) : 150 ns (max)
- Common-mode transient immunity: ± 35 kV/ μs (min)
- Isolation voltage: 5000 Vrms (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved : EN 60747-5-5, EN 62368-1 (Note 1)
- CQC-approved: GB4943.1, GB8898 Japan Factory



- Construction mechanical rating

	SO16L
Height	2.3 mm (max)
Creepage Distance	8.0 mm (min)
Clearance	8.0 mm (min)
Insulation Thickness	0.4 mm (min)

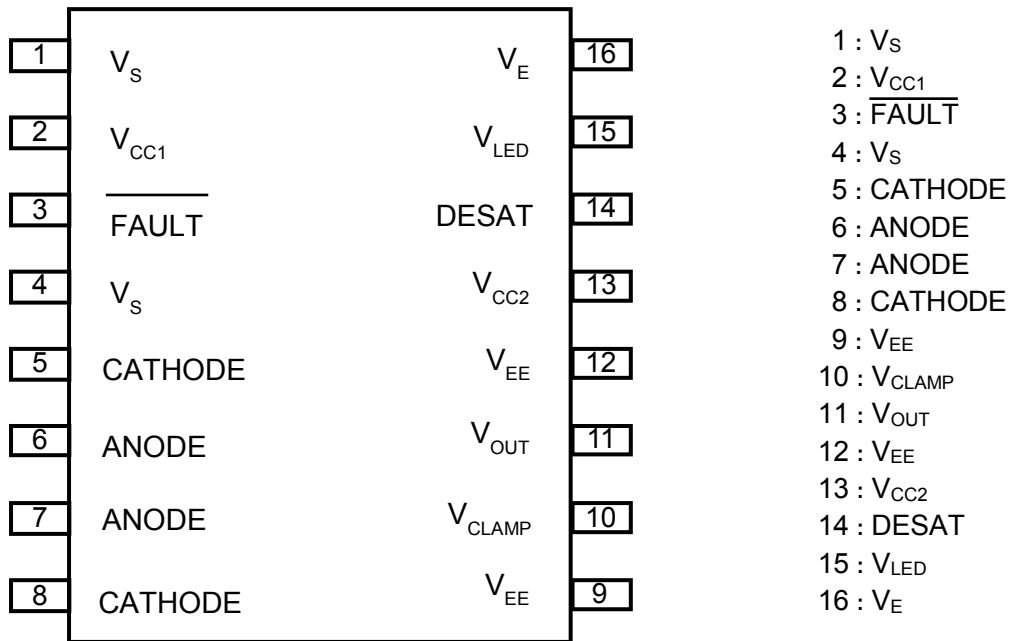
Note 1 : When a VDE approved type is needed, please designate the **Option(D4)**.

Truth Table

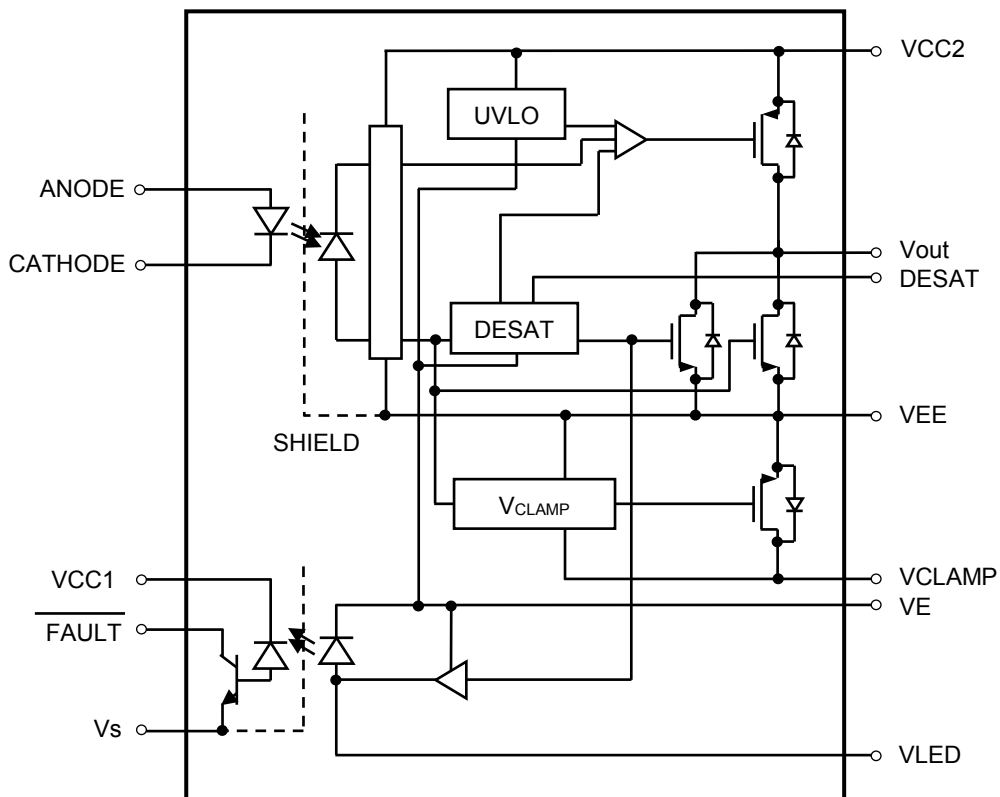
I_F	UVLO ($V_{CC2}-V_E$)	DESAT (14Pin DESAT Terminal Input)	FAULT (3Pin FAULT Terminal Output)	V_O
OFF	Not Active ($> V_{UVLO}^+$)	Not Active	High	Low
ON	Not Active ($> V_{UVLO}^+$)	Low ($< V_{DESATth}$)	High	High
ON	Not Active ($> V_{UVLO}^+$)	High ($> V_{DESATth}$)	Low (FAULT)	Low
ON	Active ($< V_{UVLO}^-$)	Not Active	High	Low
OFF	Active ($< V_{UVLO}^-$)	Not Active	High	Low

Start of commercial production
 2014-05

Pin Configuration (top view)



Internal Circuit



Note: A 1- μ F bypass capacitor must be connected between pins 9 and 13, pins 13 and 16.

Absolute Maximum Ratings (Note) (Ta = 25°C ,Unless otherwise specified)

	Characteristics	Symbol	Rating	Unit	
LED (Note 1)	Input forward current	I_F	25	mA	
	Input forward current derating (Ta ≥ 95°C)	$\Delta I_F / \Delta T_a$	-1	mA/°C	
	Peak transient input forward current (Note 1)	I_{FPT}	1	A	
	Peak transient input forward current derating (Ta ≥ 95°C)	$\Delta I_{FPT} / \Delta T_a$	-25	mA/°C	
	Reverse Input Voltage	V_R	6	V	
	Input power dissipation	P_D	145	mW	
	Input power dissipation derating (Ta ≥ 95°C)	$\Delta P_D / \Delta T_a$	-5.0	mW/°C	
Detector	Positive Input Supply Voltage	V_{CC1}	-0.5 to 7	V	
	"H" peak output current	$T_a = -40 \text{ to } 110 \text{ } ^\circ\text{C}$ (Note 2)	I_{OPH}	-4.0	A
	"L" peak output current		I_{OPL}	+4.0	A
	FAULT Output Current	$I_{\overline{FAULT}}$	8	mA	
	FAULT Pin Voltage	$V_{\overline{FAULT}}$	-0.5 to V_{CC1}	V	
	Total Output Supply Voltage	$(V_{CC2} - V_{EE})$	-0.5 to 35	V	
	Negative Output Supply Voltage	$(V_E - V_{EE})$	-0.5 to 15	V	
	Positive Output Supply Voltage	$(V_{CC2} - V_E)$	-0.5 to 35 - $(V_E - V_{EE})$	V	
	Output voltage	V_O	-0.5 to V_{CC2}	V	
	Peak Clamping Sinking Current	I_{Clamp}	1.7	A	
	Miller Clamping Pin Voltage	V_{Clamp}	-0.5 to V_{CC2}	V	
	DESAT Voltage	V_{DESAT}	V_E to $V_E + 10$	V	
	Output power dissipation	P_O	410	mW	
	Output power dissipation (Ta ≥ 95°C)	$\Delta P_O / \Delta T_a$	-14.0	mW/°C	
	Common	Operating temperature range	T_{opr}	-40 to 110	°C
Storage temperature range		T_{stg}	-55 to 125	°C	
Lead soldering temperature (10 s) (Note 3)		T_{sol}	260	°C	
Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 4)		BV_S	5000	Vrms	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: A ceramic capacitor (1 μF) should be connected between pins 9 and 13, pins 13 and 16 to stabilize the operation of the high gain linear amplifier. Furthermore, in case $V_E - V_{EE} > 0$ V, a bypass capacitor, which has good high frequency characteristic, a ceramic capacitor (1 μF) should be connected between pins 9 and 16. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: Pulse width $P_W \leq 1 \mu\text{s}$, 300 pps

Note 2: Exponential waveform pulse width $P_W \leq 0.2 \mu\text{s}$, $f \leq 15 \text{ kHz}$, $V_{CC} = 15 \text{ V}$

Note 3: For the effective lead soldering area.

Note 4: This device considered a two-terminal device: All pins on the LED side are shorted together, and all pin on the photodetector side are shorted together.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Min	Typ.	Max	Unit
Total Output Supply Voltage (Note 5)	$(V_{CC2}-V_{EE})$	15	-	30	V
Negative Output Supply Voltage	(V_E-V_{EE})	0	-	15	V
Positive Output Supply Voltage	$(V_{CC2}-V_E)$	15	-	$30 - (V_E-V_{EE})$	V
Input On-State Current (Note 6)	$I_{F(ON)}$	7.5	-	12	mA
Input Off-State Voltage	$V_{F(OFF)}$	0	-	0.8	V
Operating frequency (Note 7)	f	-	-	50	kHz

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 5: If the Vcc rise slope is sharp, an internal circuit might not operate with stability. Please design the VCC rise slope under $3.0 \text{ V} / \mu\text{s}$.

Note 6: Input signal rise time (fall time) $\leq 0.5 \mu\text{s}$.

Note 7: Exponential waveform. $I_{OPH} \geq -4.0 \text{ A}$ ($\leq 90 \text{ ns}$), $I_{OPL} \leq 4.0 \text{ A}$ ($\leq 90 \text{ ns}$), $T_a = 110^\circ\text{C}$

Electrical Characteristics (Note) ($T_a = -40$ to 110°C , unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit
Input Forward Voltage	V_F	—	$I_F = 10 \text{ mA}$, $T_a = 25^\circ\text{C}$	1.4	-	1.7	V
Input Reverse Current	I_R	—	$V_R = 5 \text{ V}$	-	-	10	μA
Input Capacitance	C_t	—	$V = 0 \text{ V}$, $f = 1 \text{ MHz}$, $T_a = 25^\circ\text{C}$	-	95	-	pF
FAULT Low Level Output Voltage	V_{FAULTL}	—	$I_{FAULT} = 1.1 \text{ mA}$, $V_{CC1} = 5.5 \text{ V}$	-	0.2	0.4	V
			$I_{FAULT} = 1.1 \text{ mA}$, $V_{CC1} = 3.3 \text{ V}$	-	0.2	0.4	
FAULT High Level Output Current	I_{FAULTH}	—	$V_{FAULT} = 5.5 \text{ V}$, $V_{CC1} = 5.5 \text{ V}$, $T_a = 25^\circ\text{C}$	-	-	0.5	μA
			$V_{FAULT} = 5.5 \text{ V}$, $V_{CC1} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$	-	-	0.3	
High Level Output Current (Note 8)	I_{OPH}	1	$V_O = V_{CC2} - 4 \text{ V}$	-	-4.0	-1.2	A
			$V_O = V_{CC2} - 7 \text{ V}$	-	-6.5	-3.0	
Low Level Output Current (Note 8)	I_{OPL}	2	$V_O = V_{EE} + 2.5 \text{ V}$	1.2	3.5	-	
			$V_O = V_{EE} + 7 \text{ V}$	3	5.5	-	
Low Level Output Current During Fault Condition	I_{OLF}	—	$V_O - V_{EE} = 14 \text{ V}$	90	150	230	mA
High Level Output Voltage	V_{OH}	3	$I_O = -100 \text{ mA}$	$V_{CC2}-0.3$	$V_{CC2}-0.2$	-	V
Low Level Output Voltage	V_{OL}	4	$I_O = 100 \text{ mA}$	-	0.1	0.2	
Clamp Pin Threshold Voltage	V_{tClamp}	—	—	-	3.0	-	
Clamp Low Level Sinking Current	I_{CL}	—	$V_O = V_{EE} + 2.5 \text{ V}$	0.56	1.8	-	A
High Level Supply Current	I_{CC2H}	5	$I_O = 0 \text{ mA}$	-	2.4	3.5	mA
Low Level Supply Current	I_{CC2L}	6	$I_O = 0 \text{ mA}$	-	2.3	3.5	
Blanking Capacitor Charging Current	I_{CHG}	7	$V_{DESAT} = 2 \text{ V}$	-0.13	-0.24	-0.33	
Blanking Capacitor Discharge Current	I_{DSCHG}	8	$V_{DESAT} = 7 \text{ V}$	10	49	-	
DESAT Threshold Voltage	V_{DESAT}	—	$V_{CC2}-V_E > V_{UVLO-}$	6	6.5	7.5	V
UVLO Threshold Voltage	V_{UVLO+}	9	$V_O > 5 \text{ V}$	10.5	11.6	13.5	
	V_{UVLO-}	9	$V_O < 5 \text{ V}$	9.2	10.3	11.1	
UVLO hysteresis	$UVLO_{HYS}$	—	—	-	1.3	-	

(*): All typical values are at $T_a = 25^\circ\text{C}$

Note 8: I_O application time $\leq 50 \mu\text{s}$, 1 pulse

Electrical Characteristics (Note) (Ta = -40 to 110 °C, unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit
Threshold Input Current(L/H)	I _{FLH}	10	V _{CC} = 30 V, V _O < 5 V	-	2.3	6	mA
Threshold Input Voltage (H/L)	V _{FHL}	—	V _{CC} = 30 V, V _O > 5 V	0.8	-	-	V

(*): All typical values are at Ta = 25°C

Note: This product is more sensitive than conventional products to electrostatic discharge (ESD) owing to its low power consumption design.
It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

Isolation Characteristics (Note) (Ta = 25 °C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C _S	V _S = 0 V, f = 1 MHz	-	1.0	-	pF
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 V	10 ¹²	10 ¹⁴	-	Ω
Isolation voltage	BV _S	AC, 60 s	5000	-	-	V _{rms}

Note: This device considered a two-terminal device: All pins on the LED side are shorted together, and all pin on the photodetector side are shorted together.

Switching Characteristics (Note) (Ta = -40 to 110 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit		
Propagation delay time (Note 9)	L → H	t _{pLH}	11	V _{CC2} = 30 V R _g = 10 Ω C _g = 25 nF Duty = 50%	I _F = 0 → 10 mA	50	85	150	ns	
	H → L	t _{pHL}			I _F = 10 → 0 mA	50	90	150		
Output rise time (10–90 %) (Note 9)		t _r			I _F = 0 → 10 mA	-	32	-		
Output fall time (90–10 %) (Note 9)		t _f			I _F = 10 → 0 mA	-	18	-		
Pulse with distortion (Note 9)		t _{pHL} - t _{pLH}			I _F = 0 ↔ 10 mA	-	-	50		
Propagation delay skew (device to device) (Note 9) (Note 10)		t _{psk}			I _F = 0 ↔ 10 mA	-80	-	80		
DESAT Sense to 90% Delay		t _{DESAT(90%)}	12	C _{DESAT} = 100 pF, R _g = 10 Ω C _g = 25 nF, V _{CC2} = 30 V R _F = 2.1 kΩ	-	180	500	μs		
DESAT Sense to 10% Delay		t _{DESAT(10%)}			-	3.5	5			
DESAT Sense to Low Level FAULT Signal Delay		t _{DESAT(FAULT)}			C _{DESAT} = 100 pF, R _g = 10 Ω C _g = 25 nF, V _{CC2} = 30 V R _F = 2.1 kΩ C _F = Open	-	300	500	ns	
DESAT Sense to Low Propagation Delay		t _{DESAT(LOW)}				-	200	-		
DESAT Input Mute		t _{DESAT(MUTE)}				7	14	-		μs
RESET to High Level FAULT Signal Delay		t _{RESET(FAULT)}				V _{CC1} = 5.5 V	0.2	0.45	2	
High-level common-mode Transient Immunity		CM _H			13 to 16	I _F = 10 mA V _O (min) = 26 V	±35	-	-	kV/μs
Low-level common-mode Transient Immunity		CM _L	I _F = 0 mA V _O (max) = 1 V	±35			-	-		

(*): All typical values are at Ta = 25 °C.

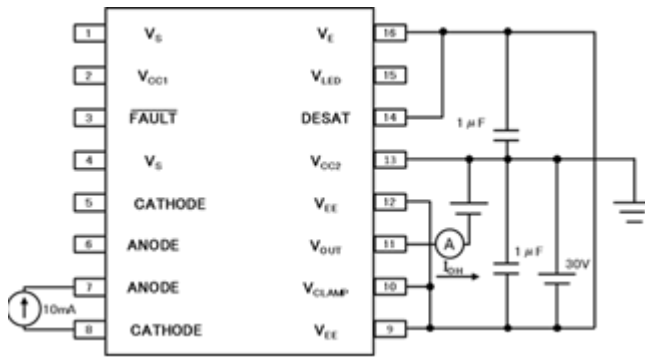
Note 9: Input signal (f = 10 kHz, duty = 50%, t_r = t_f = 5 ns or less)

CL is less than 15 pF which includes probe and stray wiring capacitance.

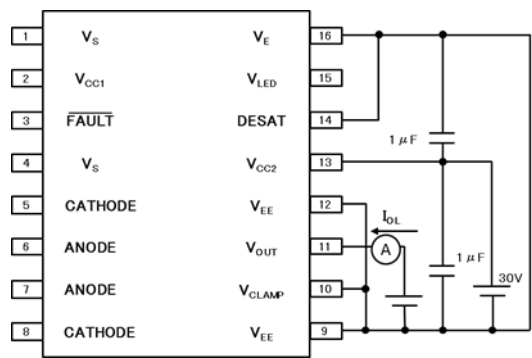
Note 10: The propagation delay skew, t_{psk}, is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

Test Circuit

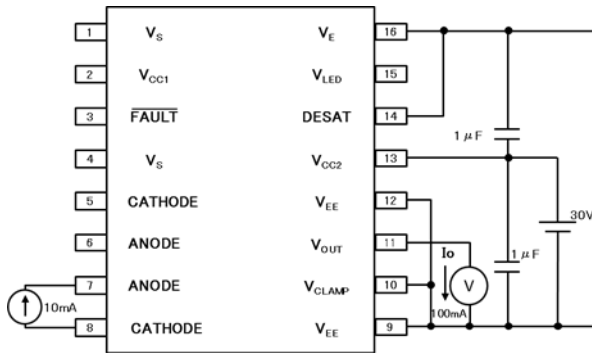
Test Circuit 1: IOPH



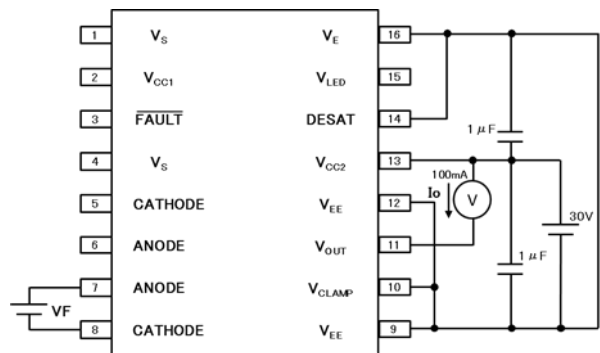
Test Circuit 2: IOPL



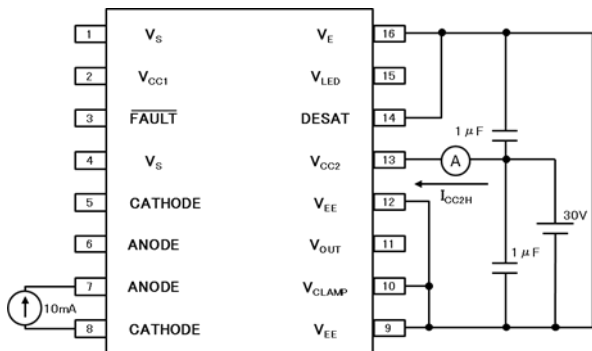
Test Circuit 3: VOH



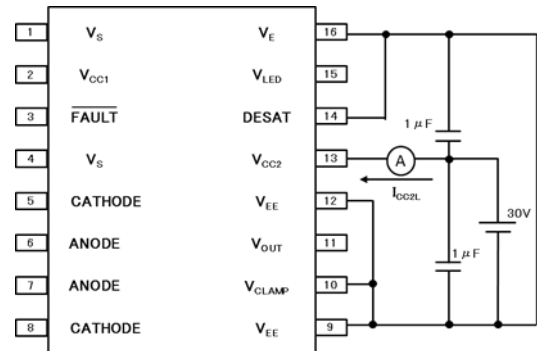
Test Circuit 4: VOL



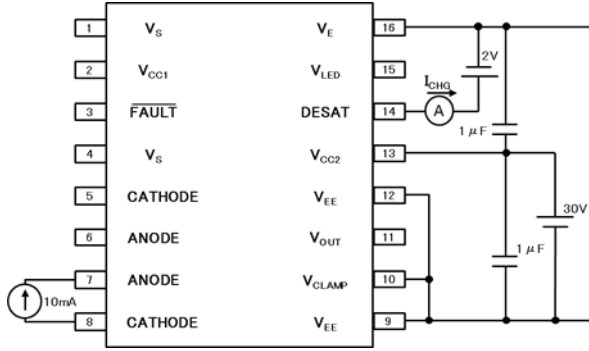
Test Circuit 5: ICC2H



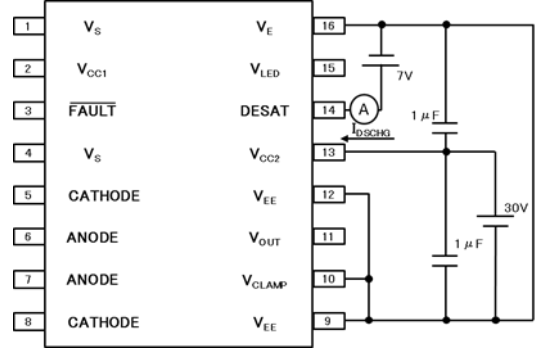
Test Circuit 6: ICC2L



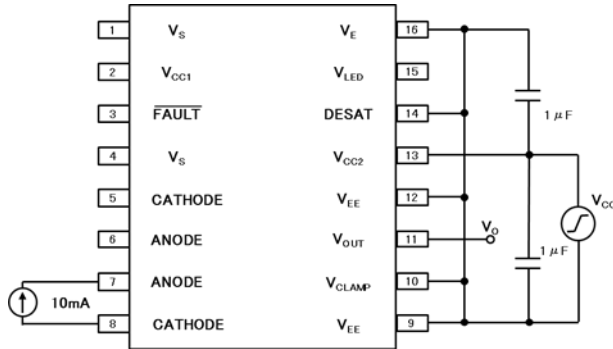
Test Circuit 7: I_{CHG}



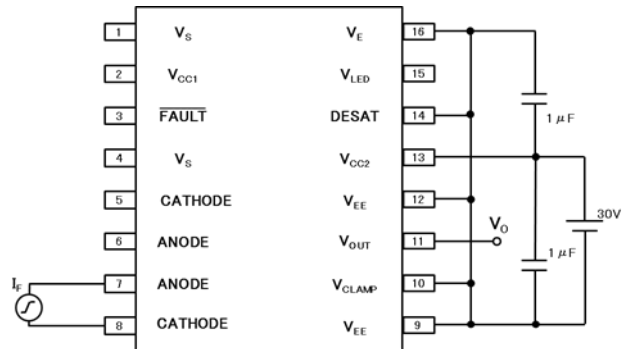
Test Circuit 8: I_{DSCHG}



Test Circuit 9: V_{UVLO}

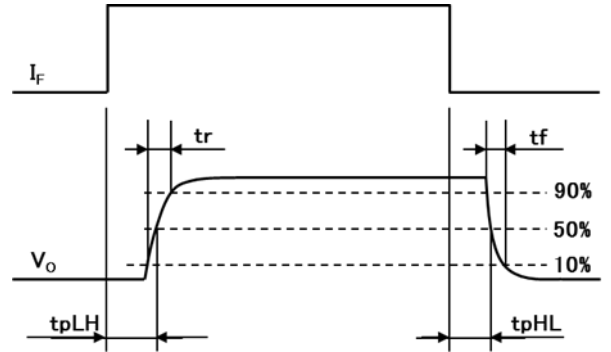
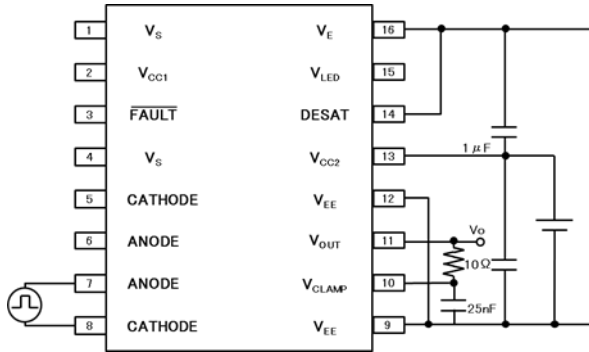


Test Circuit 10: I_{FLH}



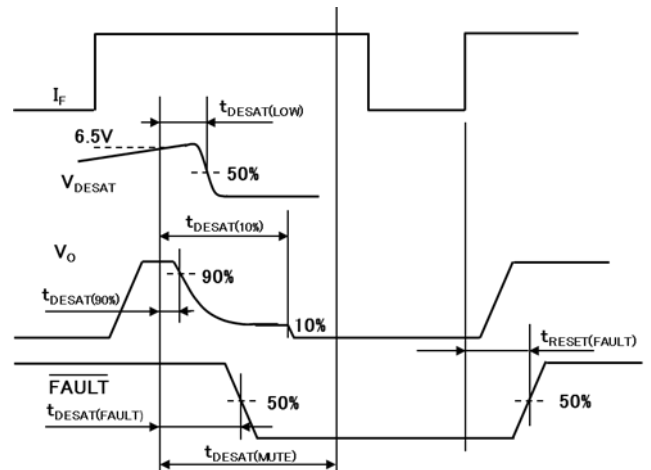
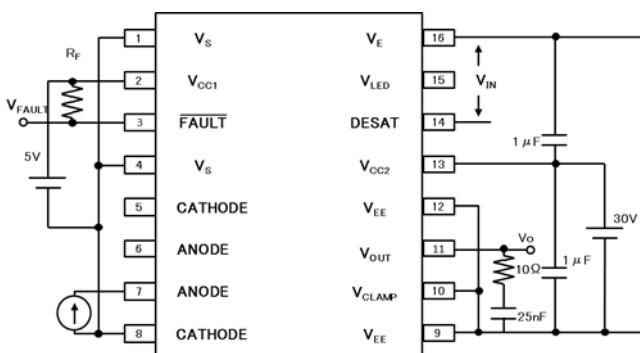
Test Circuit 11: t_{pLH}, t_{pHL}, t_r, t_f, | t_{pHL}-t_{pLH} |

I_F = 10 mA (P.G.)
 (f = 10 kHz, duty = 50%, rise / fall time 5 ns or less)

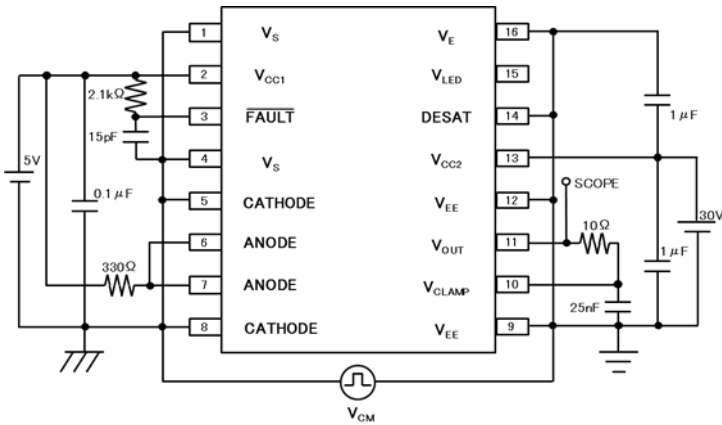


Test Circuit 12: t_{DESAT(90%)}, t_{DESAT(10%)}, t_{DESAT(FAULT)}, t_{DESAT(Low)}, t_{DESAT(MUTE)}, t_{RESET(FAULT)}

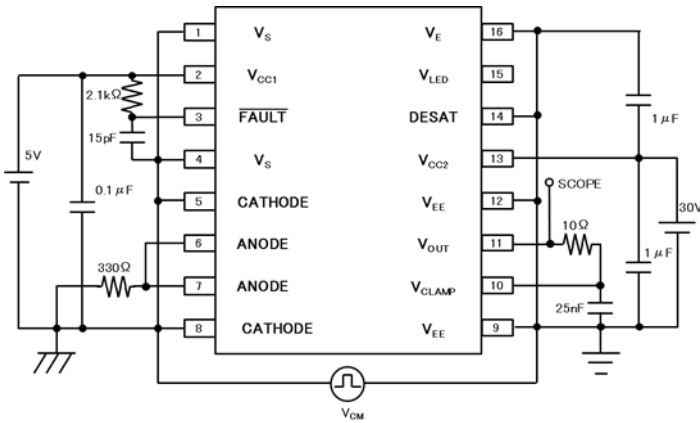
I_F = 10 mA (P.G.)
 (f = 10 kHz, duty = 50%, rise / fall time 5 ns or less)



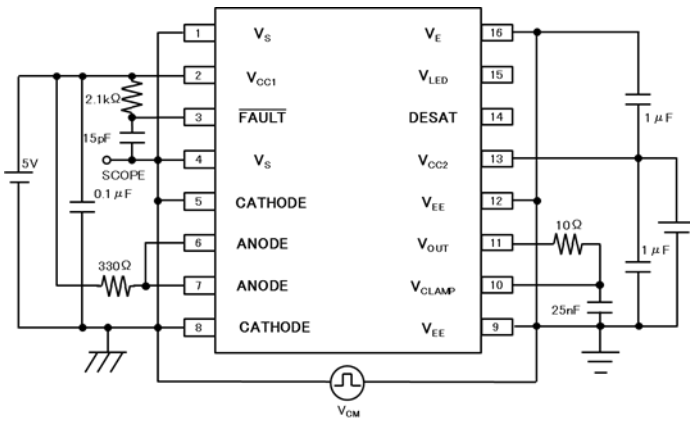
Test Circuit 13: CMR_LED1 ON



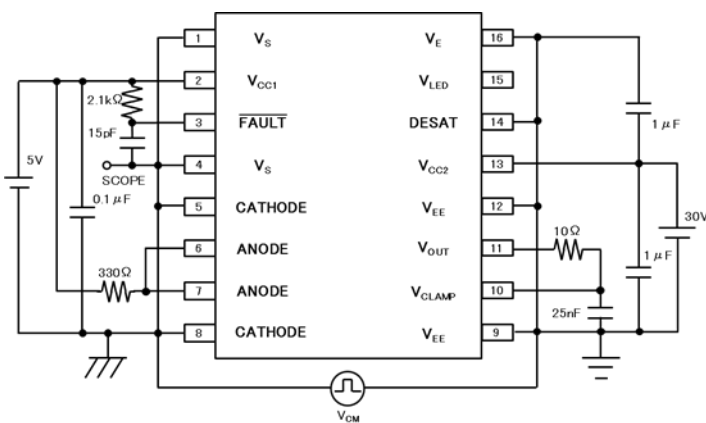
Test Circuit 14: CMR_LED1 OFF



Test Circuit 15: CMR_LED2 ON

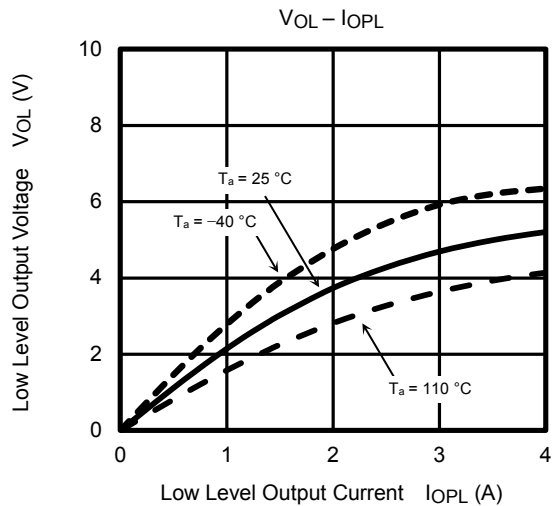
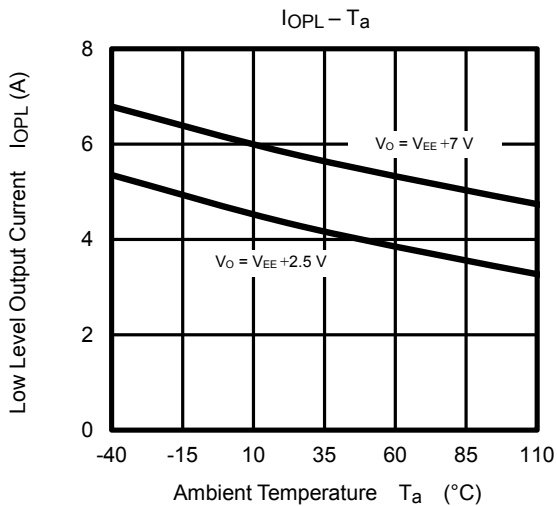
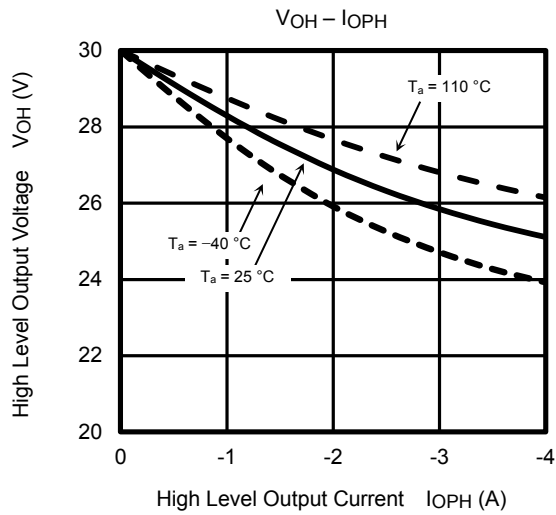
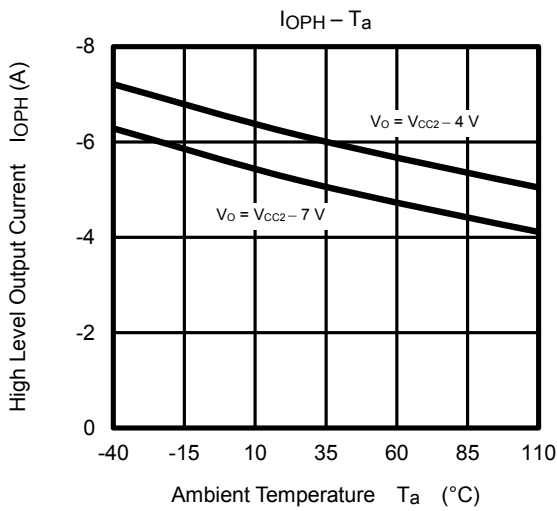
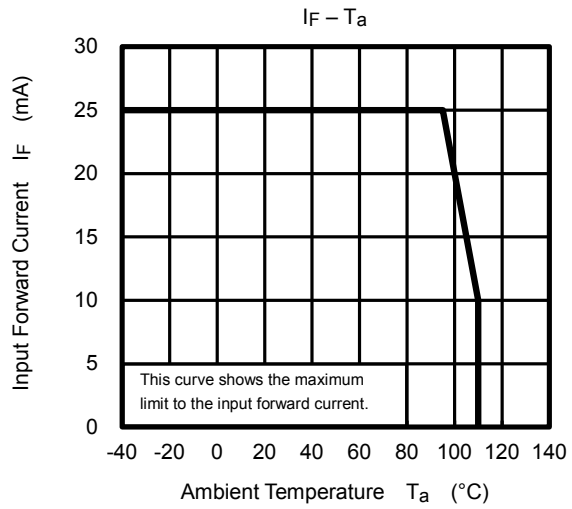
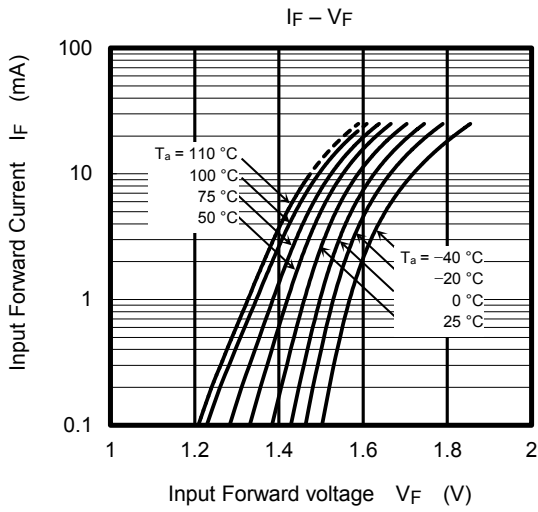


Test Circuit 16: CMR_LED2 OFF

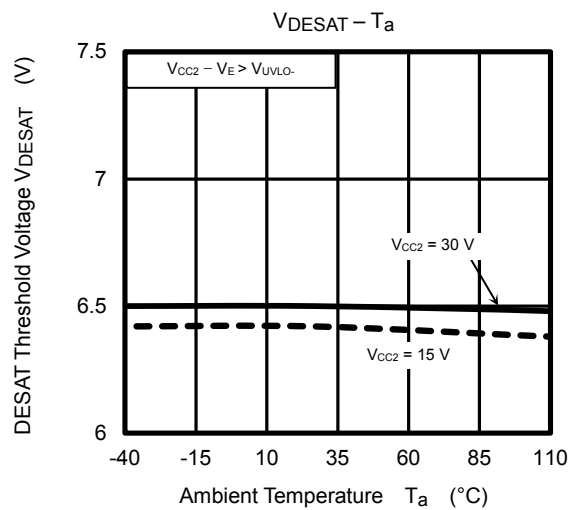
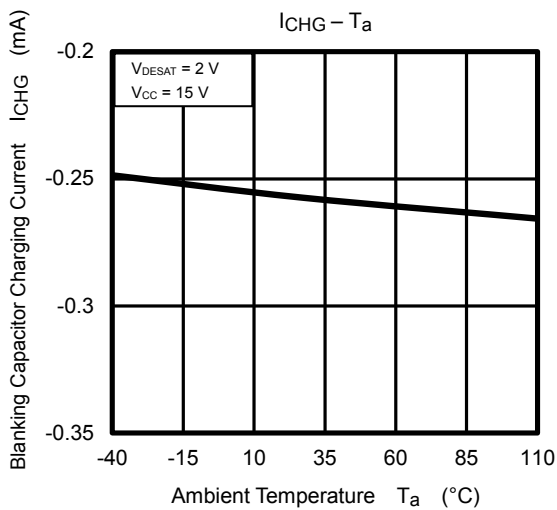
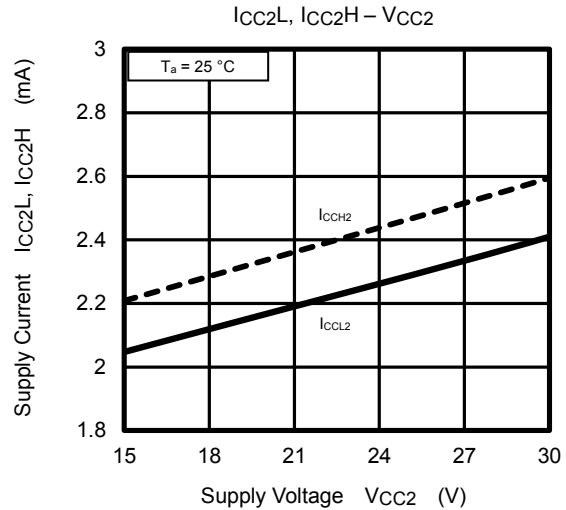
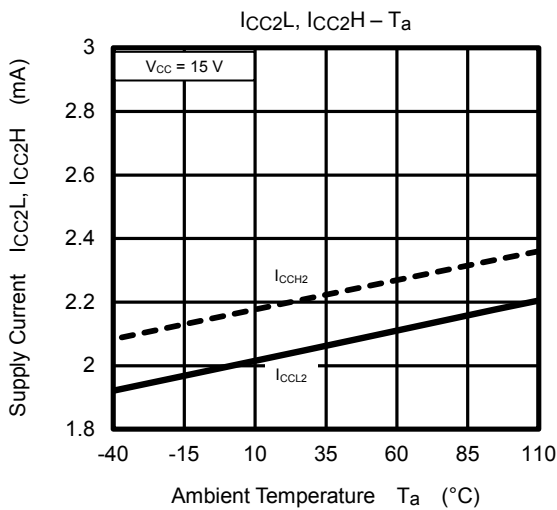
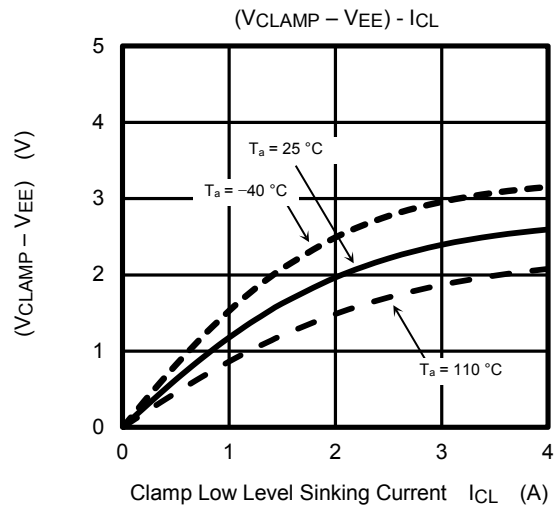
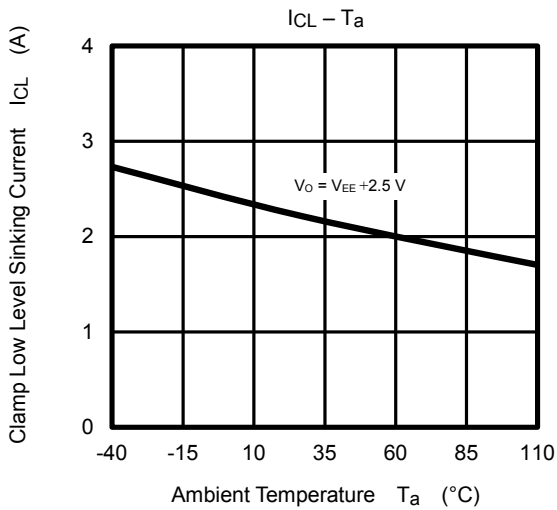


CML (CMH) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the LOW (HIGH) state.

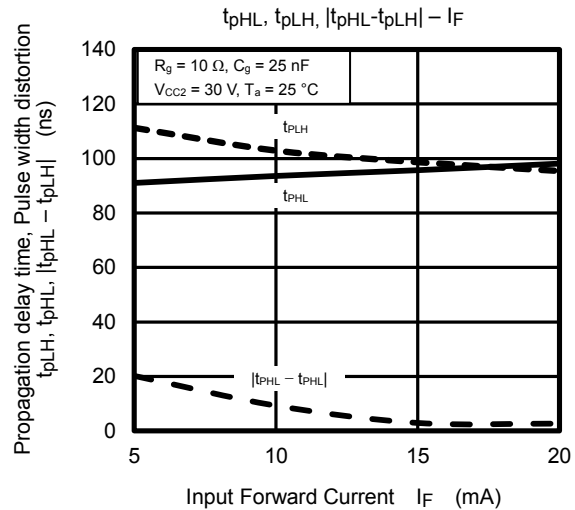
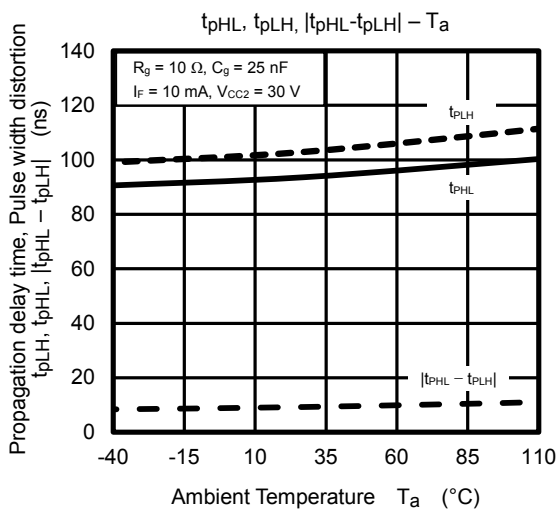
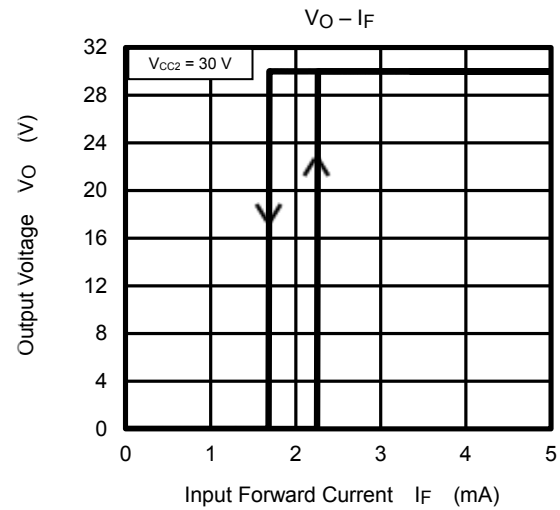
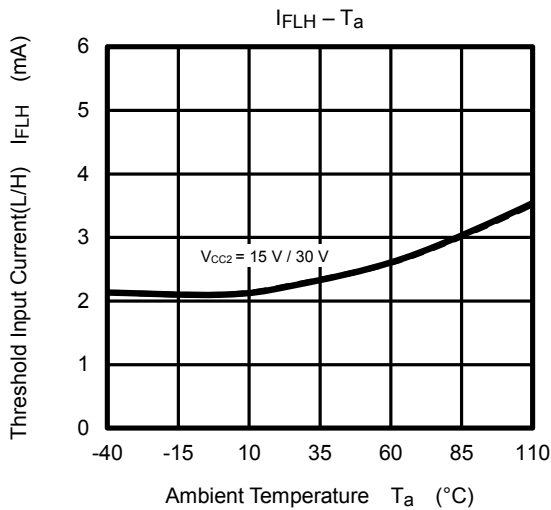
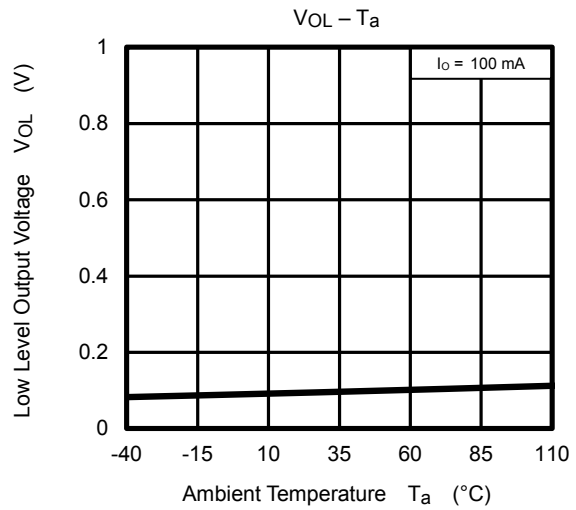
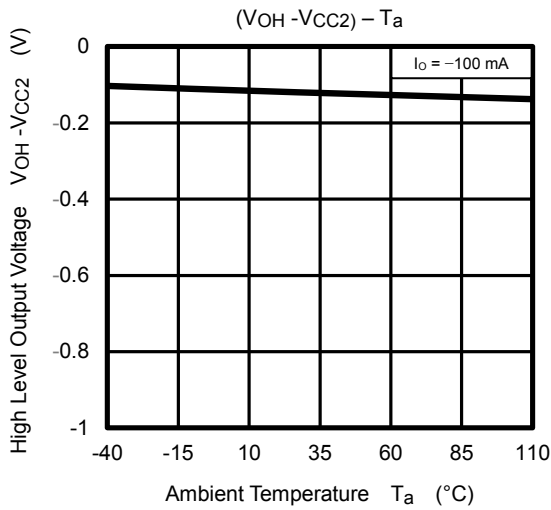
Characteristics Curve



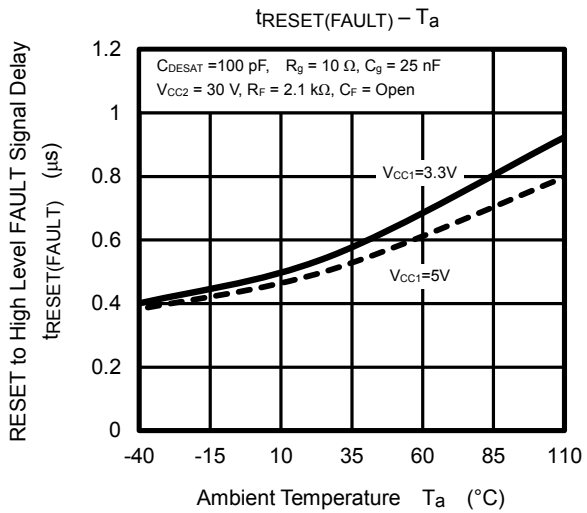
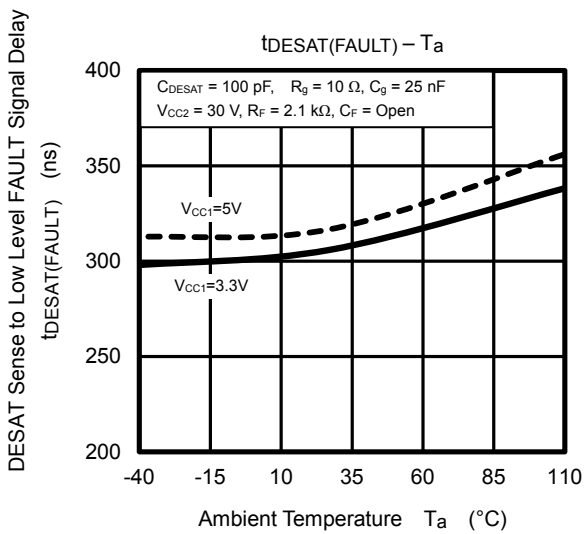
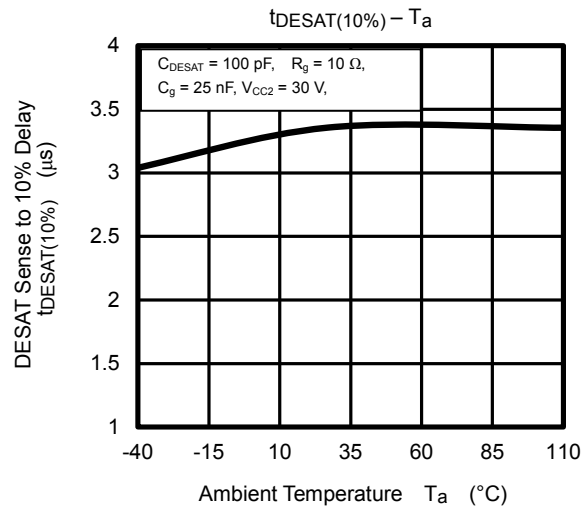
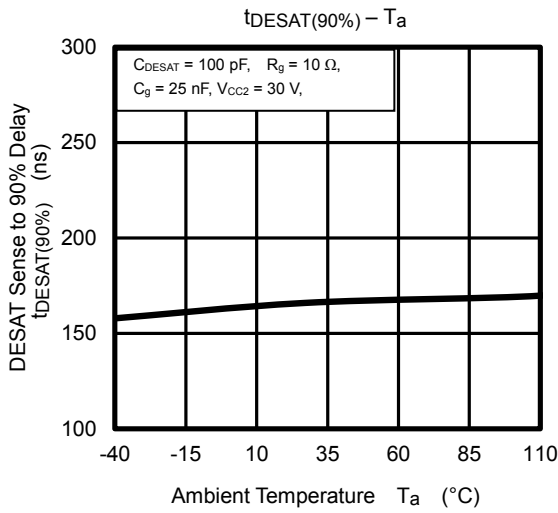
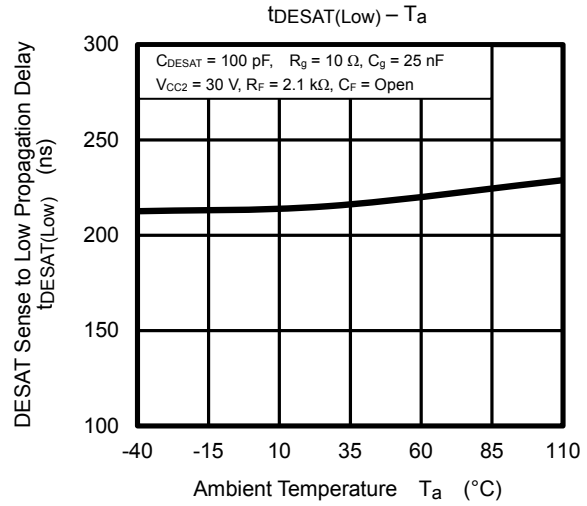
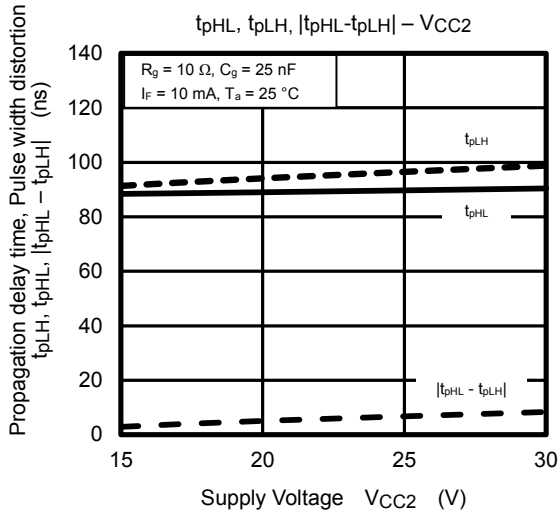
NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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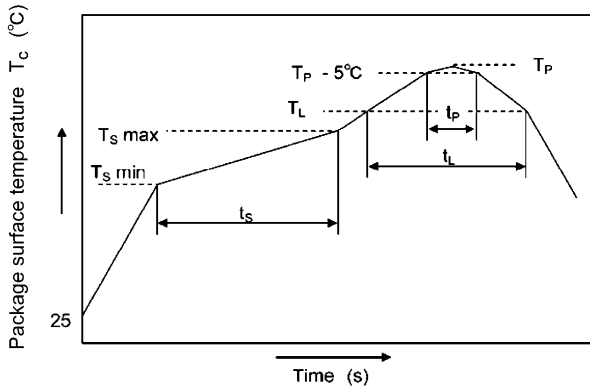
PRECAUTIONS OF SURFACE MOUNTING TYPE PHOTOCOUPLER SOLDERING & GENERAL STORAGE

(1) Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

1) When Using Soldering Reflow

An example of a temperature profile when lead(Pb)-free solder is use



	Symbol	Min	Max	Unit
Preheat temperature	T_S	150	200	°C
Preheat time	t_s	60	120	s
Ramp-up rate (T_L to T_P)			3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	150	s
Peak temperature	T_P		260	°C
Time during which T_c is between ($T_P - 5$) and T_P	t_p		30	s
Ramp-down rate (T_P to T_L)			6	°C/s

An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used

- Reflow soldering must be performed once or twice.
- The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

2) When using soldering Flow

- Apply preheating of 150 °C for 60 to 120 seconds.
- Mounting condition of 260 °C or less within 10 seconds is recommended.
- Flow soldering must be performed once

3) When using soldering Iron

- Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C.
- Heating by soldering iron must be only once per 1 lead

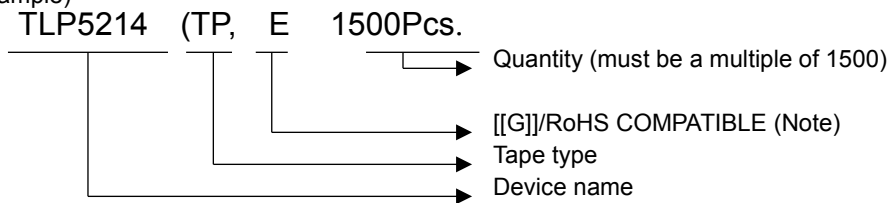
(2) Precautions for General Storage

- 1) Do not store devices at any place where they will be exposed to moisture or direct sunlight.
- 2) When transportation or storage of devices, follow the cautions indicated on the carton box.
- 3) The storage area temperature should be kept within a temperature range of 5 degree C to 35 degree C, and relative humidity should be maintained at between 45% and 75%.
- 4) Do not store devices in the presence of harmful (especially corrosive)gases, or in dusty conditions.
- 5) Use storage areas where there is minimal temperature fluctuation. Because rapid temperature changes can cause condensation to occur on stored devices, resulting in lead oxidation or corrosion, as a result, the solderability of the leads will be degraded.
- 6) When repacking devices, use anti-static containers.
- 7) Do not apply any external force or load directly to devices while they are in storage.
- 8) If devices have been stored for more than two years, even though the above conditions have been followed, it is recommended that solderability of them should be tested before they are used.

Ordering Method

When placing an order, please specify the product number, the CTR rank, the tape and the quantity as shown in the following example.

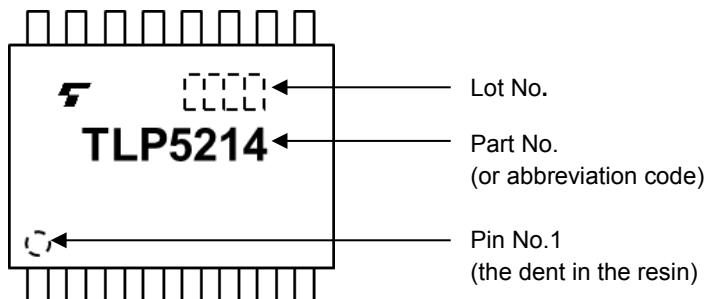
(Example)



Note : Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronics equipment.

Marking



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