Unit: mm

7.62 ± 0.25

0.25 +0.1

7.85~8.80

11-10C4

11-1004

TOSHIBA Photocoupler GaAłAs IRED & Photo IC

TLP552

Isolated Line Receiver Simplex/Multiplex Data Transmission Computer-Peripheral Interface Microprocessor System Interface Digital Isolation for A-D, D-A Conversion

The TOSHIBA TLP552 is a photocoupler which combines a GaAlAs IRED LED as the emitter and an integrated high gain, high speed photodetector. This unit is 8-lead DIP.

The output of the detector circuit is an open collector, schottky clamped transistor.

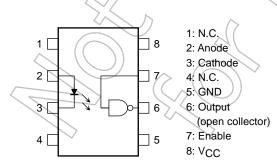
- TTL/LSTTL compatible: $V_{CC} = 5 V$
- Isolation voltage: 2500 V_{rms} (min)
- Switching speed: t_{pHL} , $t_{pLH} = 60$ ns (typ.) (@R_L = 350 Ω)
- Guaranteed performance over temp.: 0 to 70°C
- UL recognized: UL1577, file no. E67349

Truth Table (positive logic)

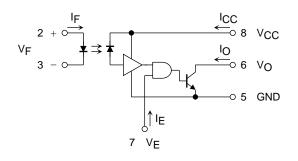
Input	Enable	Output
н	Н	
L	н	H
Н	L ((ЛУн
L		Н .

Note: A 0.1 µF bypass capacitor must be connected between pins 8 and 5 (see "Instruction for use" on page 3).

Pin Configurations (top view)



Schematic



2.54 ± 0.2

Weight: 0.54 g (typ.)

JEDEC

JEITA TOSHIBA

Note: A 0.1 μF bypass capacitor must be connected between pins 8 and 5 (see "Instruction for use" on page 3)

Start of commercial production 1982-08

Absolute Maximum Ratings (Ta = 25°C)

	Characteristics	Symbol	Rating	Unit	
	Forward current	١ _F	20	mA	
	Forward current derating (Ta ≥ 53°C)	∆ IF/∆ Ta	-0.28	mA/°C	
	Pulse forward current (Note 1)	I _{FP}	40	mA 🔇	
LED	Peak transient forward current (Note 2)	IFPT	0.5	А	
	Reverse voltage	V _R	5	V	$\sum r$
	Diode power dissipation	PD	40	mW	
	Input power dissipation derating(Ta ≥ 53°C)	∆PD/°C	-0.56	mW/°C))
	Output current	ΙO	50	mA	
	Output voltage	VO	7	V	
Detector	Supply voltage (Note 3)	VCC	7	<	
Dete	Enable input voltage (Note 4)	VE	5.5	v	
	Output collector power dissipation	PO	85	mW	5
	Output power dissipation derating (Ta \geq 53°C)	ΔPo/ ΔTa	4.2	mW/°C	
Ope	erating temperature range	Topr	0 to 70	°C	
Storage temperature range		T _{stg}	-55 to 125	°Q	$\overline{\mathbf{a}}$
Lead solder temperature (10 s) (Note 5)		Tsol	260	ç	9
Isol	ation voltage (AC, 1 minute, R.H. \leq 60%) (Note 6)	BVS	2500	Vrms	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- Note 1: 50% duty cycle, 1 ms pulse width.
- Note 2: Pulse width \leq 1µs, 300 pps.
- Note 3: 1 minute maximum.
- Note 4: Not to exceed VCC by more than 500 mV.
- Note 5: Soldering portion of lead: up to 2 mm from the body of the device.
- Note 6: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Recommended Operating Conditions

Characteristics	Symbol	Min	Тур.	Max	Unit
Input current, low level	FL	0	_	250	μΑ
Input current, high level	Ігн	7	_	20	mA
Supply voltage, output	Vcc	4.5	_	5.5	V
High level enable voltage	V _{EH}	2.0	_	Vcc	V
Low level enable voltage	V _{EL}	0	_	0.8	V
Fan out (TTL load)	Ν	_	_	8	_
Operating temperature	т _{орг}	0	_	70	°C

Note: The recommended operating conditions are given as a design guideline to obtain expected performance of the device. In addition, each item is an independent guideline. In developing designs using this product, please confirm the specified characteristics shown in this document.

Electrical Characteristics (unless otherwise specified, for $0^{\circ}C \le Ta \le 70^{\circ}C$)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input forward voltage	VF	$I_F = 10 \text{ mA}, \text{ Ta} = 25^{\circ}\text{C}$	_	1.65	1.8	V
Input diode temperature coefficient	∆V _F /∆Ta	I _F = 10 mA	_	-2.0		mV/°C
Input reverse current	IR	V _R = 5 V, Ta = 25°C	/	_	10	μA
Input capacitance	CT	V _F = 0 V, f = 1 MHz, Ta = 25°C	$\langle \rangle$	45		pF
High level output current	ЮН	$V_{CC} = 5.5 \text{ V}, V_O = 5.5 \text{ V}$ IF = 250 µA, VE = 2.0 V	\mathbb{Q}	710	250	μΑ
Low level output voltage	VOL	$V_{CC} = 5.5 \text{ V}, \text{ I}_{F} = 5 \text{ mA}$ $V_{EH} = 2.0 \text{ V}, \text{ I}_{OL} = 13 \text{ mA}$ (sinking)	\mathcal{D}	0.4	0.6	V
Input current logic low output level	IFH	$I_{OL} = 13 \text{ mA} (\text{sinking}),$ $V_{O} = 0.6 \text{ V}, V_{CC} = 5.5 \text{ V},$ $V_{EH} = 2.0 \text{ V}$	_		5	mA
High level enable current	IEH	$V_{CC} = 5.5 \text{ V}, \text{ V}_{E} = 2.0 \text{ V}$	- 2	-1.0	1	mA
Low level enable current	IEL	$V_{CC} = 5.5 \text{ V}, \text{ V}_{E} = 0.5 \text{ V}$	- (C)_1.6_	-2.0	mA
High level supply current	^I ССН	$V_{CC} = 5.5 \text{ V}, 1_{F} = 0 \text{ mA}, V_{E} = 0.5 \text{ V}$	R	40)	15	mA
Low level supply current	ICCL	$V_{CC} = 5.5 \text{ V}, I_{F} = 10 \text{ mA}, V_{E} = 0.5 \text{ V}$		12	18	mA
Current transfer ratio	CTR	I _F = 5.0 mA, R _L = 100 Ω V _{CC} = 5.0 V, Ta = 25°C	2)	1000	_	%
Resistance (input-output)	R _S	$V_{S} = 500 \text{ V, R.H.} \le 60\%, \text{ Ta} = 25^{\circ}\text{C}$	5 × 10 ¹⁰	10 ¹⁴	_	Ω
Capacitance (input-output)	C _S	V _S = 0 V, f = 1 MHz, Ta = 25°C	_	0.6	_	pF

Note: All typical values are at Ta=25°C

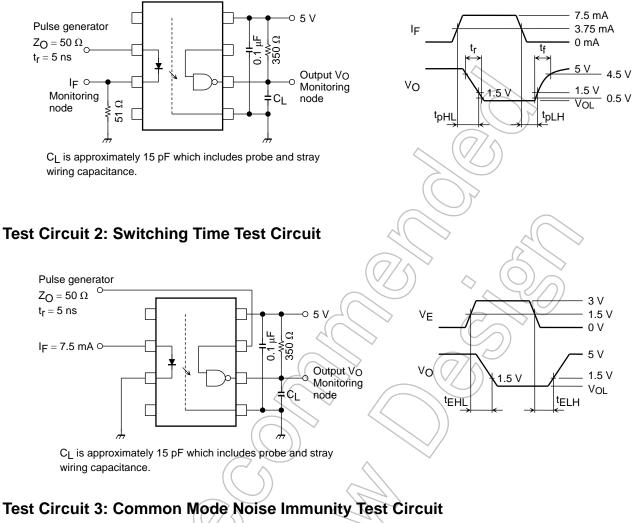
Switching Characteristics (Ta = 25°C, V_{CC} = 5 V)

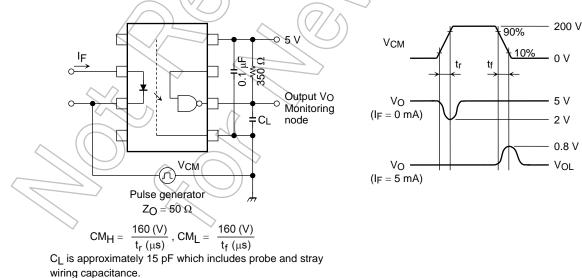
Characteristics	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
Propagation delay time to high output level (L \rightarrow H)	трін		RL = 350 Ω, CL = 15 pF /F = 7,5 mA	_	60	120	ns
Propagation delay time to low output level (H \rightarrow L)	tpHL	17	RL = 3 50 Ω, CL = 15 pF N _F = 7.5 mA	_	60	120	ns
Output rise fall time (10 to 90%)	t _r , t _f	$\left \begin{array}{c} \end{array} \right\rangle$	$R_L = 350 \Omega$, $C_L = 15 pF$ $I_F = 7.5 mA$	_	30		ns
Propagation delay time of enable from VEH to VEL	Ц Ц	2	R _L = 350 Ω, C _L = 15 pF I _F = 7.5 mA, V _{EH} = 3.0 V		25		ns
Propagation delay time of enable from V _{EL} to V _{EH}	EHL C	2	R _L = 350 Ω, C _L = 15 pF I _F = 7.5 mA, V _{EH} = 3.0 V		25		ns
Common mode transient immunity at logic high output level	CMH	3	V_{CM} = 200 V, R_L = 350 Ω V_O (min) = 2 V, I_F = 0 mA	_	200	_	V / μs
Common mode transient immunity at logic low output level	CML	3	V_{CM} = 200 V, R_L = 350 Ω V_O (max) = 0.8 V, I_F = 5 mA	_	-500	_	V/μs

Instruction for use

- A ceramic capacitor (0.1 μF) should be connected from pin 8 and pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between the capacitor and coupler should not exceed 1 cm.
- 2. Maximum electrostatic discharge voltage for any pins: 180 V (C = 200 pF, R = 0).

Test Circuit 1: Switching Time Test Circuit

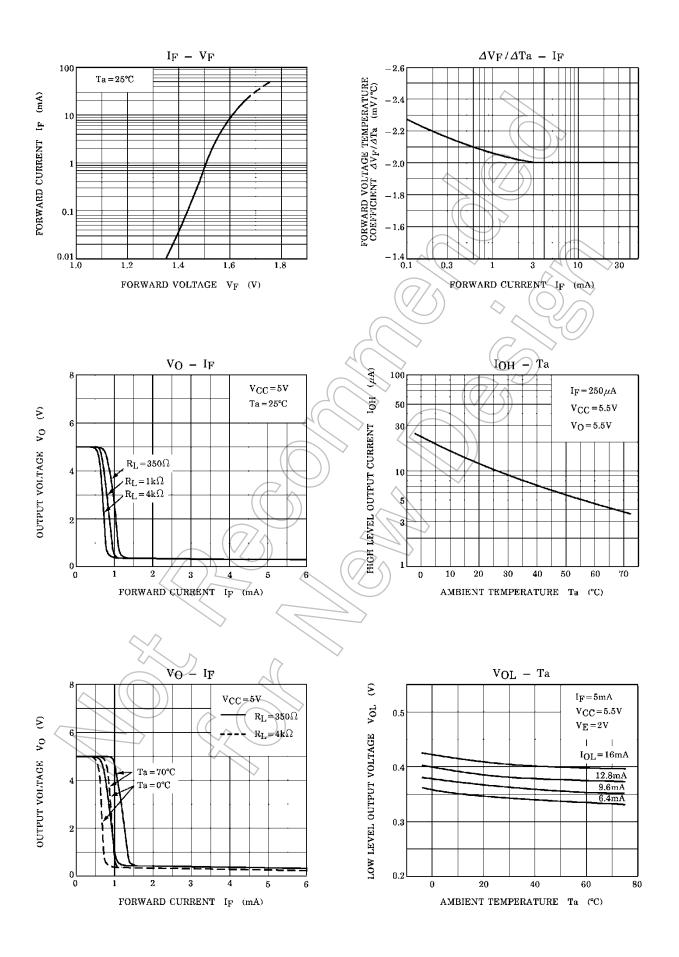




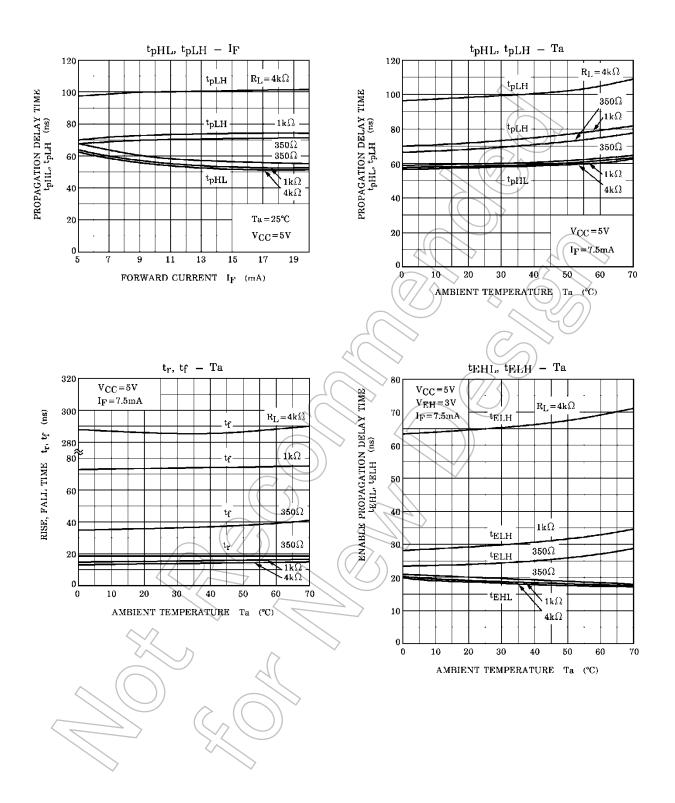
CMH: The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high output state (i.e., VO > 2.0 V). Measured in volts per microsecond (V / μ s).

CML: The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., VO < 0.8 V). Measured in volts per microsecond (V / μ s).

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