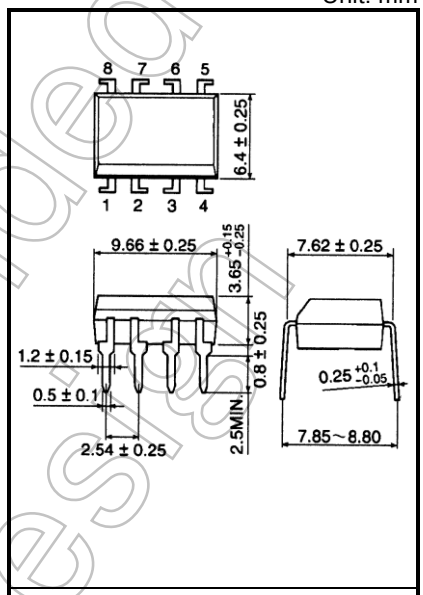
TOSHIBA Photocoupler GaAℓAs Ired & Photo-IC

TLP554

Isolated Line Receiver
Simplex/Multiplex Data Transmission
Computer-Peripheral Interface
Microprocessor System Interfaces
Digital Isolation for A/D, D/A Conversion

Unit: mm



JEDEC	―
TOSHIBA	11-10C4

Weight: 0.54 g (typ.)

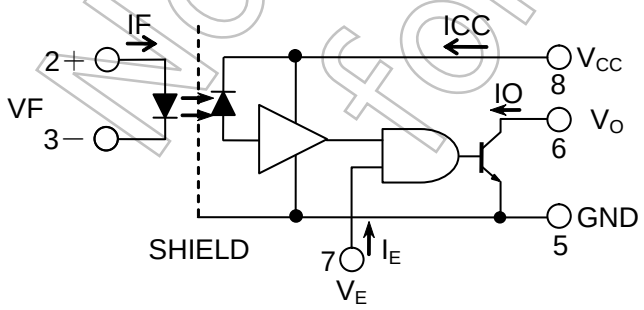
The TOSHIBA TLP554 a photocoupler which combines a GaAℓAs IRED as the emitter and an integrated high gain, high speed photodetector.
The output of the detector circuit is an open collector, Schottky Clamped transistor.
A Faraday shield integrated on the photodetector chip reduces the effects of capacitive coupling between the input LED emitter and the high gain stages of the detector. This provides an effective common mode transient immunity of 1000 V/μs.

- Input Current Threshold : I_F = 5 mA (max)
- Switching Speed : 10 MBd (typ. @NRZ)
- Common mode transient immunity : ±1000 V/μs (min)
- Guaranteed Performance over Temperature : 0 to 70°C
- Isolation Voltage : 2500 Vrms (min)
- UL approved : UL1577, File No.E67349
- c-UL approved :CSA Component Acceptance Service No. 5A, File No.E67349

Truth Table

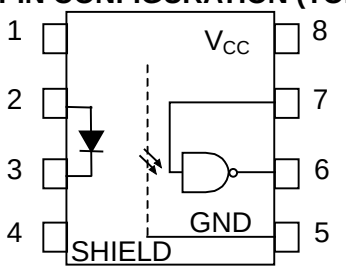
INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

Schematic



Note: A 0.1μF bypass capacitor must be connected Between pins 8 and 5.

PIN CONFIGURATION (TOP VIEW)



1:NC
2:ANODE
3:CATHODE
4:N.C.
5:GND
6:OUTPUT
7:ENABLE
8:V_{CC}

Start of commercial production
1985-01

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Low Level input Voltage	V_{FL}	-3	0	1.0	V
High Level input current	I_{FH}	6.3 (Note 1)	—	20	mA
Supply Voltage (Note 2)	V_{CC}	4.5	5	5.5	V
High-Level Enable Voltage	V_{EH}	2.0	—	V_{CC}	V
Low-Level Enable Voltage	V_{EL}	0	—	0.8	V
Fan Out(TTL Load)	N	—	—	8	—
Operating Temperature	Topr	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: 6.3 mA condition permits at least 20% CTR degradation. Initial switching threshold is 5.0 mA or less.

Note 2: Denotes the operating range, not the recommended operating condition.

Absolute Maximum Ratings (Ta = 25°C)

Characteristic			Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating	(Ta > 85°C)	$\Delta I_F/\Delta Ta$	-1.6	mA/°C
	Reverse voltage		V_R	5	V
	Input power dissipation		P_D	100	mW
	Input power dissipation derating	(Ta > 85°C)	$\Delta P_D/°C$	-2.5	mW/°C
DETECTOR	Output current		I_O	25	mA
	Output voltage		V_O	-0.5 to 7	V
	Supply voltage	(Note 1)	V_{CC}	7	V
	Enable voltage	(Note 2)	V_E	5.5	V
	Output power dissipation		P_O	40	mW
	Output power dissipation derating	(Ta > 85°C)	$\Delta Po/\Delta Ta$	-2.6	mW/°C
Storage temperature range			T_{stg}	-55 to 125	°C
Operating temperature range			T_{opr}	-40 to 85	°C
Lead soldering temperature (10 s)		(Note 3)	T_{sol}	260	°C
Isolation voltage (AC, 60 s, R.H.≤ 60%)		(Note 4)	BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 60 s Maximum.

Note 2: Not to exceed V_{CC} by more than 500 mV.

Note 3: 2 mm below seating plane.

Note 4: Device considered a two-terminal device :Pins 1, 2, 3 and 4 shorted together,and Pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics
(Unless otherwise specified Ta = 0 to 70°C , V_{CC} = 4.5 to 5.5 V , V_{FL} ≤ 1.0 V)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Forward Voltage		V_F	I_F = 10 mA, Ta=25°C	—	1.65	1.80	V
Temperature Coefficient of Forward Voltage		$\Delta V_F/\Delta Ta$	I_F = 10 mA	—	-2.0	—	mV/°C
Input Reverse Current		I_R	V_R = 5 V, Ta = 25°C	—	—	10	μA
Input Capacitance		C_T	V_F = 0 V, f = 1MHz, Ta=25°C	—	45	—	pF
High-Level Output Current		I_{OH}	V_F = 1.0 V, V_O = 5.5 V V_E = 2.0 V	—	10	250	μA
			V_F = 1.0 V, V_O = 5.5 V V_E = 2.0 V, Ta = 25°C	—	0.5	10	
Low-Level Output Voltage		V_{OL}	I_F = 5 mA, V_E = 2.0 V I_{OL} = 13 mA (Sinking)	—	0.4	0.6	V
High Level input current		I_{FH}	I_{OL} = 13 mA (Sinking) V_E = 2.0 V, V_{OL} = 0.6 V	—	—	5	mA
Supply Current	High Level	I_{CCH}	V_{CC} = 5.5 V, I_F = 0 mA, V_E = 0.5 V	—	7	15	mA
	Low Level	I_{CCL}	V_{CC} = 5.5 V, I_F = 10 mA V_E = 0.5 V	—	12	19	
Enable Current	High Level	I_{EH}	V_{CC} = 5.5 V, V_E = 2.0 V	—	-1.0	—	mA
	Low Level	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	—	-1.6	-2.0	
Enable Voltage	High Level	V_{EH}	(Note 1)	2.0	—	—	V
	Low Level	V_{EL}	—	—	—	0.8	
Resistance (Input-Output)		R_S	V_S = 500 V, R.H. ≤ 60%, Ta = 25°C, (Note 2)	5×10^{10}	10^{14}	—	Ω
Capacitance (Input-Output)		C_S	V_S = 0 V, f = 1 MHz, Ta = 25°C (Note 2)	—	0.6	—	pF

Note: All typ.values are at Ta = 25°C

Note 1: No pull up resistor required as the device has an internal pull up resistor.

Note 2: Device considered a two-terminal device :Pins 1, 2, 3 and 4 shorted together,and Pins 5, 6, 7 and 8 shorted together.

Switching Characteristics (Ta = 25°C, VCC = 5 V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation Delay Time (L→H)	t_{pLH}	1	I_F = 7.5→0 mA, R_L = 350 Ω C_L = 15 pF	—	60	120	ns
Propagation Delay Time (H→L)	t_{pHL}		I_F = 0→7.5 mA, R_L = 350 Ω C_L = 15 pF	—	60	120	
Output Rise Time(10-90%)	t_r		I_F = 7.5→0 mA, R_L = 350 Ω C_L = 15 pF	—	30	—	
Output Fall Time(90-10%)	t_f		I_F = 0→7.5 mA, R_L = 350 Ω C_L = 15 pF	—	30	—	
Enable Propagation Delay Time (L→H)	t_{ELH}	2	V_E = 0.5→3.0 V, R_L = 350 Ω I_F = 7.5 mA, C_L = 15 pF	—	25	—	ns
Enable Propagation Delay Time (H→L)	t_{EHL}		V_E = 3.0→0.5 V, R_L = 350 Ω I_F = 7.5 mA, C_L = 15 pF	—	25	—	
Common Mode Transient Immunity at Hight Level Outout (Note 1)	CM_H	3	I_F = 0 mA, R_L = 350 Ω V_{CM} = 400 V, $V_{O(min)}$ = 2 V	1000	10000	—	V/μs
Common Mode Transient Immunity at Low Level Outout (Note 2)	CM_L		I_F = 7.5 mA, R_L = 350Ω V_{CM} = 400 V, $V_{O(max)}$ = 0.8 V	-1000	-10000	—	

Note: A ceramic capacitor (0.1 μF) should be connected from pin 8 (V_{CC}) to pin 5 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

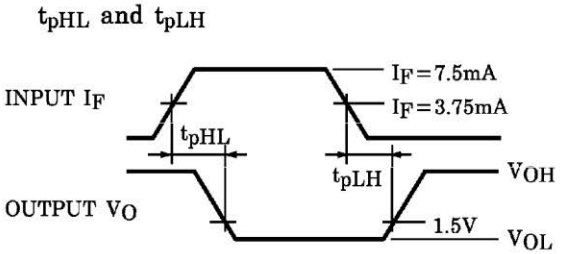
Note: Maximum electrostatic discharge voltage for any pins: 180 V (C = 200 pF, R = 0)

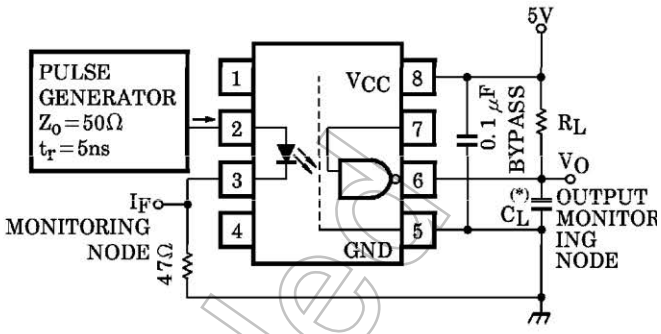
Note 1: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V)

Note 2: CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V).

TEST CIRCUIT 1.

t_{pHL} and t_{pLH}

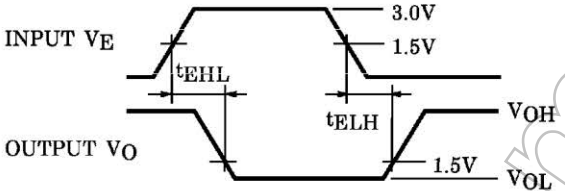


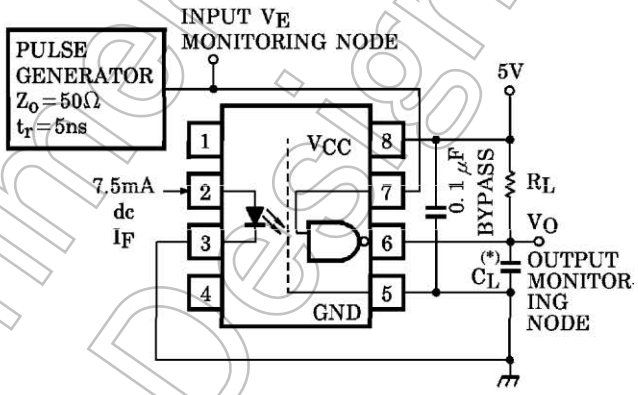


(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 2.

t_{ELH} and t_{EHL}

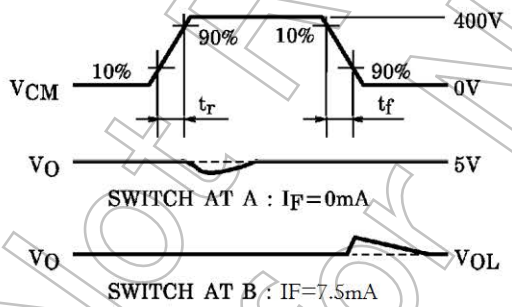


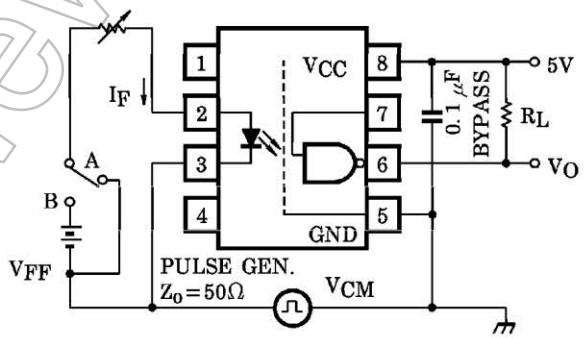


(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

TEST CIRCUIT 3.

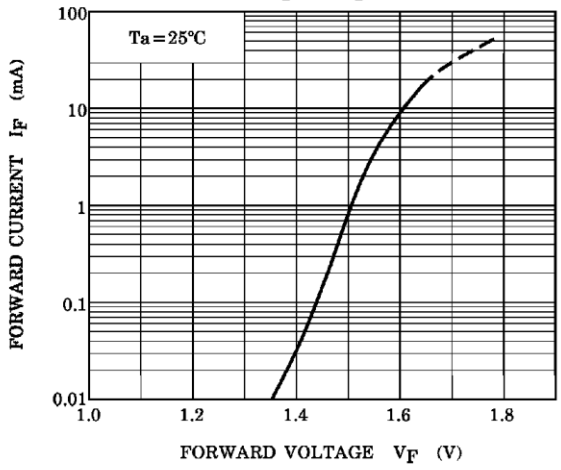
Transient Immunity and Typ. Waveforms.



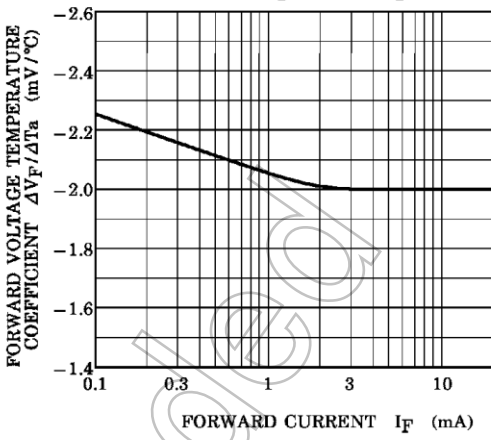


$$CM_H = \frac{320(V)}{t_r(\mu s)},\ CM_L = \frac{320(V)}{t_f(\mu s)}$$

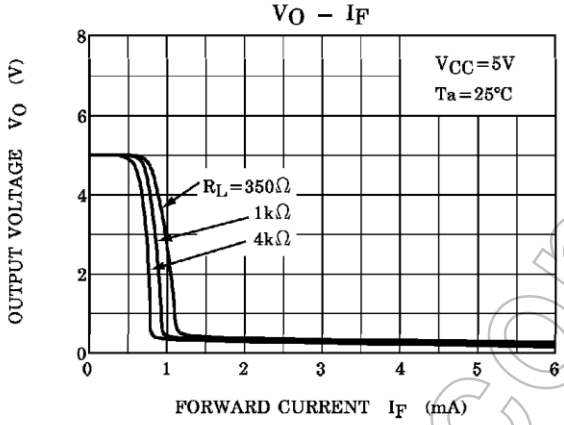
$I_F - V_F$



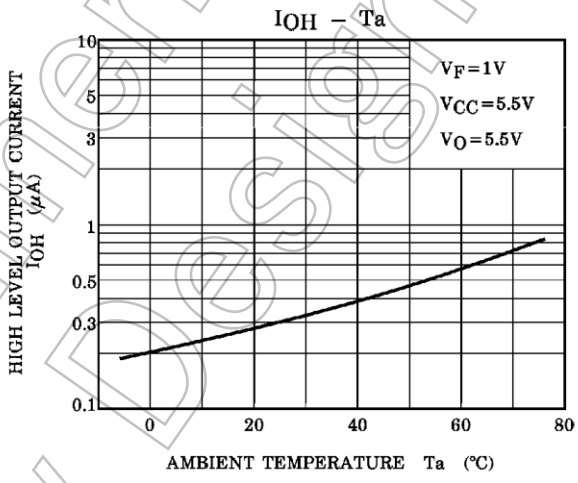
$\Delta V_F / \Delta Ta - I_F$



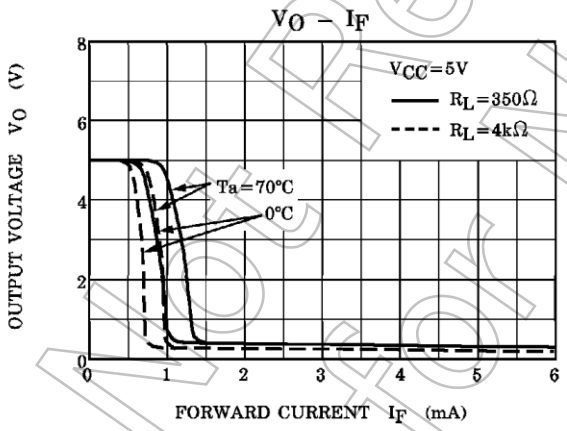
$V_O - I_F$



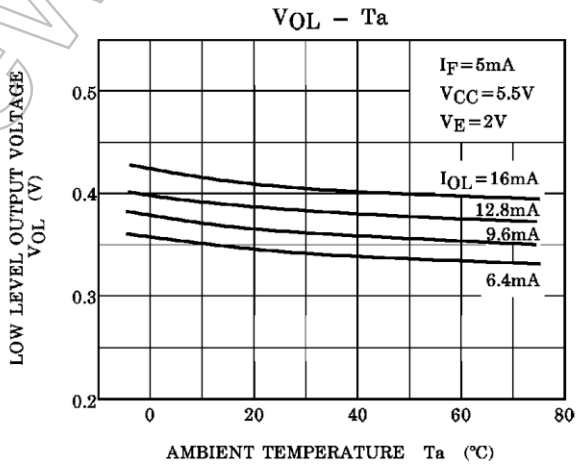
$I_{OH} - Ta$



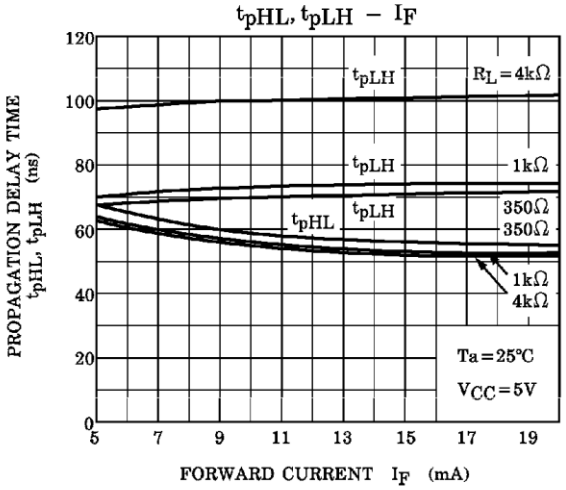
$V_O - I_F$



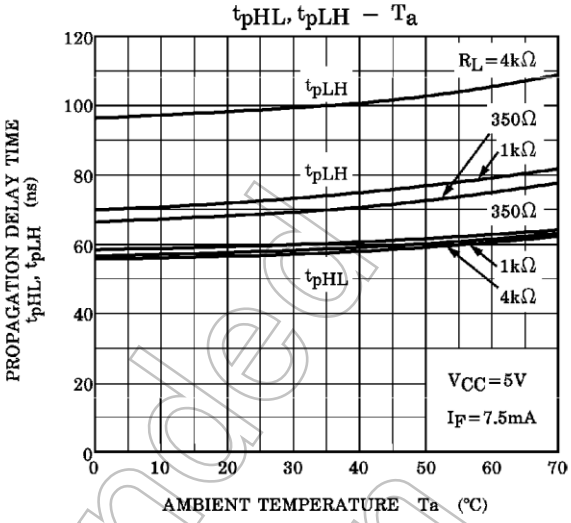
$V_{OL} - Ta$



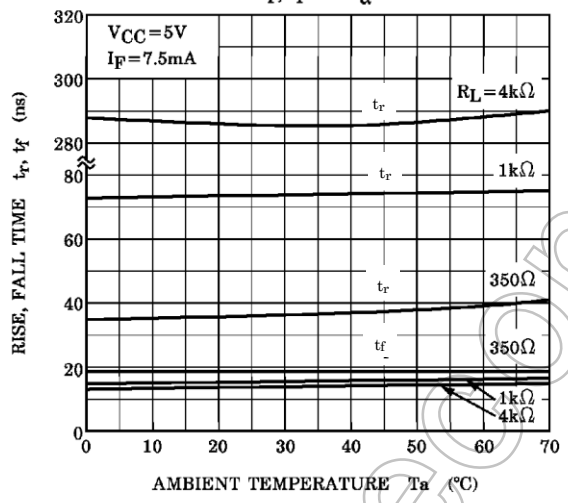
t_{pHL}, t_{pLH} – I_F



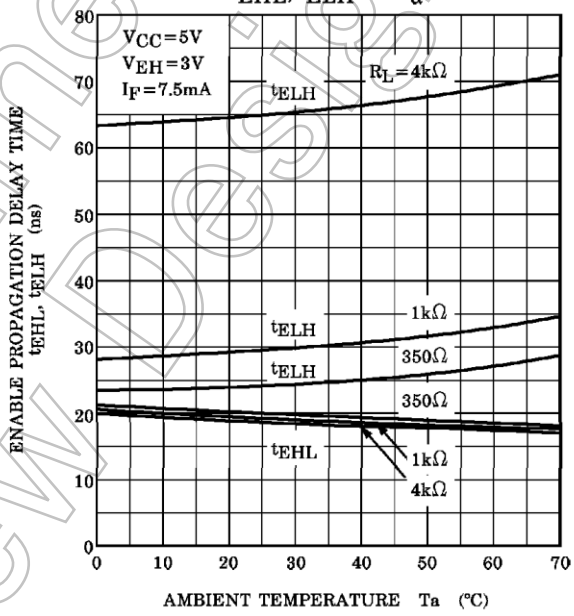
t_{pHL}, t_{pLH} – T_a



t_r, t_f – T_a



t_{EHL}, t_{ELH} – T_a



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