

TLP705F

Plasma Display Panel
Industrial Inverter
IGBT/Power MOS FET Gate Drive

TLP705F consists of an infrared LED and an integrated photodetector. This unit is 6-lead SDIP package. TLP705F is 50% smaller than 8pin DIP and has suited the safety standard reinforced insulation class. So mounting area in safety standard required equipment can be reduced. TLP705F is suitable for gate driving circuit of IGBT or power MOS FET. Especially TLP705F is capable of "direct" gate drive of lower Power IGBTs.

- Peak output current : ± 0.45 A (max)
- Operating frequency : 250kHz (max)
- Guaranteed performance over temperature : -40 to 100°C
- Supply current : 3.0mA (max)
- Power supply voltage : 10 to 20 V
- Threshold input current : IFLH = 8 mA (max)
- Switching time (tpLH / tpHL) : 200 ns (max)
- Common mode transient immunity : 10 kV/ μ s (min)
- Isolation voltage : 5000 Vrms (min)

• Construction Mechanical Rating

| | |
|----------------------|--------------|
| Creepage Distance | 8.0 mm (min) |
| Clearance | 8.0 mm (min) |
| Insulation Thickness | 0.4 mm (min) |

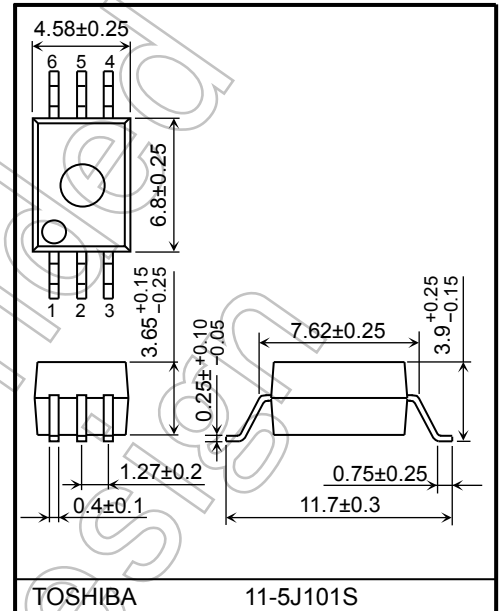
- UL-recognized : UL 1577, File No.E67349
- cUL-recognized : CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved : EN 60747-5-5, EN 62368-1 (Note 1)

Note 1: When a VDE approved type is needed, please designate the **Option(D4)**.

Truth Table

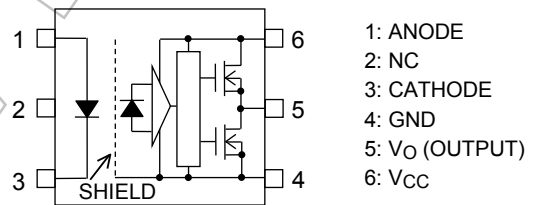
| Input | LED | Tr1 | Tr2 | Output |
|-------|-----|-----|-----|--------|
| H | ON | ON | OFF | H |
| L | OFF | OFF | ON | L |

Unit: mm

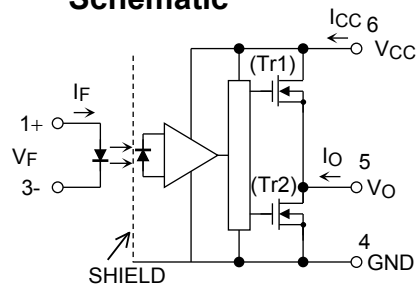


Weight: 0.26 g (typ.)

Pin Configuration (Top View)



Schematic



Note: A 0.1 μ F bypass capacitor must be connected between pins 6 and 4.

Start of commercial production
2004-04

Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|--|--|---------------------------|------------------|---------|
| LED | Forward current | I_F | 20 | mA |
| | Forward current derating (Ta ≥ 85°C) | $\Delta I_F / \Delta T_a$ | -0.54 | mA/°C |
| | Peak transient forward current (Note 1) | I_{FP} | 1 | A |
| | Reverse voltage | V_R | 5 | V |
| | Diode power dissipation | P_D | 40 | mW |
| | Diode power dissipation derating (Ta ≥ 85°C) | $\Delta P_D / ^\circ C$ | -1.0 | mW/°C |
| | Junction temperature | T_j | 125 | °C |
| Detector | "H" peak output current (Note 2) | I_{OPH} | -0.45 | A |
| | "L" peak output current (Note 2) | I_{OPL} | 0.45 | A |
| | Output voltage | V_O | 25 | V |
| | Supply voltage | V_{CC} | 25 | V |
| | Power dissipation | P_C | 400 | mW |
| | Power dissipation derating (Ta ≥ 25°C) | $\Delta P_C / ^\circ C$ | -4.0 | mW / °C |
| | Junction temperature | T_j | 125 | °C |
| Operating frequency (Note 3) | f | 250 | kHz | |
| Storage temperature range | T_{stg} | -55 to 125 | °C | |
| Operating temperature range | T_{opr} | -40 to 100 | °C | |
| Lead soldering temperature (10 s) (Note 4) | T_{sol} | 260 | °C | |
| Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 5) | BV_S | 5000 | V _{rms} | |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note : A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: Pulse width $P_W \leq 1 \mu s$, 300 pps

Note 2: Exponential waveform pulse width $P_W \leq 2 \mu s$, $f \leq 15 \text{ kHz}$

Note 3: Exponential waveform $I_{OPH} \leq -0.25 \text{ A}$ ($P_W \leq 80 \text{ ns}$), $I_{OPL} \leq +0.25 \text{ A}$ ($P_W \leq 80 \text{ ns}$), $T_a = 100 \text{ }^\circ\text{C}$

Note 4: It is effective soldering area of Lead.

Note 5: Device considered a two terminal device: pins 1, 2 and 3 shorted together, and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

| Characteristics | Symbol | Min | Typ. | Max | Unit |
|----------------------------|-------------------------------------|------|------|--------|------|
| Input current, ON (Note 1) | I _F (ON) | 10 | — | 15 | mA |
| Input voltage, OFF | V _F (OFF) | 0 | — | 0.8 | V |
| Supply voltage | V _{CC} | 10 | — | 20 | V |
| Peak output current | I _{OPH} / I _{OPL} | — | — | ± 0.15 | A |
| Operating temperature | T _{opr} | - 40 | — | 100 | °C |

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note: If the rising slope of the supply voltage (V_{CC}) for the detector is steep, stable operation of the internal circuits cannot be guaranteed.

Be sure to set 3.0 V/μs or less for a rising slope of the V_{CC}.

Note 1: Input signal rise time (fall time) < 0.5 μs.

Not Recommended for New Design

Electrical Characteristics (Ta = -40 to 100°C, unless otherwise specified)

| Characteristics | | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | |
|--|-----------|----------------------|--------------|---|---|-------|-------|-------|----|
| Forward voltage | | V _F | — | I _F = 10 mA, Ta = 25 °C | — | 1.6 | 1.8 | V | |
| Temperature coefficient of forward voltage | | ΔV _F /ΔTa | — | I _F = 10 mA | — | -2.0 | — | mV/°C | |
| Input reverse current | | I _R | — | V _R = 5 V, Ta = 25 °C | — | — | 10 | μA | |
| Input capacitance | | C _T | — | V = 0 V, f = 1 MHz, Ta = 25 °C | — | 45 | — | pF | |
| Output current (Note 1) | “H” Level | I _{OPH} | 1 | V _{CC} = 15 V I _F = 10 mA | V ₆₋₅ = 4 V | -0.15 | -0.35 | — | A |
| | | | | | V ₆₋₅ = 10 V | -0.3 | -0.6 | — | |
| | “L” Level | I _{OPL} | 2 | V _{CC} = 15 V I _F = 0 mA | V ₅₋₄ = 2 V | 0.15 | 0.36 | — | |
| | | | | | V ₅₋₄ = 10 V | 0.3 | 0.62 | — | |
| Output voltage | “H” Level | V _{OH} | 3 | V _{CC} = 10 V | I _O = -100 mA, I _F = 10 mA | 6.0 | 8.5 | — | V |
| | | | | | I _O = 100 mA, V _F = 0.8 V | — | 0.4 | 1.0 | |
| Supply current | “H” Level | I _{CCH} | 5 | V _{CC} = 10 to 20 V V _O = open | I _F = 10 mA | — | 2.0 | 3.0 | mA |
| | | | | | I _F = 0 mA | — | 2.0 | 3.0 | |
| Threshold input current | L → H | I _{FLH} | — | V _{CC} = 15 V, V _O > 1 V | — | 2.5 | 8 | mA | |
| Threshold input voltage | H → L | V _{FHL} | — | V _{CC} = 15 V, V _O < 1 V | 0.8 | — | — | V | |
| Supply voltage | | V _{CC} | — | — | 10 | — | 20 | V | |

Note: All typical values are at Ta = 25°C

Note: This product is more sensitive than the conventional product to static electricity (ESD) because of a lowest power consumption design.

General precaution to static electricity (ESD) is necessary for handling this component.

Note 1: Duration of IO time ≤ 50 μs

Isolation Characteristics (Ta = 25°C)

| Characteristic | Symbol | Test Condition | Min | Typ. | Max | Unit |
|-----------------------------|------------------|------------------------------------|------------------|------------------|-----|------------------|
| Capacitance input to output | C _S | V = 0 V, f = 1 MHz | — | 1.0 | — | pF |
| Isolation resistance | R _S | R.H. ≤ 60 %, V _S = 500V | 10 ¹² | 10 ¹⁴ | — | Ω |
| Isolation voltage | B _V S | AC, 60 s | 5000 | — | — | V _{rms} |

Note : Device considered a two terminal device: pins 1, 2 and 3 shorted together, and pins 4, 5 and 6 shorted together.

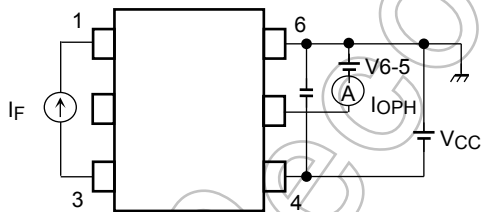
Switching Characteristics (Ta = -40 to 100°C, unless otherwise specified)

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit | |
|---|-----------------|--------------|--|---|--------|-----|------|------|
| Propagation delay time | L → H | 7 | V _{CC} = 20 V R _g = 30 Ω C _g = 1 nF F = 250 kHz Duty Cycle = 50 % | Ta = 25 °C I _F = 0 → 10 mA | 70 | 95 | 170 | ns |
| | H → L | | | Ta = 25 °C I _F = 10 → 0 mA | 70 | 105 | 170 | |
| Propagation delay time | L → H | | | Ta = -40 to 100 °C I _F = 0 → 10 mA | 50 | — | 200 | |
| | H → L | | | Ta = -40 to 100 °C I _F = 10 → 0 mA | 50 | — | 200 | |
| Propagation delay skew (Note 1) | tpsk | | | Ta = -40 to 100 °C I _F = 10 mA | -90 | — | 90 | |
| Switching time dispersion between ON and OFF | tpHL - tpLH | | | Ta = -40 to 100 °C I _F = 10 mA | -65 | — | 65 | |
| Output rise time (10-90%) | tr | | | I _F = 0 → 10 mA | — | — | — | |
| Output fall time (90-10%) | tf | | | I _F = 10 → 0 mA | — | — | — | |
| Common mode transient immunity at high level output | CMH | 8 | V _{CM} = 1000 Vp-p V _{CC} = 20 V Ta = 25 °C | I _F = 10 mA V _O (min) = 16 V | -10000 | — | — | V/μs |
| Common mode transient immunity at low level output | CM _L | | | I _F = 0 mA V _O (max) = 1 V | 10000 | — | — | |

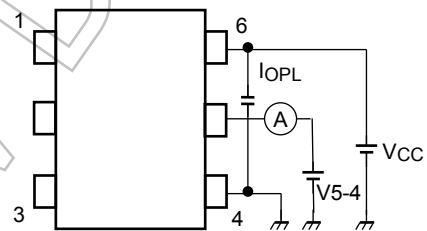
Note: All typical values are at Ta = 25 °C

Note 1: Propagation delay difference between any two parts.

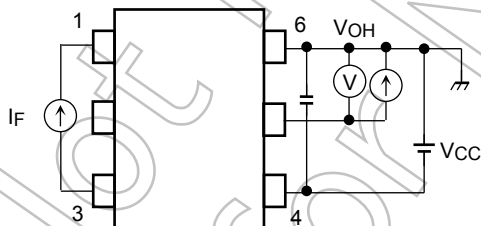
Test Circuit 1: IOPH



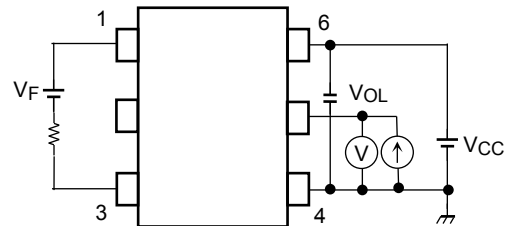
Test Circuit 2: IOPL



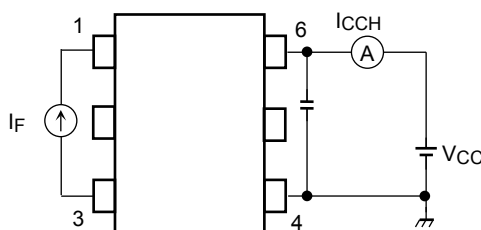
Test Circuit 3: VOH



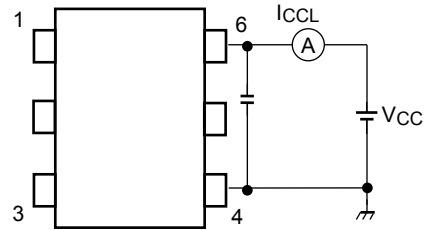
Test Circuit 4: VOL



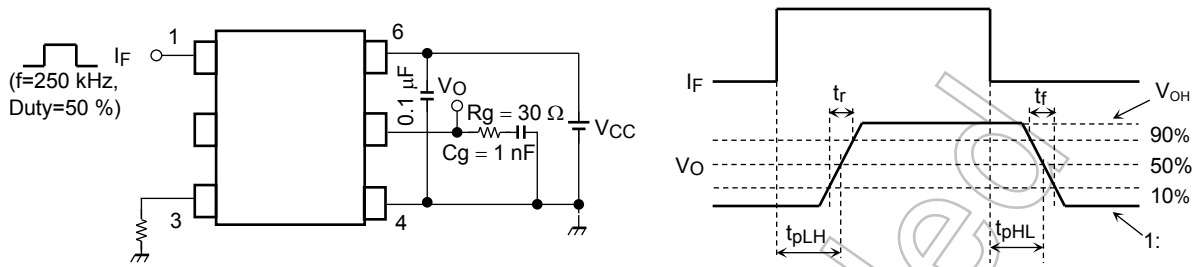
Test Circuit 5: ICCH



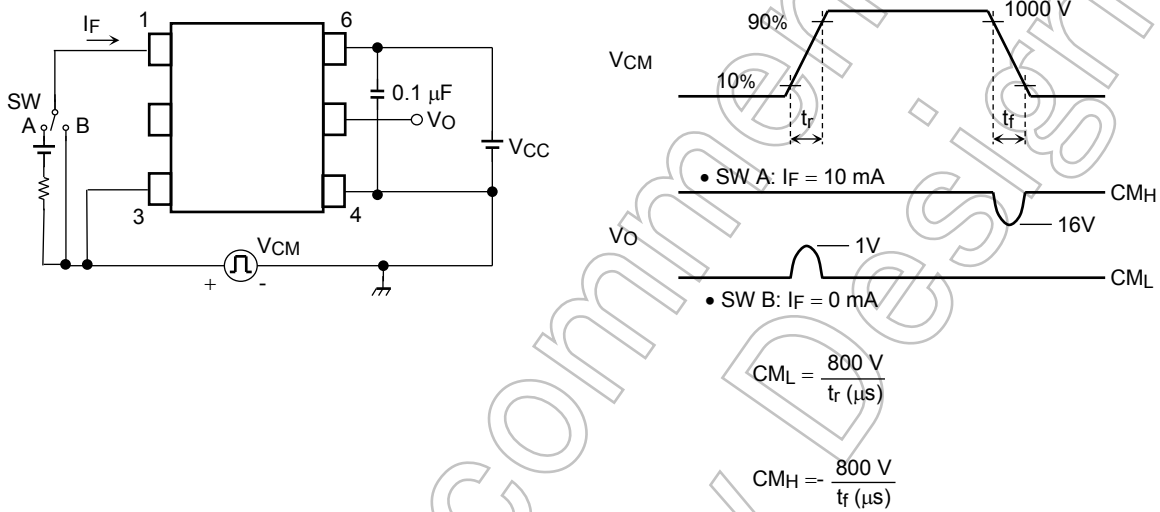
Test Circuit 6: ICCL



Test Circuit 7 : t_{pLH} , t_{pHL} , t_r , t_f , PWD



Test Circuit 8: CM_H , CM_L



Note: CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

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