

TLP715

Isolated Bus Drivers
 High Speed Line Receivers
 Microprocessor System Interfaces

The Toshiba TLP715 consists of an infrared emitting diode and an integrated high-gain, high-speed photodetector. This unit is a 6-pin SDIP. The TLP715 is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification. The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity. The TLP715 is buffer logic type. For inverter logic type, the TLP718 is in line-up.

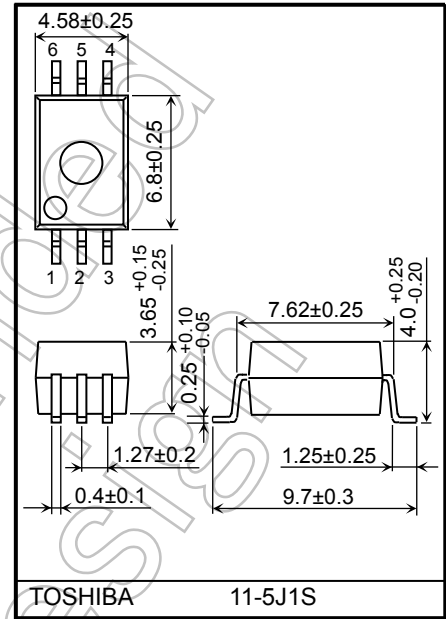
- Buffer logic output (totem pole output)
- Guaranteed performance over temperature: -40 to 100°C
- Power supply voltage: 4.5 to 20 V
- Input current: I_{FLH} = 3 mA (max)
- Switching time (t_{pLH} / t_{pHL}): 250 ns (max)
- Common-mode transient immunity: ±10 kV / μs (min)
- Isolation voltage: 5000 V_{rms} (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved : EN 60747-5-5 , EN 62368-1 (Note 1)

Note 1 : When a VDE approved type is needed, please designate the **Option(D4)**.

Truth Table

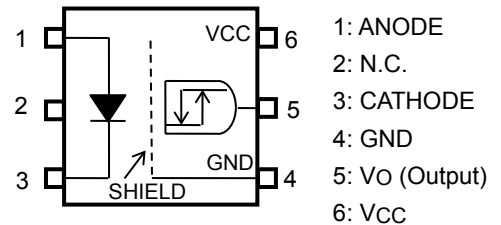
Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Unit: mm

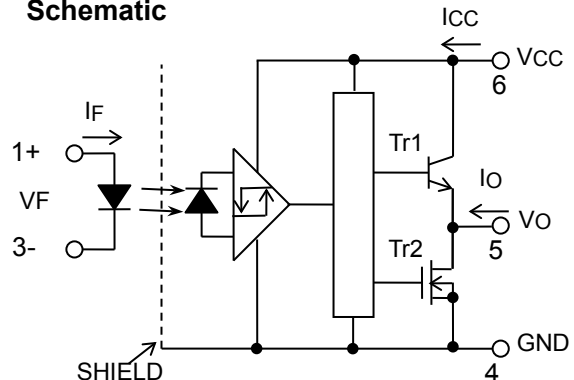


Weight: 0.26 g (typ.)

Pin Configuration (Top View)



Schematic



Note: 0.1 μF bypass capacitor must be connected between pins 6 and 4.

Start of commercial production
 2008-11

Absolute Maximum Ratings (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 83°C)	IF	20	mA
	Forward Current Derating (Ta ≥ 83°C)	ΔIF/ΔTa	-0.48	mA/°C
	Peak Transient Forward Current (Note 1)	IFPT	1	A
	Reverse Voltage	VR	5	V
	Diode power dissipation	PD	40	mW
	Diode power dissipation derating (Ta ≥ 83°C)	ΔPD/°C	-0.95	mW/°C
	Junction Temperature	Tj	125	°C
DETECTOR	Output Current 1 (Ta ≤ 25°C)	IO1	25 / -15	mA
	Output Current 2 (Ta ≤ 100°C)	IO2	13 / -13	mA
	Output Voltage	VO	-0.5 to 20	V
	Supply Voltage	VCC	-0.5 to 20	V
	Power dissipation	PC	75	mW
	Power dissipation derating (Ta ≥ 25°C)	ΔPC / °C	-0.75	mW / °C
	Junction Temperature	Tj	125	°C
Operating Temperature Range		Topr	-40 to 100	°C
Storage Temperature Range		Tstg	-55 to 125	°C
Lead Solder Temperature (10 s)		Tsol	260	°C
Isolation Voltage (AC, 60 s, R.H. ≤ 60 %) (Note 2)		BVS	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width PW ≤ 1 μs, 300 pps.

Note 2: Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON	IF(ON)	4.5	-	10	mA
Input Voltage, OFF	VF(OFF)	0	-	0.8	V
Supply Voltage (Note 1)	VCC	4.5	-	20	V
Operating Temperature	Topr	-40	-	100	°C

Note 1: This item denotes operating ranges, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics

(Unless otherwise specified, Ta = -40 to 100°C, VCC = 4.5 to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT	
Input forward voltage	V _F	-	I _F = 5 mA, Ta = 25 °C	1.4	1.6	1.7	V	
Temperature coefficient of	ΔV _F /ΔTa	-	I _F = 5 mA	-	-2.0	-	mV/°C	
Input reverse current	I _R	-	V _R = 5 V, Ta = 25 °C	-	-	10	μA	
Input capacitance	C _T	-	V = 0 V, f = 1 MHz, Ta = 25 °C	-	45	-	pF	
Logic LOW output voltage	V _{OL}	1	I _{OL} = 3.5 mA, V _F = 0.8 V	-	0.2	0.6	V	
Logic HIGH output voltage	V _{OH} (Note 1)	2	I _{OH} = -2.6 mA, I _F = 5 mA	V _{CC} = 4.5 V	2.7	3.5	-	V
				V _{CC} = 20 V	17.4	19	-	
Logic LOW supply current	I _{CCL}	3	V _F = 0 V	-	-	3.0	mA	
Logic HIGH supply current	I _{CCH}	4	I _F = 5 mA	-	-	3.0	mA	
Logic LOW short circuit output current (Note 2)	I _{OSL}	5	V _F = 0 V	V _{CC} = V _O = 5.5 V	15	80	-	mA
				V _{CC} = V _O = 20 V	20	90	-	
Logic HIGH short circuit output current (Note 2)	I _{OSH}	6	I _F = 5 mA, V _O = GND	V _{CC} = 5.5 V	-5	-15	-	mA
				V _{CC} = 20 V	-10	-20	-	
Input current logic HIGH	I _{FLH}	-	I _O = -2.6 mA, V _O > 2.4 V	-	0.4	3	mA	
Input voltage logic LOW	V _{FHL}	-	I _O = 3.5 mA, V _O < 0.6V	0.8	-	-	V	
Input current hysteresis	I _{HYS}	-	V _{CC} = 5 V	-	0.05	-	mA	

Note: All typical values are at Ta = 25 °C, V_{CC} = 5 V.

Note : A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: V_{OH} = V_{CC} - V_O [V]

Note 2: Duration of output short circuit time should not exceed 10 ms.

Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance input to output	C _S	V _S = 0 V, f = 1 MHz	-	1.0	-	pF
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 V	10 ¹²	10 ¹⁴	-	Ω
Isolation voltage	BV _S	AC, 60 s	5000	-	-	V _{rms}

Note : Device Considered a two terminal device: pins 1, 2 and 3 shorted together and pins 4, 5 and 6 shorted together.

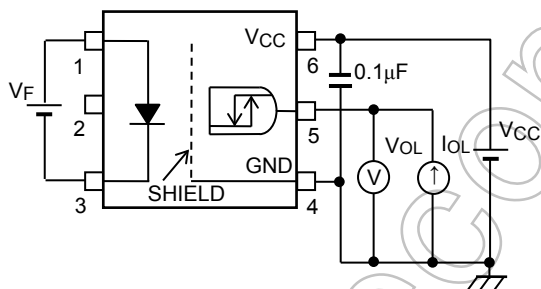
Switching Characteristics

(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 20 V)

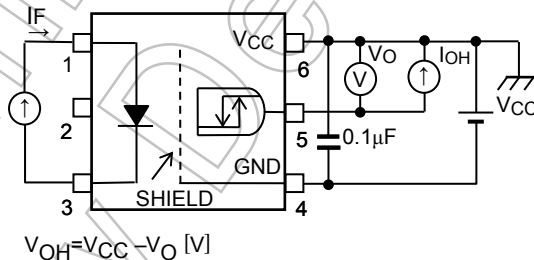
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP. *	MAX	UNIT
Propagation delay time to logic HIGH output	t_{pLH}	7 8	$I_F = 0 \rightarrow 3$ mA	30	120	250	ns
Propagation delay time to logic LOW output	t_{pHL}		$I_F = 3 \rightarrow 0$ mA	30	120	250	ns
Switching time dispersion between ON and OFF	$ t_{pLH} - t_{pHL} $		-	-	-	220	ns
Rise Time (10 – 90 %)	t_r		$I_F = 0 \rightarrow 3$ mA, $V_{CC} = 5$ V	-	30	-	ns
Fall Time (90 – 10 %)	t_f		$I_F = 3 \rightarrow 0$ mA, $V_{CC} = 5$ V	-	30	-	ns
Common-mode transient Immunity at HIGH level output	CM_H		9	$V_{CM} = 1000$ V _{p-p} , $I_F = 5$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$	10000	-	-
Common-mode transient Immunity at LOW level output	CM_L	$V_{CM} = 1000$ V _{p-p} , $I_F = 0$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$		-10000	-	-	V/ μs

*All typical values are at $T_a = 25^\circ\text{C}$.

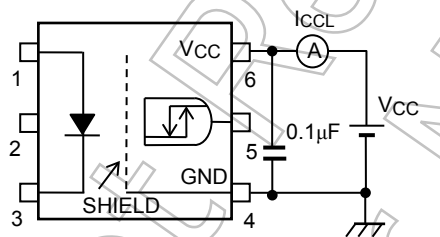
TEST CIRCUIT 1: V_{OL}



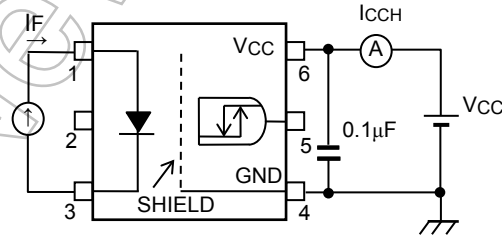
TEST CIRCUIT 2: V_{OH}



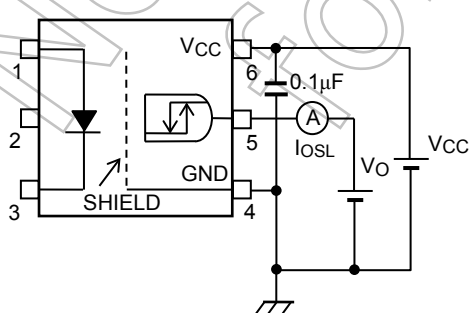
TEST CIRCUIT 3: I_{CCL}



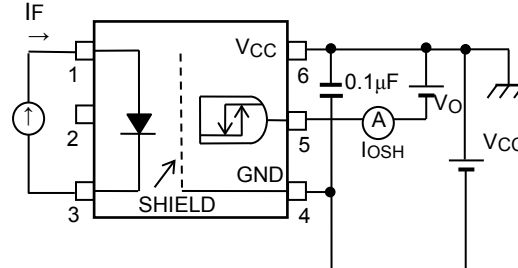
TEST CIRCUIT 4: I_{CCH}



TEST CIRCUIT 5: I_{OSL}

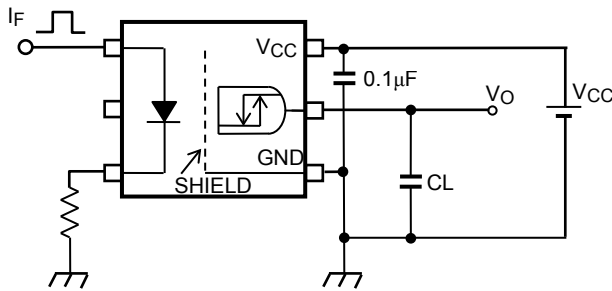


TEST CIRCUIT 6: I_{OSH}

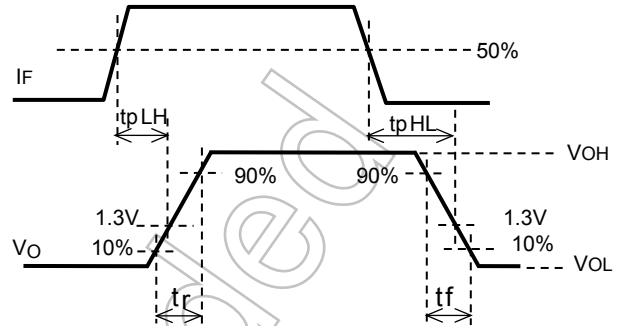


TEST CIRCUIT 7: Switching Time Test Circuit

$I_F=3\text{ mA(P.G)}$
 ($f=50\text{ kHz}$, duty=50%, less than $t_r = t_f = 5\text{ ns}$)

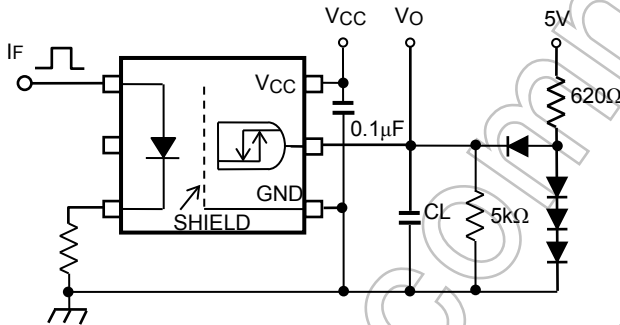


CL: stray capacitance of probe and wiring (to 15 pF)

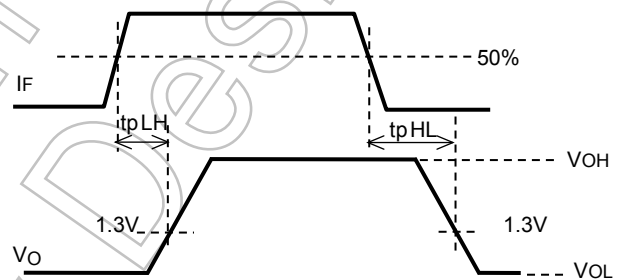


TEST CIRCUIT 8: Switching Time Test Circuit

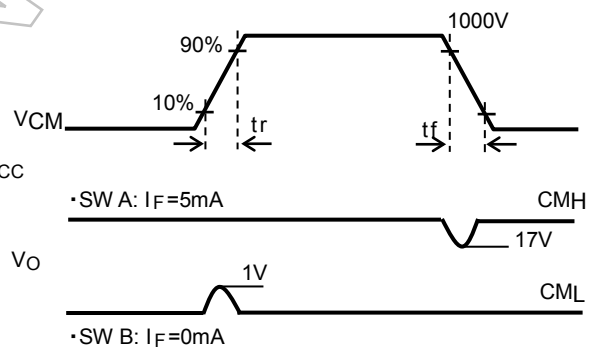
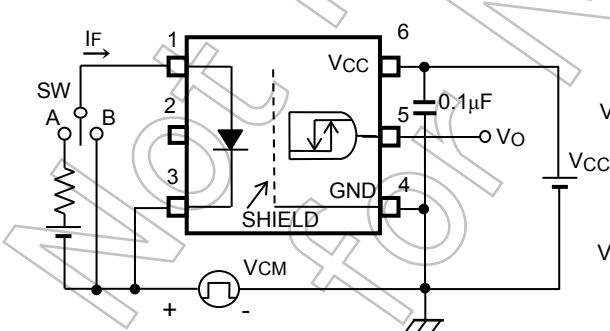
$I_F=3\text{ mA(P.G)}$
 ($f=50\text{ kHz}$, duty=50%, less than $t_r = t_f = 5\text{ ns}$)



CL: stray capacitance of probe and wiring (to 15 pF)





TEST CIRCUIT 9: Common-Mode Transient Immunity Test Circuit



$$CM_L = \frac{800(V)}{t_r(\mu s)} \quad CM_H = -\frac{800(V)}{t_f(\mu s)}$$

Note: CM_H (CM_L) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the high (low) state.

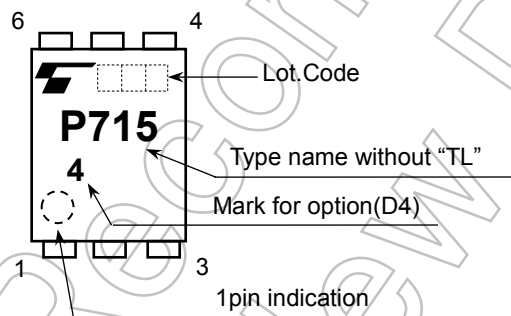
Insulation Related Specifications

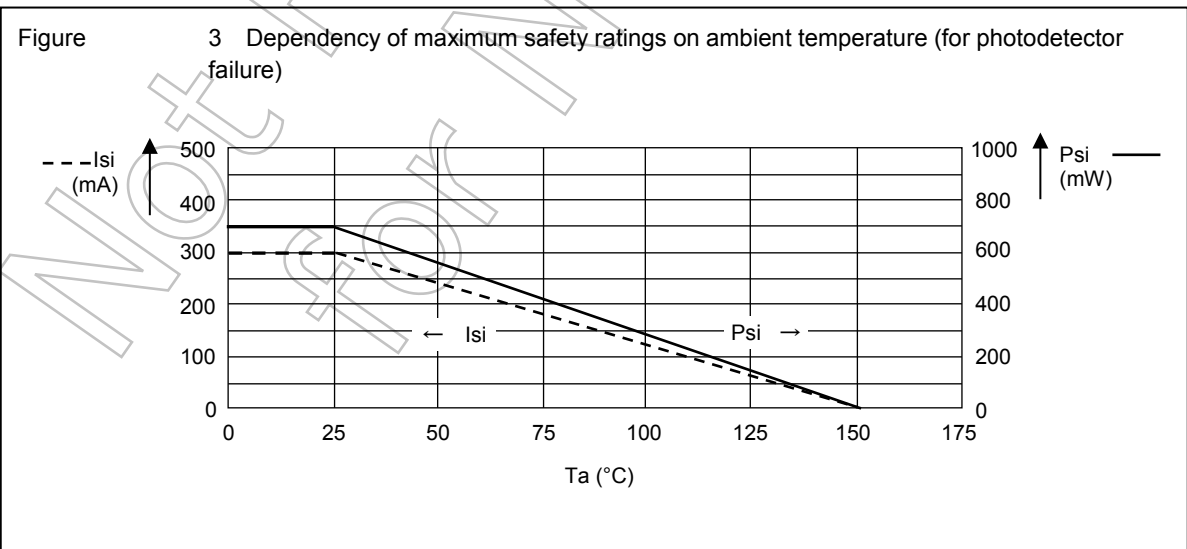
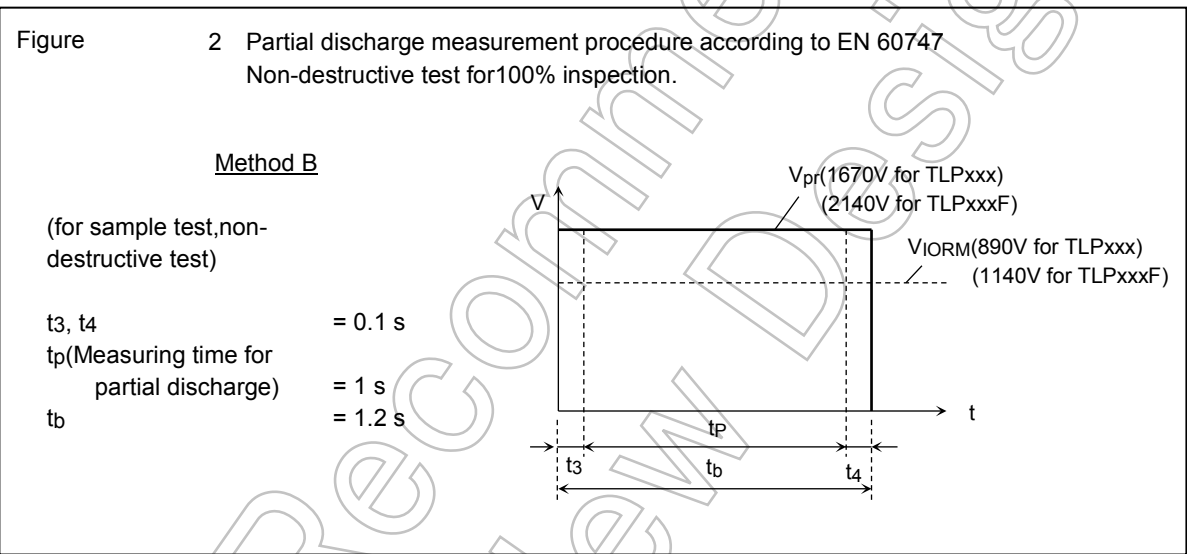
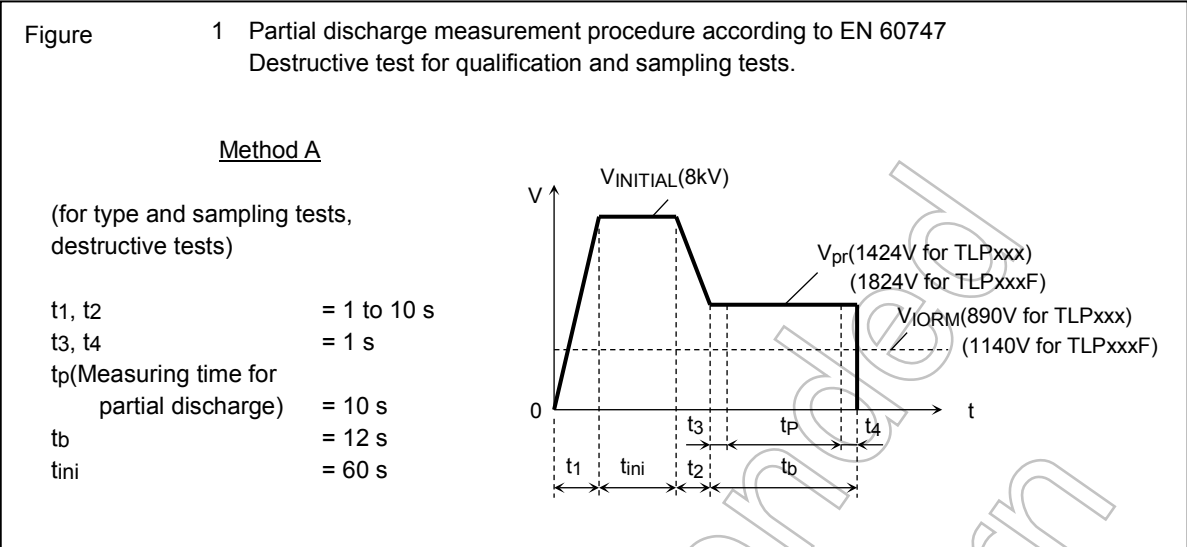
		 7.62mm pitch TLPxxx type	 10.16mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0mm	8.0mm
Minimum clearance	Cl	7.0mm	8.0mm
Minimum insulation thickness	ti	0.4mm	
Comperative tracking index	CTI	175	

1. If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. If this is not permissible, the user shall take suitable measures.
2. This photocoupler is suitable for 'safe electrical isolation' only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Marking on product for EN 60747 Option:(D4): **4**

Marking Example





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