TOSHIBA PHOTOCOUPLER IRLED & PHOTO-IC

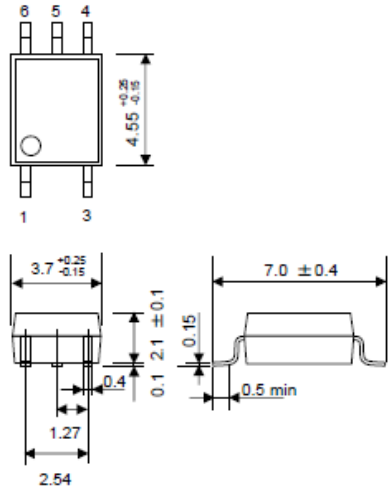
TLX9376

○ HEV (Hybrid Electric Vehicle) and EV (Electric Vehicle) Applications

The Toshiba TLX9376 consists of an infrared LED and integrated high gain, high-speed photodetector. The TLX9376 is housed in the SO6 package. It has a totem-pole output that can both sink and source current. The photodetector has an internal Faraday shield that provides a guaranteed common-mode transient immunity of 15 kV/μs. TLX9376 guarantees minimum and maximum of propagation delay time, switching speed dispersion, and high common mode transient immunity.

- Input current logic LOW output : 4.0 mA (max)
- Switching Speed : tpHL = 35 ns (max)
  : tpLH = 35 ns (max)
- Common mode transient immunity : 15kV/μs (min)
- Operating Temperature : -40 to 125°C
- Isolation voltage : 3750 Vrms (min)
- AEC-Q101 qualified

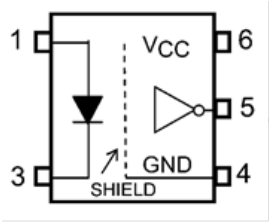
Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	11-4L1

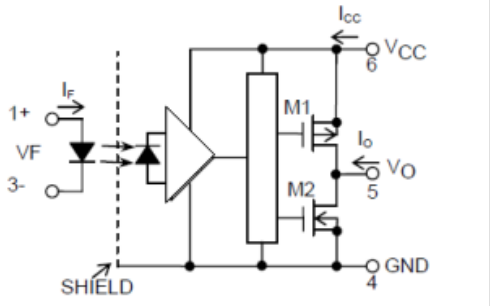
Weight: 0.08 g (typ.)

Pin Configuration



1: ANODE
3: CATHODE
4: GND
5: VO
6: VCC

Schematic



A ceramic capacitor (0.1 μF) should be connected from pin 6 (VCC) to pin 4 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Truth Table

Input	LED	M1	M2	Output
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25°C)

Characteristic			Symbol	Rating	Unit
LED	Forward Current		I_F	25	mA
	Forward Current (Ta=125 °C)		I_F	15	mA
	Forward Current Derating (Ta ≥ 70 °C)		ΔI_F/°C	-0.18	mA/°C
	Pulse Forward Current	(Note 1)	I_{FPT}	1	A
	Input Power Dissipation		PD	50	mW
	Input Power Dissipation Derating (Ta ≥ 110°C)		ΔPD/°C	-1.73	mW/°C
	Reverse Voltage		V_R	5	V
DETECTOR	Output Current		I_O	10	mA
	Output Voltage		V_O	6	V
	Supply Voltage	(Note 2)	V_{CC}	6	V
	Output Power Dissipation		P_O	40	mW
	Output Power Dissipation Derating (Ta ≥ 110°C)		ΔP_O/°C	-2.07	mW/°C
Storage Temperature Range			T_{stg}	-55 to 150	°C
Operating Temperature Range			T_{opr}	-40 to 125	°C
Lead Soldering Temperature (10 s)			T_{sol}	260	°C
Isolation Voltage (AC,60 s.,R.H.≤ 60 %)		(Note 3)	BV_S	3750	V_{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width ≤ 1 μs, 300 pps

Note 2: 60 s. (max)

Note 3: This device is considered as a two terminal device: Pins 1 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

Recommended Operating Conditions (Note)

Characteristic	Symbol	Min	Typ.	Max	Unit
Input current logic LOW output	$I_{F(ON)}$	4.5	-	10	mA
Input voltage logic HIGH output	$V_{F(OFF)}$	0	-	0.8	V
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature (Note 1)	T_{opr}	-40	-	125	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 1: Denotes the operating range, not the recommended operating condition.

Electrical Characteristics (Note)
(Unless otherwise specified, Ta = -40 to 125°C, V_{CC} =4.5 to 5.5V)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage	V_F	I_F = 10 mA, Ta=25 °C	1.45	1.57	1.75	V
		I_F = 10 mA	1.35	—	1.90	
Reverse current	I_R	V_R = 5 V, Ta = 25 °C	—	—	10	μA
Capacitance between terminals	C_T	V_F = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
Low level output voltage	V_{OL}	I_F = 4 mA, I_O = 4 mA	—	0.3	0.6	V
High level output voltage	V_{OH}	I_F = 0 mA, I_O = -4 mA, V_{CC} = 5 V	4.0	—	—	V
Input current logic LOW output	I_{FHL}	I_O = 4 mA, V_O < 0.6 V	—	—	4.0	mA
High level supply current	I_{CCH}	I_F = 0 mA	—	1.0	1.5	mA
Low level supply current	I_{CCL}	I_F = 4 mA	—	1.1	1.7	mA

Note: All typical values at V_{CC} = 5 V and Ta = 25°C.

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Capacitance input to output	C_S	V = 0 V, f = 1 MHz	—	0.5	—	pF
Isolation resistance	R_S	R.H. ≤ 60%, V_S = 500 V	5×10^{10}	10^{14}	—	Ω
Isolation voltage	BV_S	AC,60 s	3750	—	—	V_{rms}

Note . This device is considered as two-terminal device: Pins 1 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

Switching Characteristics (Note)
(Unless otherwise specified, Ta = -40 to 125°C, V_{CC}=5V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	t_{pHL}	1	Vin = 4.5 – 5.5V, Rin = 390 Ω, Cin = 100 pF, CL = 15 pF (Note 1)	—	—	35	ns
Propagation delay time (L→H)	t_{pLH}			—	—	35	
Propagation Delay Skew (Note 2)	t_{psk}			-15	—	15	
Switching Time Dispersion between ON and OFF	$\lvert t_{pHL}-t_{pLH}\rvert$			—	—	12	
Fall Time (90 – 10 %)	tf			—	2	—	
Rise Time (10 – 90 %)	tr			—	2	—	
Common mode transient immunity at high output level (Note 3)	CM_H	3	V_{CM} = 1000 Vp-p , Rin = 390 Ω, Cin = 100 pF, V_O(min)= 4.0 V, Ta=25 °C	15000	—	—	V/μs
Common mode transient Immunity at low output level (Note 4)	CM_L		VCM=1000Vp-p , Rin = 390 Ω, Cin = 100 pF,, V_O(max)= 0.4 V, Ta=25 °C	-15000	—	—	V/μs

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	t_{pHL}	2	IF = 7.5 mA, CL = 15 pF, V_{DD} = 5V (Note 1)	—	—	80	ns
Propagation delay time (L→H)	t_{pLH}			—	—	80	
Propagation Delay Skew (Note 2)	t_{psk}			-30	—	30	
Switching Time Dispersion between ON and OFF	$\lvert t_{pHL}-t_{pLH}\rvert$			—	—	25	
Fall Time (90 – 10 %)	tf			—	2	—	
Rise Time (10 – 90 %)	tr			—	2	—	
Common mode transient immunity at high output level (Note 3)	CM_H	4	V_{CM}=1000 Vp-p , I_F = 0 mA, V_O(min)= 4.0 V , Ta=25 °C	15000	—	—	V/μs
Common mode transient Immunity at low output level (Note 4)	CM_L		VCM=1000 Vp-p , IF = 7.5 mA, V_O(max)= 0.4 V , Ta = 25 °C	-15000	—	—	V/μs

Note: All typical values are at V_{CC} = 5 V and Ta = 25°C.

Note: A ceramic capacitor (0.1 μF) should be connected from pin 6 (V_{CC}) to pin 4 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

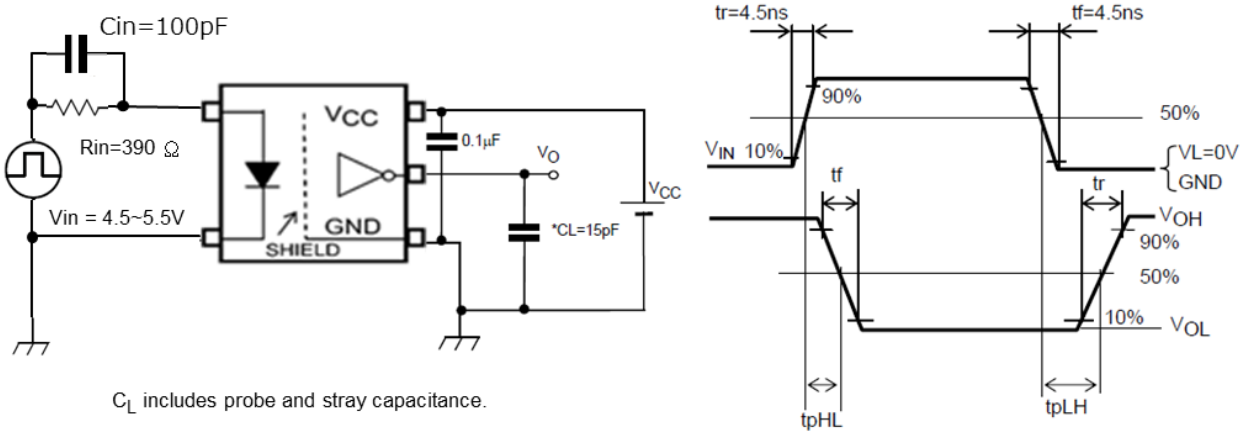
Note 1: C_L is less than 15pF which includes probe and Jig/stray wiring capacitance.

Note 2: Propagation delay skew is defined as the difference between the largest and smallest propagation delay times (i.e. tpHL or tpLH) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

Note 3: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 4.0 V)

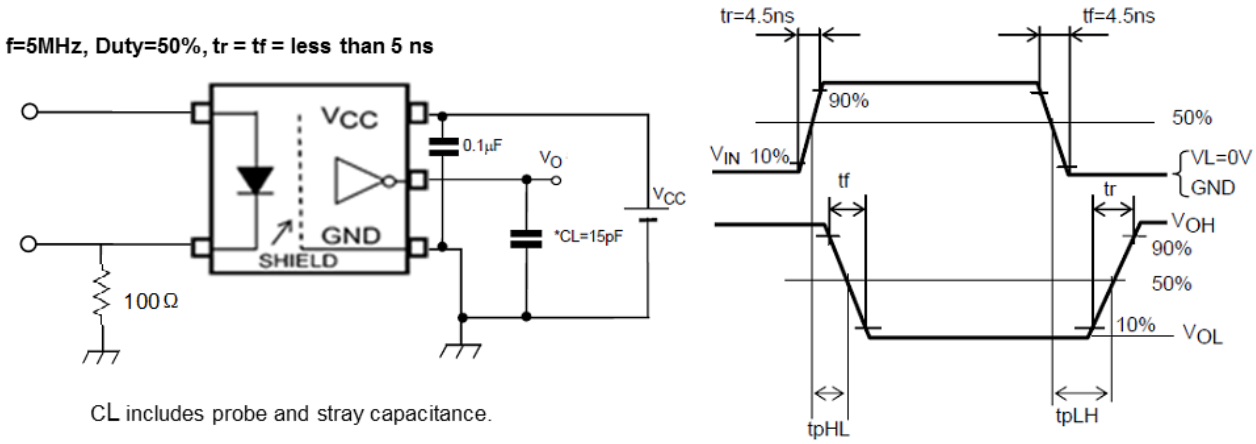
Note 4: CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.4 V).

Test Circuit 1: t_{pHL}, t_{pLH}, $|t_{pHL}-t_{pLH}|$



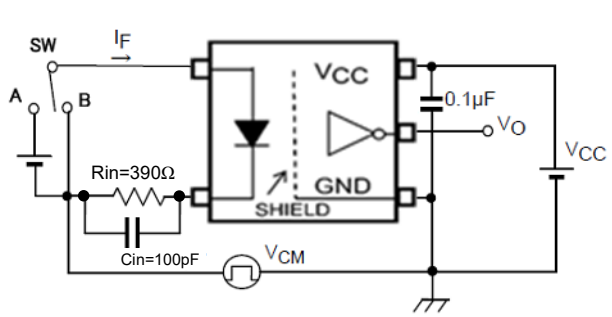
C_L includes probe and stray capacitance.

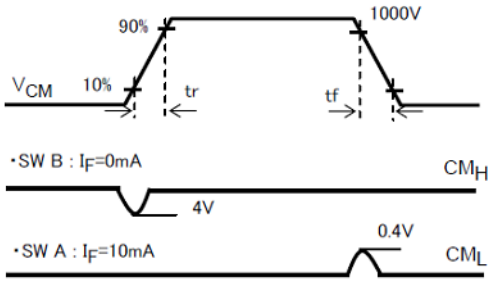
Test Circuit 2: t_{pHL}, t_{pLH}, $|t_{pHL}-t_{pLH}|$



CL includes probe and stray capacitance.

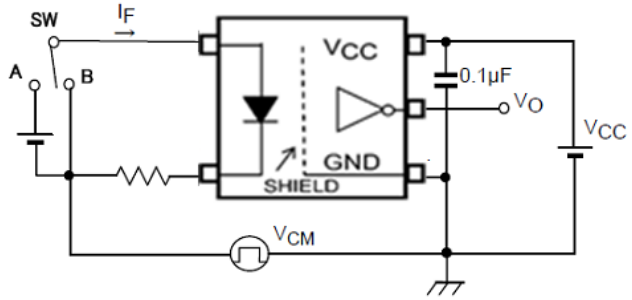
Test Circuit 3: CM_H, CM_L

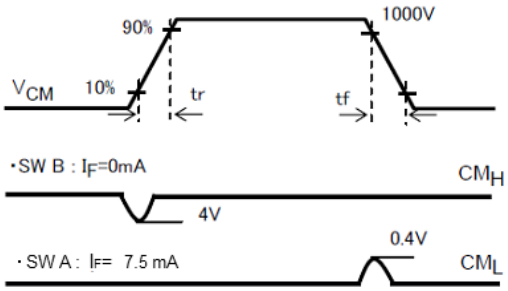




$$CM_H = \frac{800(V)}{tr(\mu s)} \qquad CM_L = -\frac{800(V)}{tf(\mu s)}$$

Test Circuit 4: CM_H, CM_L

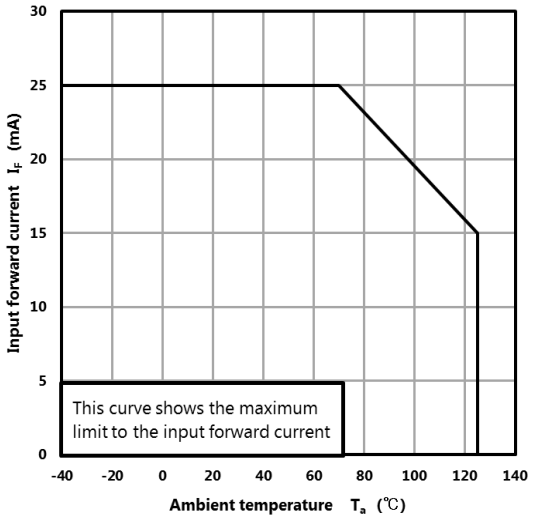




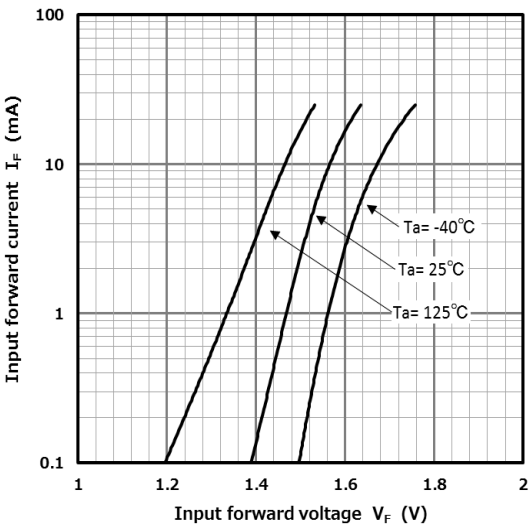
$$CM_H = \frac{800(V)}{tr(\mu s)} \qquad CM_L = -\frac{800(V)}{tf(\mu s)}$$

Characteristics Curves (Note)

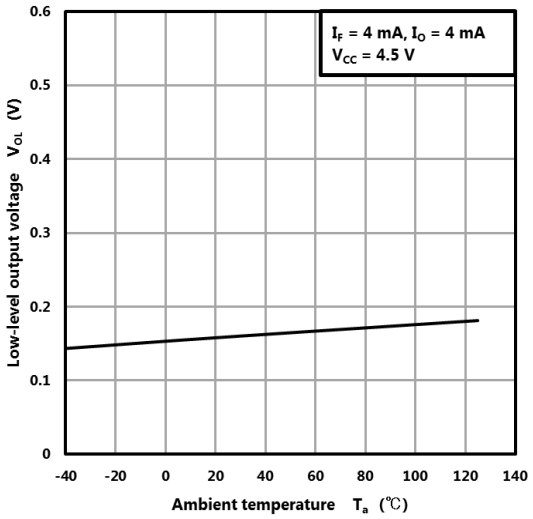
IF – Ta



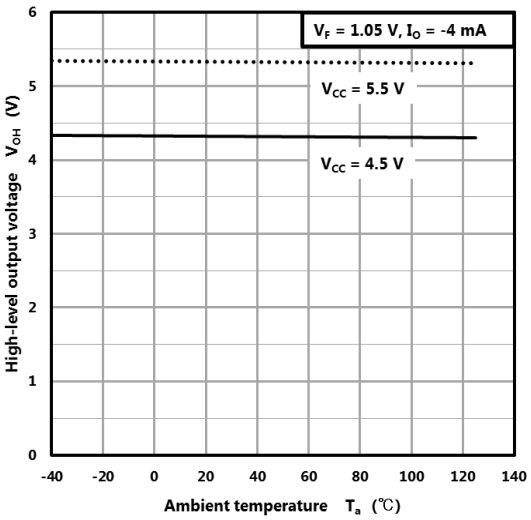
IF – VF



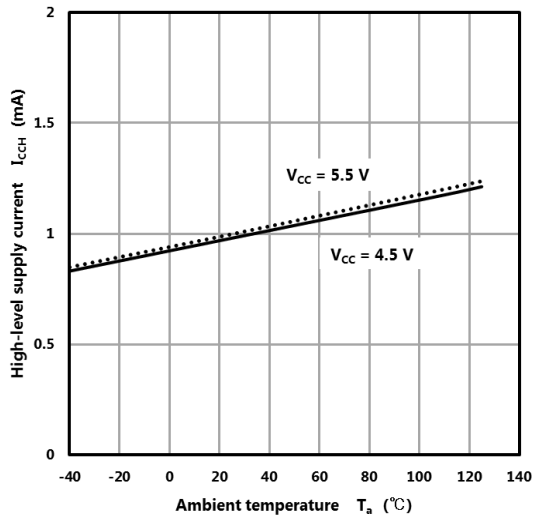
VOL – Ta



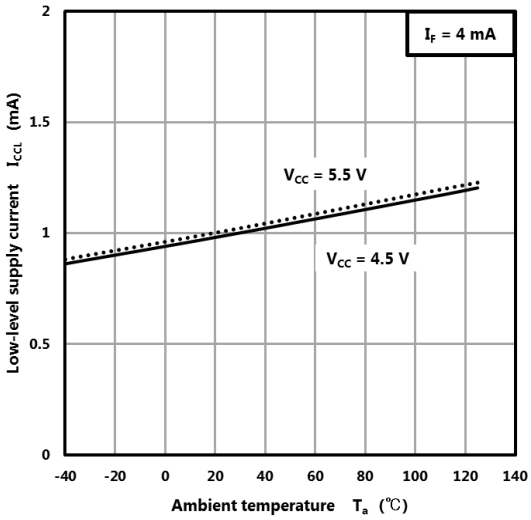
VOH – Ta



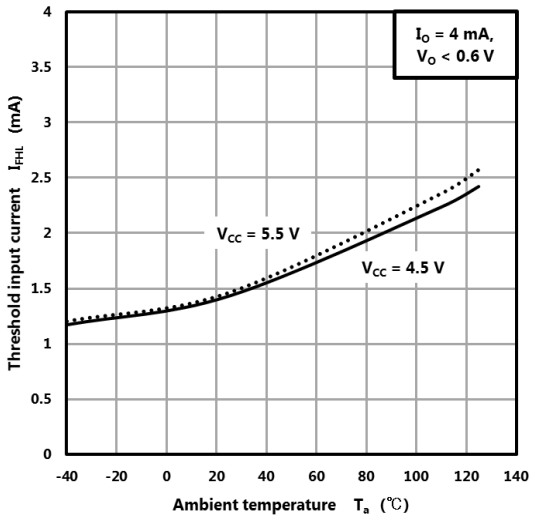
ICCH – Ta



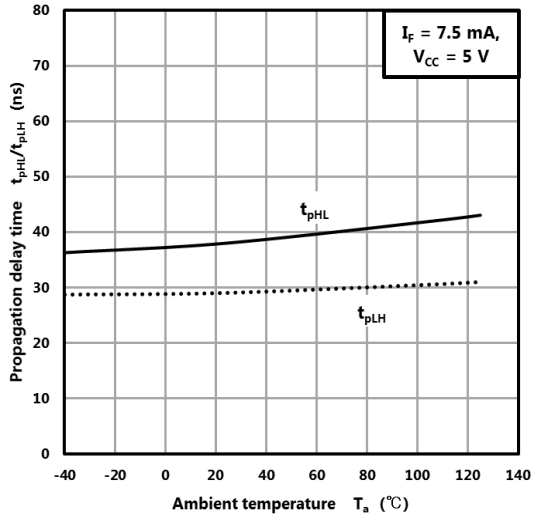
ICCL – Ta



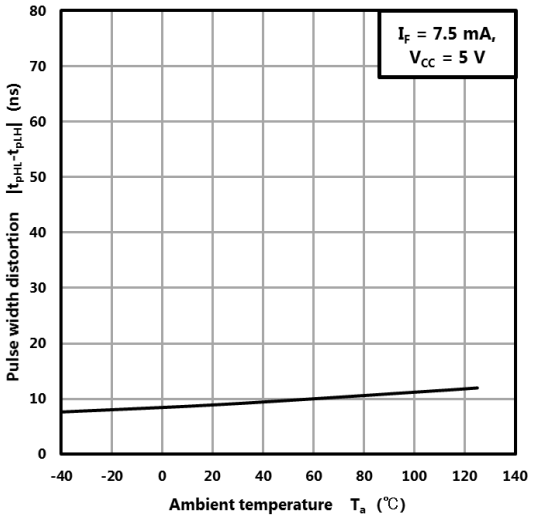
IFHL – Ta



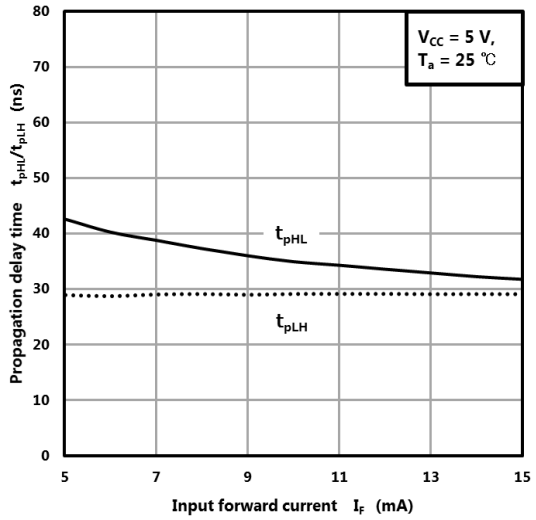
tpHL / tpLH – Ta



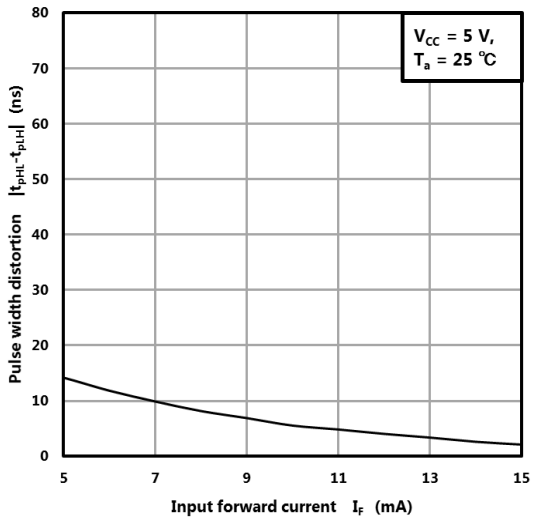
|tpHL-tpLH| – Ta



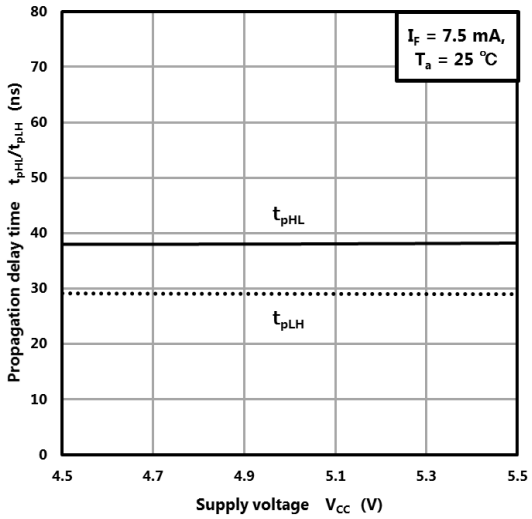
tpHL / tpLH – IF



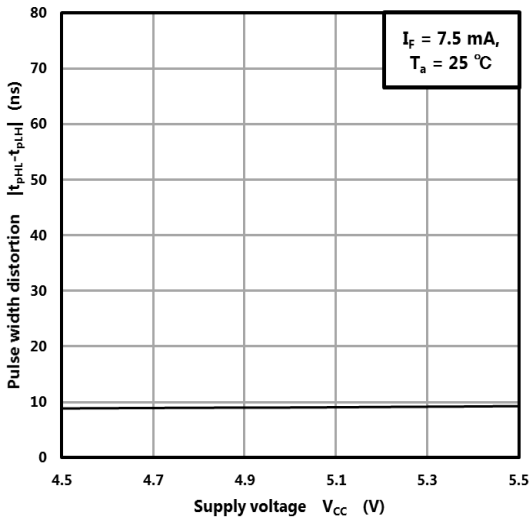
|tpHL-tpLH| – IF



tpHL / tpLH – VCC



|tpHL-tpLH| – VCC



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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