












CMOS Digital Integrated Circuit Silicon Monolithic

TMPM3H Group(1)

General Description

- Arm® Cortex®-M3 core. Operation frequency: 1 to 40 MHz.
Operation voltage: 2.7 to 5.5V
- Code flash: 32 to 128KB. Data flash: 8 to 32KB.
- Package: 32-pin to 100-pin. 11 types of packages are available.

| | | | |
|---|---------|---------|--------------|
|  | VQFN48 | 6x6mm | 0.4mm pitch |
|  | LQFP32 | 7x7mm | 0.8mm pitch |
|  | LQFP48 | 7x7mm | 0.5mm pitch |
|  | LQFP44 | 10x10mm | 0.8mm pitch |
|  | LQFP52 | 10x10mm | 0.65mm pitch |
|  | LQFP64 | 10x10mm | 0.5mm pitch |
|  | LQFP64 | 14x14mm | 0.8mm pitch |
|  | LQFP80 | 12x12mm | 0.5mm pitch |
|  | LQFP80 | 14x14mm | 0.65mm pitch |
|  | LQFP100 | 14x14mm | 0.5mm pitch |
|  | QFP100 | 14x20mm | 0.65mm pitch |

Applications

Widely used for consumer products and industrial products including home appliances, OA equipment, household equipment, AV devices, and motor control devices.

Features

- Arm Cortex-M3 core
 - Operation frequency: 1 to 40 MHz
 - Memory Protection Unit (MPU)
- Low-power consumption mode
 - Operation voltage: 2.7 to 5.5V
 - 100µA/MHz (at basic operation)
 - Low-power consumption operation: IDLE, STOP1, STOP2
- Operation temperature: -40 to +85°C
- Internal memory
 - Code flash: 32 to 128 KB, rewritable up to 10,000 times
 - Data flash: 8 to 32 KB, rewritable up to 100,000 times
 - Data flash is rewritable in parallel with instruction execution
 - RAM: 6 to 16KB and Backup RAM 2 KB
- Clock
 - External high-speed oscillator: 6 MHz to 12 MHz(Ceramic, Crystal)
 - External high-speed clock input: 6 to 20 MHz
 - Internal high-speed oscillator (IHOSC1): 10 MHz, user trimming function
 - PLL: 40 MHz output
 - External low-speed oscillator: 32.768kHz
- Oscillation frequency detection (OFD): Abnormal system clock detection
- Low-Voltage Detection (LVD): 8 level, Generate interrupts and reset outputs
- Interruption
 - External: 6 to 16 factors, with DNF
 - internal: 85 to 100 factors
- I/O ports: GPIO:24 to 87(Input:2 to 4,Output:1)
 - pull-up/-down resistor, Open-drain, 5V-tolerant
- On chip Debug(JTAG/SW)
- Trigger Selector(TRGSEL)
 - Expand Trigger request for DMAC, Timer, others
- DMA Controller(DMAC)
 - DMA requests: 32 factors, internal/external triggers
- Asynchronous Serial Interface(UART): 2 to 3 channels
 - 2.5Mbps(Max),FIFO(Send 8stage, Receive 8stage)
- Serial Peripheral Interface(TSPI): 1 to 2 channels
 - SIO/SPI mode,20Mbps(MAX),FIFO(Send 16bitsx8,Receive 16bitsx8)
- I²C Interface(I²C):1 to 3 channels
 - Multi Master, Fm+, Release function for Low Power Mode
- 8-bit DA converter(DAC): 0 to 2 channels
- 12-bit ADC(ADC): 4 to 16 channel inputs
 - Sample-and-hold circuit
 - Conversion time: 1.5µs@40MHz
 - Self-diagnosis support function
- Motor control circuit (PMD+): 1 channel
 - 3 phase PWM output, Synchronized with 12-bit ADC
 - Emergency stop function by external inputs (EMG_N pin, OVV_N pin)
- Advanced Encoder input circuit (A-ENC): 1 channel
 - Encoder/sensor (3 types)/Timer /Phase counter mode
- 32bit Timer Event Counter (T32A)
 - 12 channels as 16-bit Timers:6 channels as 32-bits Timers
 - Interval Timer, event counter, input capture, phase difference input, PPG output, Sync Start, Trigger Start
- Realtime Clock (RTC): 0 to 1 channel
- Watchdog timer (SIWDT): 1 channel
 - Clock system other than the system clock can be selected,
 - Clear window, interrupts and reset output
- Remote controller reception circuit (RMC): 1 channel
- Supports boundary scan(BSC)

Start of commercial production
2017-06

Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, Please contact your sales representative.

Table 1 Products Lists (1)

| Built-in Functions | | TMPM3H6FWFG TMPM3H6FUFG TMPM3H6FSFG | TMPM3H6FDFG TMPM3H6FUDFG TMPM3H6FSDFG | TMPM3H5FWFG TMPM3H5FUFG TMPM3H5FSFG | TMPM3H5FDFG TMPM3H5FUDFG TMPM3H5FSDFG | TMPM3H4FWUG TMPM3H4FUUG TMPM3H4FSUG | TMPM3H4FWFG TMPM3H4FUFG TMPM3H4FSFG |
|-------------------------------------|-----------------------|---|---|---|---|---|---|
| Memory | Code Flash (KB) | 128 | 128 | 128 | 128 | 128 | 128 |
| | | 96 | 96 | 96 | 96 | 96 | 96 |
| | | 64 | 64 | 64 | 64 | 64 | 64 |
| | Data Flash (KB) | 32 | 32 | 32 | 32 | 32 | 32 |
| 32 | | 32 | 32 | 32 | 32 | 32 | |
| 16 | | 16 | 16 | 16 | 16 | 16 | |
| RAM (KB) | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| | 12 | 12 | 12 | 12 | 12 | 12 | 12 |
| | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Backup RAM (KB) | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| I/O port | PORT (Pin) | 87 | 87 | 67 | 67 | 53 | 53 |
| External interrupt | INT (Pin) | 16 | 16 | 15 | 15 | 11 | 11 |
| DMA | DMAC (Ch) | 32 | 32 | 32 | 32 | 32 | 32 |
| Timer function | T32A (Ch) | 6 | 6 | 6 | 6 | 6 | 6 |
| | RTC (Ch) | 1 | 1 | 1 | 1 | 1 | 1 |
| Serial communication function | UART (Ch) | 3 | 3 | 3 | 3 | 3 | 3 |
| | I ² C (Ch) | 3 | 3 | 3 | 3 | 3 | 3 |
| | TSPI (Ch) | 2 | 2 | 2 | 2 | 2 | 2 |
| Analog function | 12-bit ADC (Ch) | 16 | 16 | 10 | 10 | 8 | 8 |
| | 8-bit DAC (Ch) | 2 | 2 | 2 | 2 | 1 | 1 |
| Motor Control peripherals | A-ENC (Ch) | 1 | 1 | 1 | 1 | 1 | 1 |
| | PMD+ (Ch) | 1 | 1 | 1 | 1 | 1 | 1 |
| Remote Control Receiver peripherals | RMC (Ch) | 1 | 1 | 1 | 1 | 1 | 1 |
| System function | LVD (Ch) | 1 | 1 | 1 | 1 | 1 | 1 |
| | SIWDT (Ch) | 1 | 1 | 1 | 1 | 1 | 1 |
| | OFD (Ch) | 1 | 1 | 1 | 1 | 1 | 1 |
| | POR | 1 | 1 | 1 | 1 | 1 | 1 |
| Debug interface | Debug | JTAG/SW/ TRACE | JTAG/SW | JTAG/SW | JTAG/SW | JTAG/SW | JTAG/SW |
| BSC | | 1 | 1 | 1 | 1 | 1 | 1 |
| Package | Package type | LQFP100 (14mm x 14mm, 0.5 mm pitch) | QFP100 (14mm x 20mm, 0.65 mm pitch) | LQFP80 (12mm x 12mm, 0.5 mm pitch) | LQFP80 (14mm x 14mm, 0.65 mm pitch) | LQFP64 (10mm x 10mm, 0.5 mm pitch) | LQFP64 (14mm x 14mm, 0.8 mm pitch) |
| | Package name | LQFP100-P-1414 -0.50H | P-QFP100-1420 -0.65-001 | LQFP80-P-1212 -0.50F | P-LQFP80-1414 -0.65-001 | LQFP64-P-1010 -0.50E | P-LQFP64-1414 0.80-002 |

Table 2 Products Lists (2)

| Built-in functions | | TMPM3H3FWUG TMPM3H3FUUG TMPM3H3FSUG | TMPM3H2FWDUG TMPM3H2FUDUG TMPM3H2FSDUG | TMPM3H2FWQG TMPM3H2FUQG TMPM3H2FSQG | TMPM3H1FWUG TMPM3H1FUUG TMPM3H1FSUG TMPM3H1FPUG | TMPM3H0FSDUG TMPM3H0FMDUG |
|-------------------------------------|-----------------------|---|--|---|--|--|
| Memory | Code Flash (KB) | 128 96 64 | 128 96 64 | 128 96 64 | 128 96 64 48 | 64 32 |
| | Data Flash (KB) | 32 32 16 | 32 32 16 | 32 32 16 | 32 32 16 8 | 16 8 |
| | RAM (KB) | 16 12 8 | 16 12 8 | 16 12 8 | 16 12 8 6 | 8 6 |
| | Backup RAM (KB) | 2 | 2 | 2 | 2 | 2 |
| I/O port | PORT (Pin) | 43 | 40 | 40 | 36 | 24 |
| External interrupt | INT (Pin) | 8 | 7 | 7 | 6 | 6 |
| DMA | DMAC (Ch) | 32 | 30 | 30 | 30 | 24 |
| Timer function | T32A (Ch) | 6 | 6 | 6 | 6 | 6 |
| | RTC (Ch) | 1 | 1 | 1 | 0 | 0 |
| Serial communication function | UART (Ch) | 3 | 3 | 3 | 3 | 2 |
| | I ² C (Ch) | 3 | 2 | 2 | 2 | 1 |
| | TSPI (Ch) | 2 | 2 | 2 | 2 | 1 |
| Analog function | 12-bit ADC (Ch) | 8 | 8 | 8 | 8 | 4 |
| | 8-bit DAC (Ch) | 1 | 1 | 1 | 0 | 0 |
| Motor Control peripherals | A-ENC (Ch) | 1 | 1 | 1 | 1 | 1 |
| | PMD+ (Ch) | 1 | 1 | 1 | 1 | 1 |
| Remote Control Receiver peripherals | RMC (Ch) | 1 | 1 | 1 | 1 | 1 |
| System function | LVD (Ch) | 1 | 1 | 1 | 1 | 1 |
| | SIWDT (Ch) | 1 | 1 | 1 | 1 | 1 |
| | OFD (Ch) | 1 | 1 | 1 | 1 | 1 |
| | POR | 1 | 1 | 1 | 1 | 1 |
| Debug interface | Debug | JTAG/SW | JTAG/SW | JTAG/SW | JTAG/SW | SW |
| BSC | | 1 | 0 | 0 | 0 | 0 |
| Package | Package type | LQFP52 (10mm x 10mm, 0.65 mm pitch) | LQFP48 (7mm x 7mm, 0.5 mm pitch) | VQFN48 (6mm x 6mm, 0.4 mm pitch) | LQFP44 (10mm x 10mm, 0.8 mm pitch) | LQFP32 (7mm x 7mm, 0.8 mm pitch) |
| | Package name | P-LQFP52-1010 -0.65-001 | LQFP48-P-0707 -0.50C | P-VQFN48-0606 -0.40-003 | LQFP44-P-1010 -0.80A | P-LQFP32-0707 -0.80-002 |

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Preface

Conventions

- Numeric formats follow the rules as shown below:
 - Hexadecimal: 0xABC
 - Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
 - Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
Example: S[3:0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by [] defines the register.
Example: [ABCD]
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
Example: [XYZ1], [XYZ2], [XYZ3] → [XYZn]
- "x" substitutes suffix number or character of units and channels in the Register List.
 - In case of unit, "x" means A, B, and C . . .
 - Example: [ADACR0], [ADBCR0], [ADCCR0] → [ADxCR0]
 - In case of channel, "x" means 0, 1, and 2 . . .
 - Example: [T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]
- The bit range of a register is written like as [m: n].
Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
Example: [ABCD]<EFG> = 0x01 (hexadecimal), [XYZn]<VW> = 1 (binary)
- Word and Byte represent the following bit length.
 - Byte: 8 bits
 - Half word: 16 bits
 - Word: 32 bits
 - Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
 - R: Read only
 - W: Write only
 - R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

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All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

The following words are terms or abbreviations mainly used in this datasheet.

| | |
|-------------------|---|
| ADC | Analog to Digital Converter |
| A-ENC | Advanced Encoder Input Circuit |
| BSC | Boundary Scan |
| DAC | Digital to Analog Converter |
| DMAC | Direct Memory Access Controller |
| DNF | Digital Noise Filter |
| ELOSC | External Low Speed Oscillator |
| EHOSC | External High Speed Oscillator |
| Fm+ | I ² C Fast Mode Plus |
| IHOSC | Internal High Speed Oscillator |
| INT | Interrupt |
| I ² C | Inter-Integrated Circuit |
| I ² CS | I ² C wake-up circuit from Stand-by mode |
| LVD | Voltage Detection Circuit |
| NMI | Non-Maskable Interrupt |
| OFD | Oscillation Frequency Detector |
| PMD+ | Programmable Motor Control Circuit Plus |
| POR | Power On Reset Circuit |
| RMC | Remote Control Signal Preprocessor |
| RTC | Real Time Clock |
| SIWDT | Clock Selective Watchdog Timer |
| TRGSEL | Trigger Selection Circuit |
| TSPI | Toshiba Serial Peripheral Interface |
| T32A | 32-bit Timer Event Counter |
| UART | Universal Asynchronous Receiver Transmitter |

1. Block Diagram

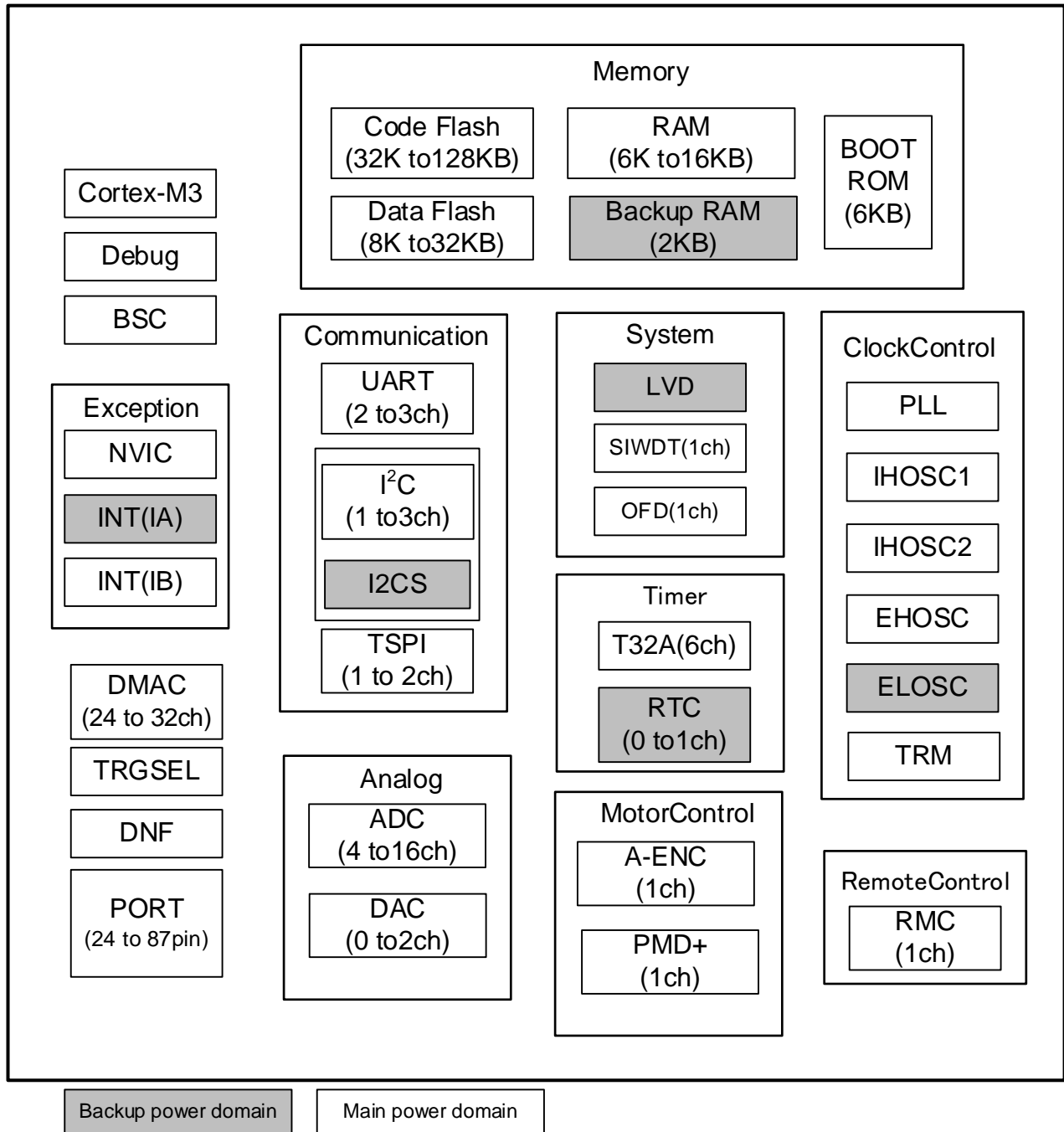
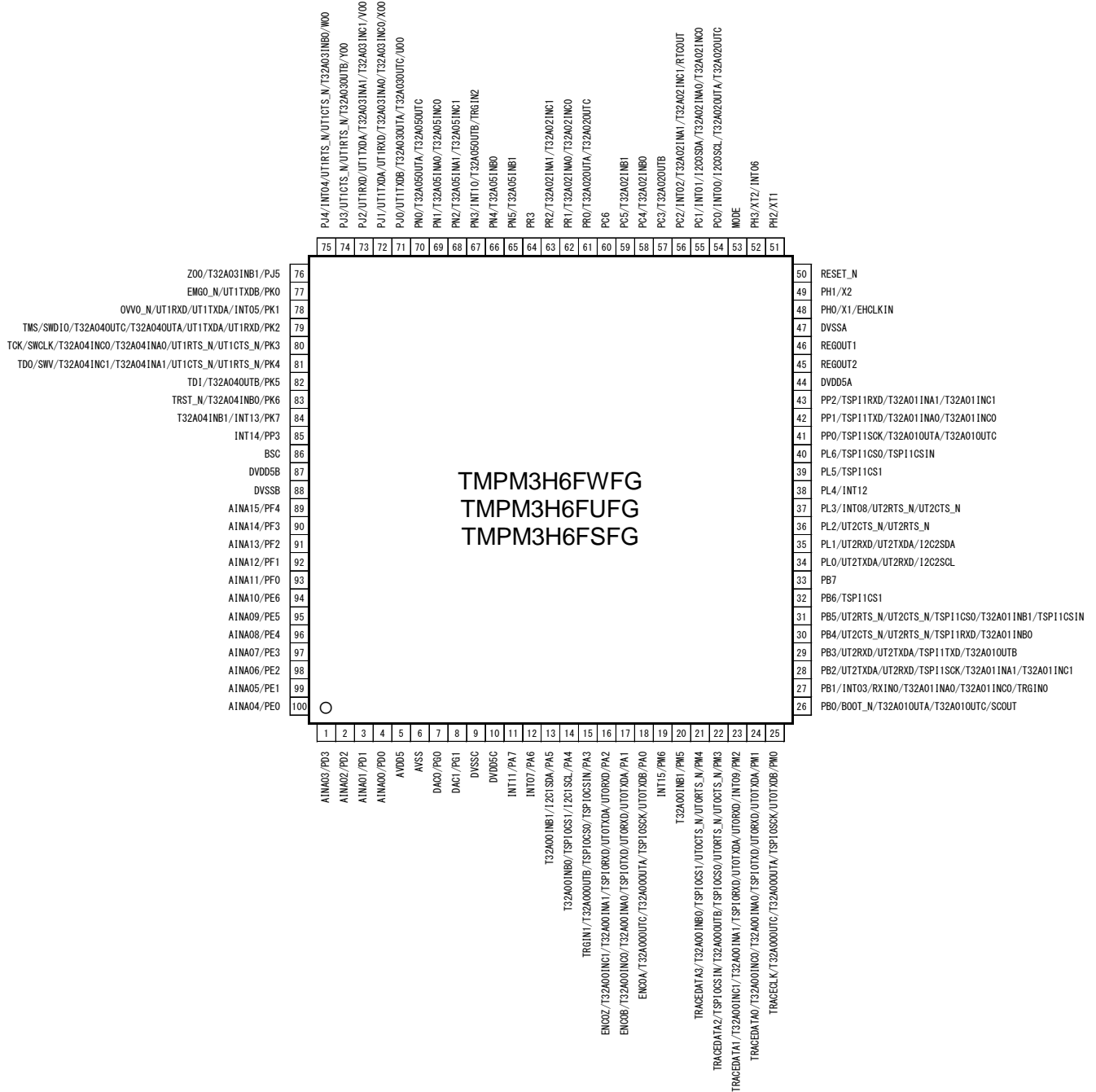


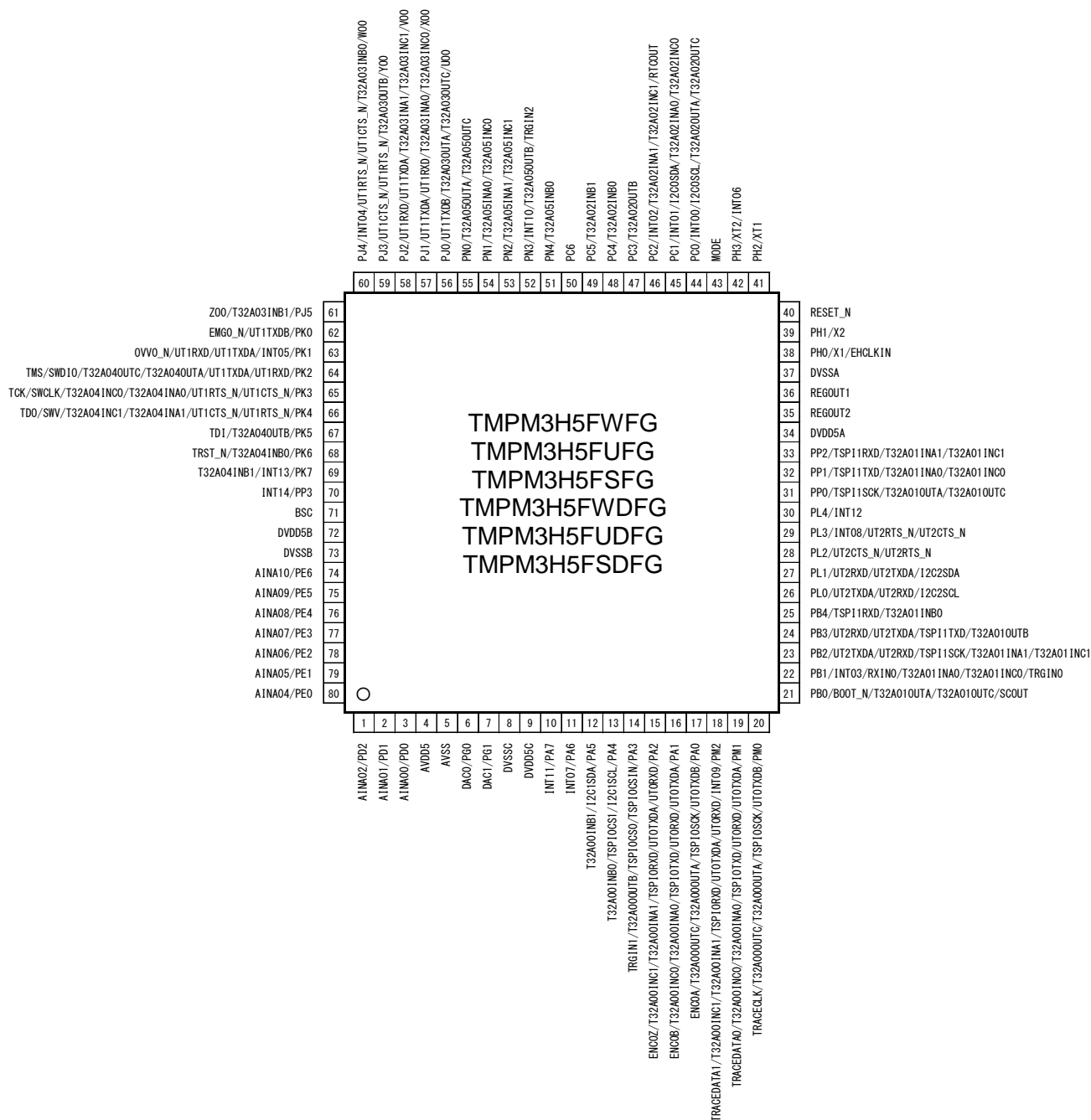
Figure 1.1 Block diagram of the TMPM3H Group(1)

2. Pin Assignment

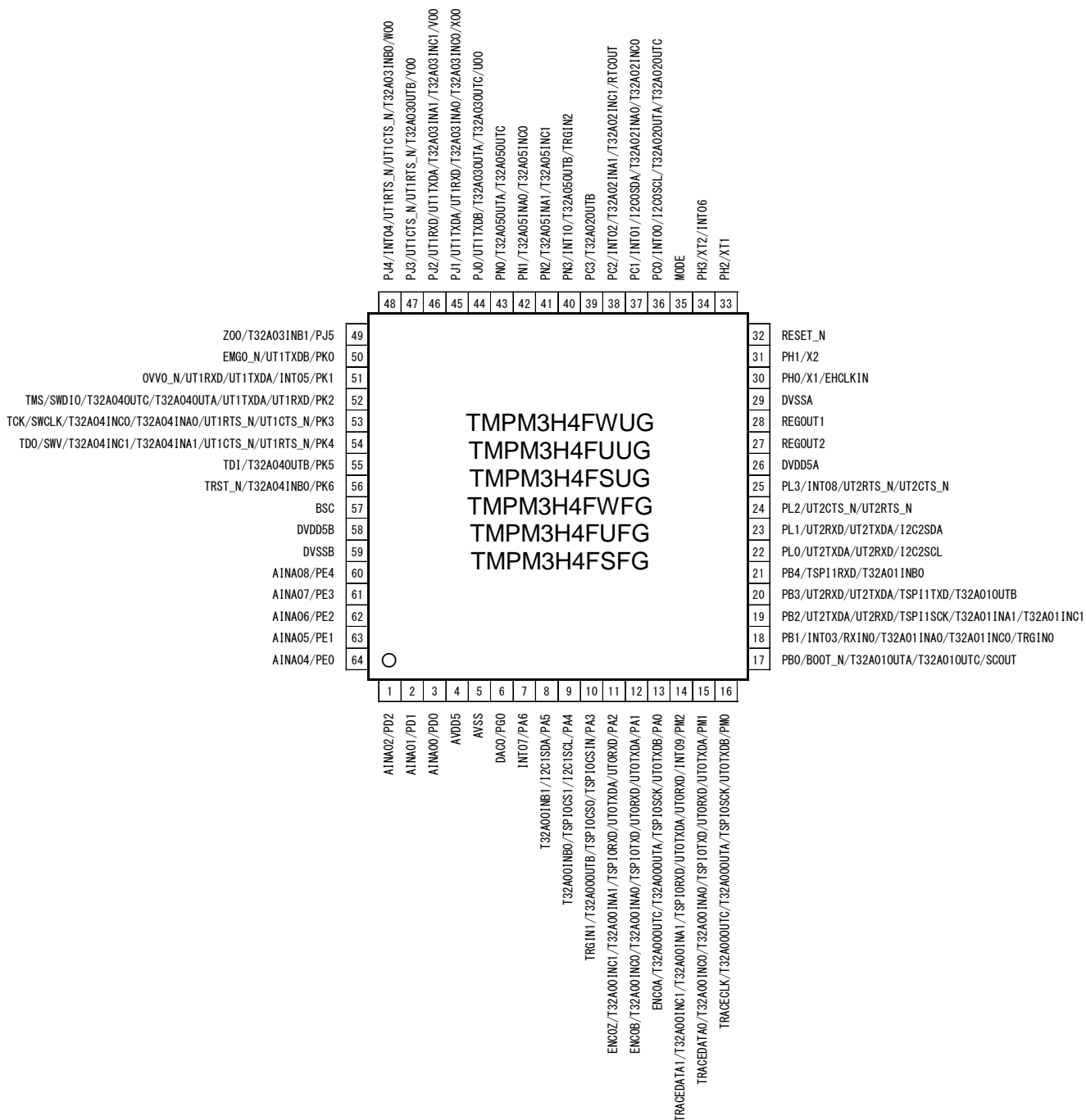
2.1. LQFP100



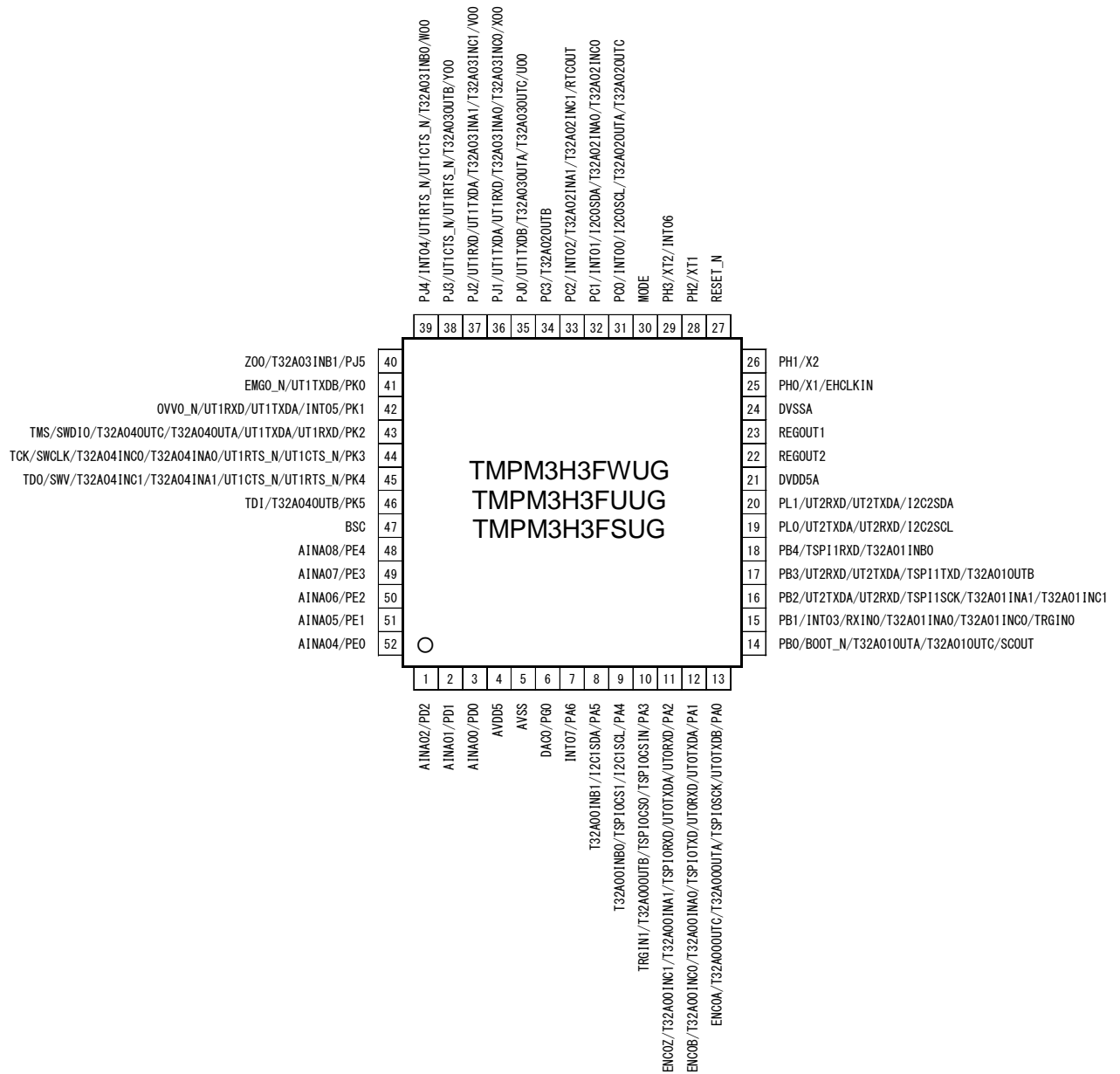
2.3. LQFP80



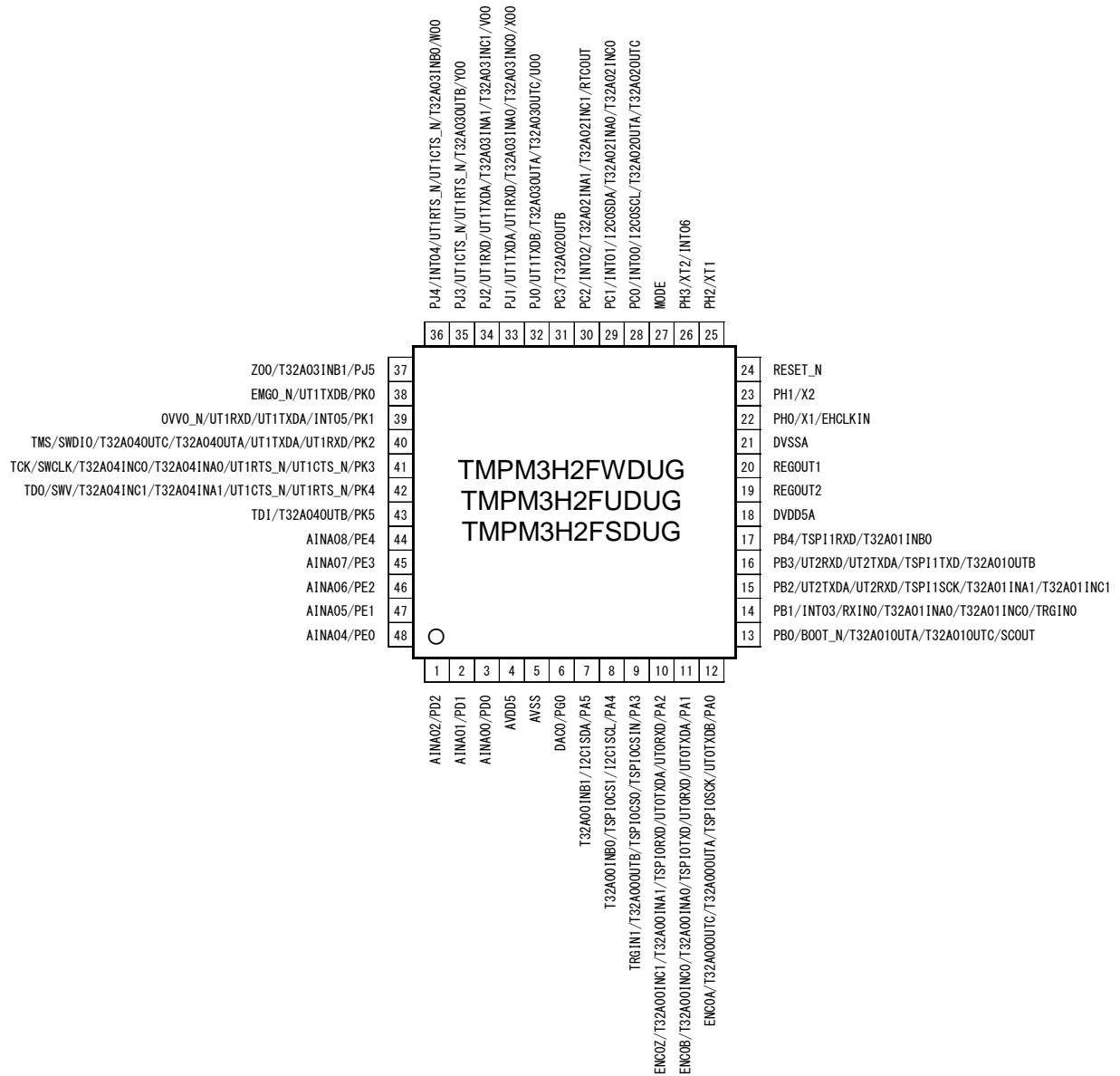
2.4. LQFP64



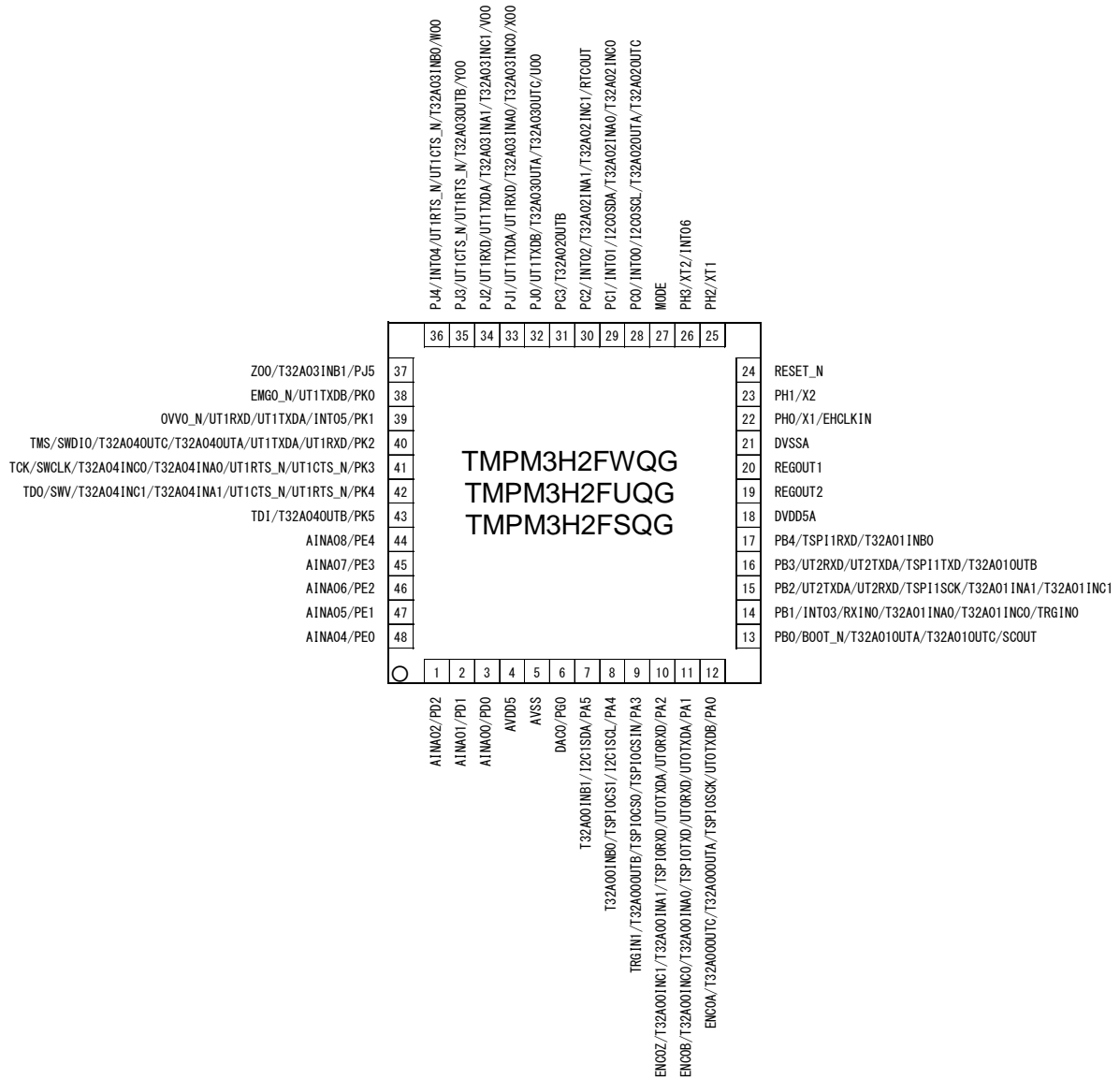
2.5. LQFP52



2.6. LQFP48



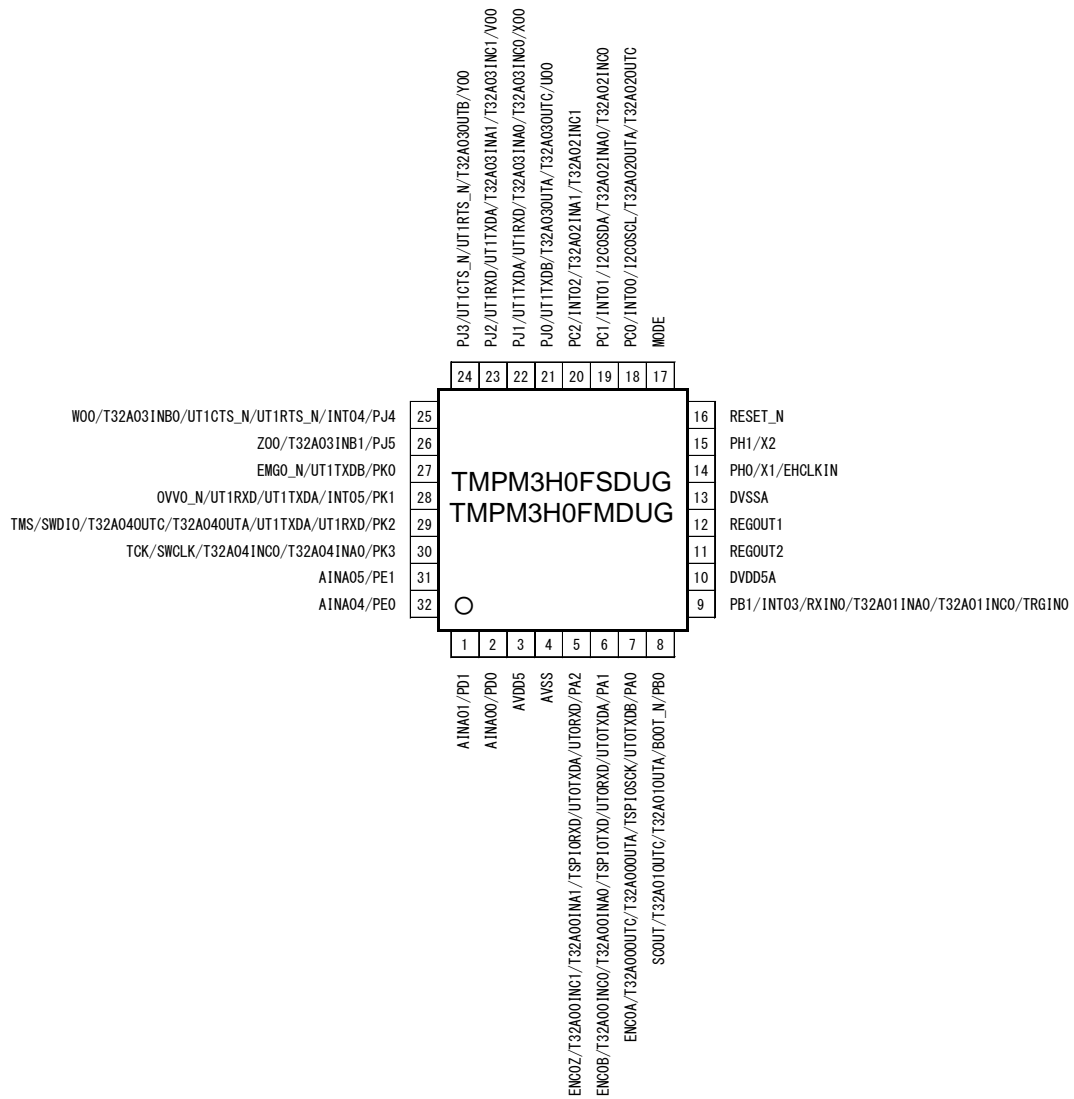
2.7. VQFN48



2.8. LQFP44



2.9. LQFP32



3. Memory Map

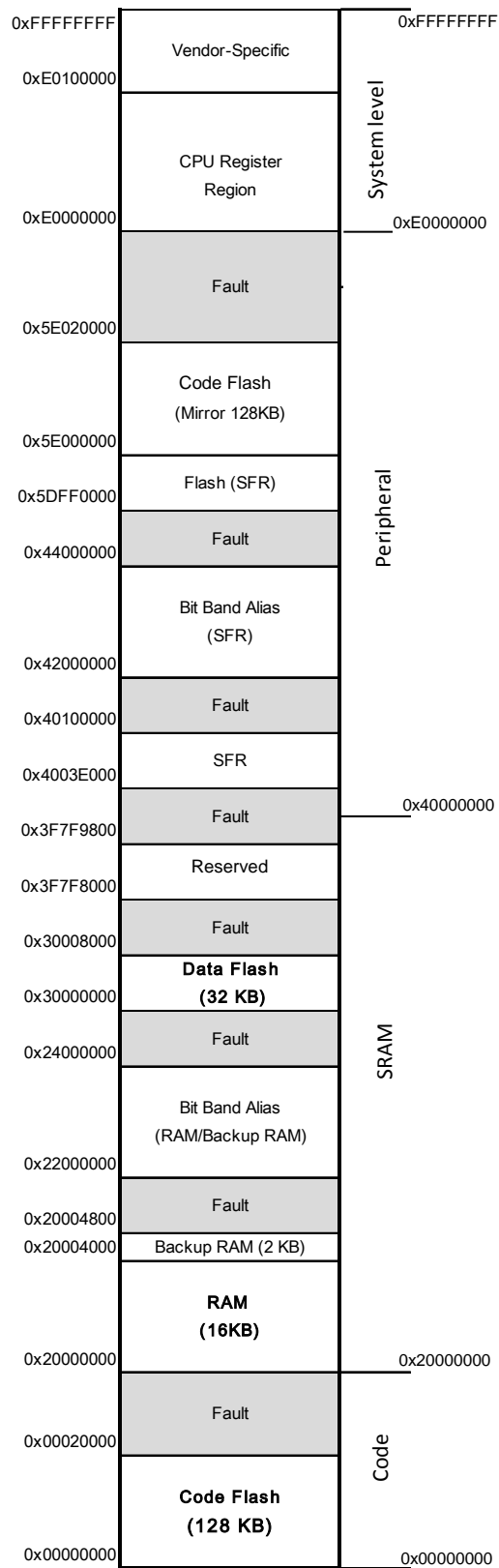


Figure 3.1 Example of the TPM3H6FW

3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

| Products | | | TMPM3H6FWFG TMPM3H6FWDFG TMPM3H5FWFG TMPM3H5FWDFG TMPM3H4FWFG TMPM3H4FWUG TMPM3H3FWUG TMPM3H2FWDUG TMPM3H2FWQG TMPM3H1FWUG | TMPM3H6FUFG TMPM3H6FUDFG TMPM3H5FUFG TMPM3H5FUDFG TMPM3H4FUFG TMPM3H4FUUG TMPM3H3FUUG TMPM3H2FUDUG TMPM3H2FUQG TMPM3H1FUUG | TMPM3H6FSFG TMPM3H6FSDFG TMPM3H5FSFG TMPM3H5FSDFG TMPM3H4FSFG TMPM3H4FSUG TMPM3H3FSUG TMPM3H2FSDFG TMPM3H2FSQG TMPM3H1FSUG TMPM3H0FSDFG | TMPM3H1FPUG | TMPM3H0FMDUG |
|-------------------|---------------------|-------|---|---|---|-------------|--------------|
| Peripheral region | Code Flash (Mirror) | Size | 128KB | 96KB | 64KB | 48KB | 32KB |
| | | START | 0x5E000000 | 0x5E000000 | 0x5E000000 | 0x5E000000 | 0x5E000000 |
| | | END | 0x5E01FFFF | 0x5E017FFF | 0x5E00FFFF | 0x5E00BFFF | 0x5E007FFF |
| SRAM region | Data Flash | Size | 32 KB | | 16 KB | 8 KB | |
| | | START | 0x30000000 | | 0x30000000 | 0x30000000 | |
| | | END | 0x30007FFF | | 0x30003FFF | 0x30001FFF | |
| | Backup RAM | Size | 2 KB | | | | |
| | | START | 0x20004000 | | | | |
| | | END | 0x200047FF | | | | |
| | RAM | Size | 16 KB | 12 KB | 8 KB | 6 KB | 6 KB |
| | | START | 0x20000000 | 0x20000000 | 0x20000000 | 0x20000000 | 0x20000000 |
| | | END | 0x20003FFF | 0x20002FFF | 0x20001FFF | 0x200017FF | 0x200017FF |
| Code Region | Code Flash | Size | 128 KB | 96 KB | 64 KB | 48 KB | 32 KB |
| | | START | 0x00000000 | 0x00000000 | 0x00000000 | 0x00000000 | 0x00000000 |
| | | END | 0x0001FFFF | 0x00017FFF | 0x0000FFFF | 0x0000BFFF | 0x00007FFF |

4. Pin Description

4.1. Functional Pin Name and Their Functions

4.1.1. Peripheral Function Pins

Table 4.1 Pin names and functions of peripheral pins

| Peripheral function | Pin name | Input or Output | Function |
|--|-----------|-----------------|--|
| Clock/Mode control (CG) | SCOUT | Output | Output pin for the system clock |
| Interrupt control (IA/IB) | INTx | Input | External interrupt input pin External input pin provides the noise filter (filter width: typ. 30 ns). |
| 32-bit Timer event counter (T32A) | T32AxINA0 | Input | 16-bit timer A input capture input pin 0 |
| | T32AxINA1 | Input | 16-bit timer A input capture input pin 1 |
| | T32AxOUTA | Output | 16-bit timer A output pin |
| | T32AxINB0 | Input | 16-bit timer B input capture input pin 0 |
| | T32AxINB1 | Input | 16-bit timer B input capture input pin 1 |
| | T32AxOUTB | Output | 16-bit timer B output pin |
| | T32AxINC0 | Input | 32-bit timer input capture input pin 0 |
| | T32AxINC1 | Input | 32-bit timer input capture input pin 1 |
| | T32AxOUTC | Output | 32-bit timer output pin |
| Serial peripheral interface (TSPI) | TSPIxCSIN | Input | Chip select input pin |
| | TSPIxCS0 | Output | Chip select output pin 0 |
| | TSPIxCS1 | Output | Chip select output pin 1 |
| | TSPIxRXD | Input | Data input pin |
| | TSPIxTXD | Output | Data output pin |
| | TSPIxSCK | I/O | Clock input/output pin |
| Asynchronous serial communication circuit (UART) | UTxRXD | Input | Data input |
| | UTxTXDA | Output | Data output pin A |
| | UTxTXDB | Output | Data output pin B |
| | UTxCTS_N | Input | Clear to send signal pin |
| | UTxRTS_N | Output | Request to send signal pin |
| I ² C interface (I ² C) | I2CxSDA | I/O | Data input/output pin |
| | I2CxSCL | I/O | Clock input/output pin |

| | | | |
|--|--------|--------|-------------------------------------|
| Motor control circuit (PMD+) | EMGx_N | Input | Emergency state detection input pin |
| | OVVx_N | Input | Over voltage detection input |
| | UOx | Output | U-phase output pin |
| | VOx | Output | V-phase output pin |
| | WOx | Output | W-phase output pin |
| | XOx | Output | X-phase output pin |
| | YOx | Output | Y-phase output pin |
| | ZOx | Output | Z-phase output pin |
| Encoder input circuit (A-ENC) | ENCxA | Input | Encoder input |
| | ENCxB | Input | Encoder input |
| | ENCxZ | Input | Encoder input |
| Analog-to-digital converter (ADC) | AINAx | Input | Analog input pin |
| Digital-to- analog converter (DAC) | DACx | Output | DAC output pin |
| Trigger input | TRGINx | Input | External trigger input pin |
| Remote signaling receive circuit (RMC) | RXINx | Input | Remote Signaling Data input pin |
| Real time clock (RTC) | RTCOUT | Output | 1Hz clock output pin |

Note: "x" means channel number or unit number or interrupt number.

4.1.2. Debug Pins

Table 4.2 Debug pin names and their function

| Debug Port | Pin name | Input or Output | Function |
|------------|------------|-----------------|------------------------------------|
| JTAG | TMS | Input | JTAG test mode selection input pin |
| | TCK | Input | JTAG serial clock input pin |
| | TDO | Output | JTAG serial data output pin |
| | TDI | Input | JTAG serial data input pin |
| | TRST_N | Input | JTAG test reset input pin |
| SW | SWDIO | I/O | Serial wire data input/output pin |
| | SWCLK | Input | Serial wire clock input pin |
| | SWV | Output | Serial wire viewer output pin |
| TRACE | TRACECLK | Output | Trace clock output pin |
| | TRACEDATA0 | Output | Trace data output pin 0 |
| | TRACEDATA1 | Output | Trace data output pin 1 |
| | TRACEDATA2 | Output | Trace data output pin 2 |
| | TRACEDATA3 | Output | Trace data output pin 3 |

4.1.3. Control Pins

Table 4.3 Control pin names and their function

| | Pin name | Input or Output | Function |
|-------------|----------|-----------------|--|
| Control Pin | X1 | Input | High-speed oscillator connection pin |
| | X2 | Output | High-speed oscillator connection pin |
| | XT1 | Input | Low-speed oscillator connection pin |
| | XT2 | Output | Low-speed oscillator connection pin |
| | EHCLKIN | Input | External Clock signal input pin |
| | BOOT_N | Input | BOOT mode control pin The BOOT mode control pin is sampled on the rising edge of the RESET_N input. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single boot mode. If it is "High", the MCU enters single chip mode. For details, refer to "Flash Memory" reference manual. |
| | RESET_N | Input | Reset signal input pin |
| | MODE | Input | Mode pin This pin must be fixed to the "Low" level. |
| | BSC | Input | Boundary scan mode control pin |

4.1.4. Power Supply Pins

Table 4.4 Power supply pin names and their function

| Function | Pin name | Function |
|--------------|--|--|
| Power Supply | DVDD5A (Note1) DVDD5B (Note1) DVDD5C (Note1) | Power supply pin for digital DVDD5A/B/C supplies the power to the following pins: PA to PC, PH to PR, MODE, RESET_N, BOOT_N, BSC A power supply is supplied to an oscillating circuit from a built-in regulator. X1,X2,XT1,XT2 |
| | DVSSA (Note2) DVSSB (Note2) DVSSC (Note2) | GND pin for digital |
| | REGOUT1 (Note3) | Capacitor for a regulator connection pin (Note4) |
| | REGOUT2 (Note3) | Capacitor for a regulator connection pin (Note4) |
| | AVDD5 | Power supply pin and reference power pin (VREFH) for analog are combination pins. AVDD5 supplies the power to the following pins: PD, PE, PF, PG |
| | AVSS | GND pin for analog, reference GND (VREFL) for analog are combination pins. |

Note1: Apply the voltage to DVDD5A, DVDD5B, and DVDD5C at the same potential except the case that the pins are not provided.

Note2: Apply the external voltage to DVSSA, DVSSB, and DVSSC at the same potential except the case that the pins are not provided.

Note3: For REGOUT1 and REGOUT2, do not cause a short circuit with DVDD5A, DVDD5B, or DVDD5C; or DVSSA, DVSSB, or DVSSC.

Note4: For the capacitor value, refer to the "Electrical Characteristics"

4.1.5. Capacitors between power supply pins

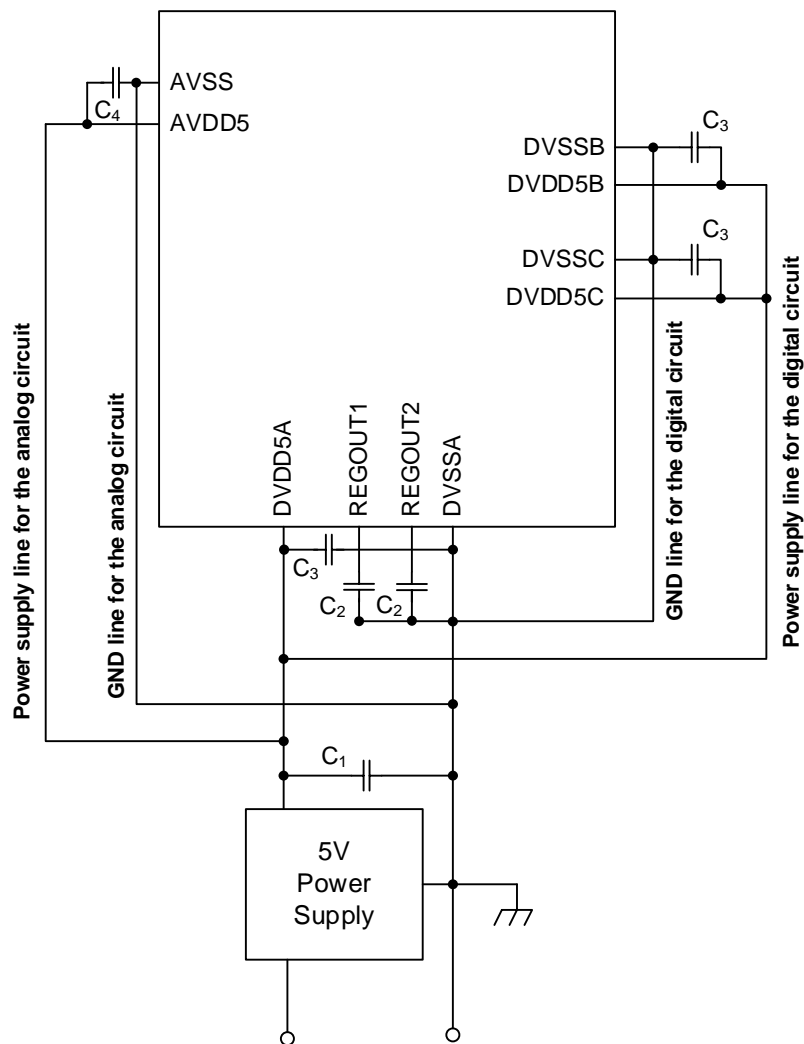


Figure 4.1 Capacitors between power supply pins

Note1: 5V power supply output capacitor (C₁: min 1 μF) must be placed on the shortest distance from the output pin of 5V power supply. Ceramic capacitor recommended for C₁.

Note2: Bypass capacitor must be placed between the 5V power supply and GND near each MCU power supply pin.(C₃,C₄:0.01 to 0.1μF)

Note3: Power stabilizing Capacitors of REGOUT1 and REGOUT2 for built-in regulators must be the same capacity(C₂:4.7μF), and ceramic capacitor recommended for C₂. They must be placed on the shortest distance from DVSSA.

Note4: Separate the analog power supply line and the digital power supply line near the 5V power supply output pin in order to reduce noise mixing into the analog circuit from the digital power supply.

Note5: When inserting a filter circuit or pull-up / down resistor at the input / output pin of the analog power supply system to reduce noise mixing from the peripheral circuit to the analog circuit, connect the components that make up these circuits to the analog power supply line.

Note6: Do not separate the power supply line and the GND line from each other in order to reduce high frequency noise etc, received by the power supply line, the GND line, and the loop circuit of the capacitor.

4.2. Functional Pin and Ports Assignment (Pin Number)

Following table shows a pin number of the port assignment and each product which were seen from the functional pin.

"-" means that it does not have a pin or there is no assignment of a function.

Table 4.5 SCOUT

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| SCOUT | PB0 | 26 | 28 | 21 | 17 | 14 | 13 | 12 | 8 |

Table 4.6 INTx

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| INT00 | PC0 | 54 | 56 | 44 | 36 | 31 | 28 | 25 | 18 |
| INT01 | PC1 | 55 | 57 | 45 | 37 | 32 | 29 | 26 | 19 |
| INT02 | PC2 | 56 | 58 | 46 | 38 | 33 | 30 | 27 | 20 |
| INT03 | PB1 | 27 | 29 | 22 | 18 | 15 | 14 | 13 | 9 |
| INT04 | PJ4 | 75 | 77 | 60 | 48 | 39 | 36 | 32 | 25 |
| INT05 | PK1 | 78 | 80 | 63 | 51 | 42 | 39 | 35 | 28 |
| INT06 | PH3 | 52 | 54 | 42 | 34 | 29 | 26 | - | - |
| INT07 | PA6 | 12 | 14 | 11 | 7 | 7 | - | - | - |
| INT08 | PL3 | 37 | 39 | 29 | 25 | - | - | - | - |
| INT09 | PM2 | 23 | 25 | 18 | 14 | - | - | - | - |
| INT10 | PN3 | 67 | 69 | 52 | 40 | - | - | - | - |
| INT11 | PA7 | 11 | 13 | 10 | - | - | - | - | - |
| INT12 | PL4 | 38 | 40 | 30 | - | - | - | - | - |
| INT13 | PK7 | 84 | 86 | 69 | - | - | - | - | - |
| INT14 | PP3 | 85 | 87 | 70 | - | - | - | - | - |
| INT15 | PM6 | 19 | 21 | - | - | - | - | - | - |

Table 4.7 T32A00, T32A01

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| T32A00INA0 | PA1 | 17 | 19 | 16 | 12 | 12 | 11 | 10 | 6 |
| | PM1 | 24 | 26 | 19 | 15 | - | - | - | - |
| T32A00INA1 | PA2 | 16 | 18 | 15 | 11 | 11 | 10 | 9 | 5 |
| | PM2 | 23 | 25 | 18 | 14 | - | - | - | - |
| T32A00OUTA | PA0 | 18 | 20 | 17 | 13 | 13 | 12 | 11 | 7 |
| | PM0 | 25 | 27 | 20 | 16 | - | - | - | - |
| T32A00INB0 | PA4 | 14 | 16 | 13 | 9 | 9 | 8 | 7 | - |
| | PM4 | 21 | 23 | - | - | - | - | - | - |
| T32A00INB1 | PA5 | 13 | 15 | 12 | 8 | 8 | 7 | 6 | - |
| | PM5 | 20 | 22 | - | - | - | - | - | - |
| T32A00OUTB | PA3 | 15 | 17 | 14 | 10 | 10 | 9 | 8 | - |
| | PM3 | 22 | 24 | - | - | - | - | - | - |
| T32A00INC0 | PA1 | 17 | 19 | 16 | 12 | 12 | 11 | 10 | 6 |
| | PM1 | 24 | 26 | 19 | 15 | - | - | - | - |
| T32A00INC1 | PA2 | 16 | 18 | 15 | 11 | 11 | 10 | 9 | 5 |
| | PM2 | 23 | 25 | 18 | 14 | - | - | - | - |
| T32A00OUTC | PA0 | 18 | 20 | 17 | 13 | 13 | 12 | 11 | 7 |
| | PM0 | 25 | 27 | 20 | 16 | - | - | - | - |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| T32A01INA0 | PB1 | 27 | 29 | 22 | 18 | 15 | 14 | 13 | 9 |
| | PP1 | 42 | 44 | 32 | - | - | - | - | - |
| T32A01INA1 | PB2 | 28 | 30 | 23 | 19 | 16 | 15 | 14 | - |
| | PP2 | 43 | 45 | 33 | - | - | - | - | - |
| T32A01OUTA | PB0 | 26 | 28 | 21 | 17 | 14 | 13 | 12 | 8 |
| | PP0 | 41 | 43 | 31 | - | - | - | - | - |
| T32A01INB0 | PB4 | 30 | 32 | 25 | 21 | 18 | 17 | 16 | - |
| T32A01INB1 | PB5 | 31 | 33 | - | - | - | - | - | - |
| T32A01OUTB | PB3 | 29 | 31 | 24 | 20 | 17 | 16 | 15 | - |
| T32A01INC0 | PB1 | 27 | 29 | 22 | 18 | 15 | 14 | 13 | 9 |
| | PP1 | 42 | 44 | 32 | - | - | - | - | - |
| T32A01INC1 | PB2 | 28 | 30 | 23 | 19 | 16 | 15 | 14 | - |
| | PP2 | 43 | 45 | 33 | - | - | - | - | - |
| T32A01OUTC | PB0 | 26 | 28 | 21 | 17 | 14 | 13 | 12 | 8 |
| | PP0 | 41 | 43 | 31 | - | - | - | - | - |

Table 4.8 T32A02, T32A03

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| T32A02INA0 | PC1 | 55 | 57 | 45 | 37 | 32 | 29 | 26 | 19 |
| | PR1 | 62 | 64 | - | - | - | - | - | - |
| T32A02INA1 | PC2 | 56 | 58 | 46 | 38 | 33 | 30 | 27 | 20 |
| | PR2 | 63 | 65 | - | - | - | - | - | - |
| T32A02OUTA | PC0 | 54 | 56 | 44 | 36 | 31 | 28 | 25 | 18 |
| | PR0 | 61 | 63 | - | - | - | - | - | - |
| T32A02INB0 | PC4 | 58 | 60 | 48 | - | - | - | - | - |
| T32A02INB1 | PC5 | 59 | 61 | 49 | - | - | - | - | - |
| T32A02OUTB | PC3 | 57 | 59 | 47 | 39 | 34 | 31 | - | - |
| T32A02INC0 | PC1 | 55 | 57 | 45 | 37 | 32 | 29 | 26 | 19 |
| | PR1 | 62 | 64 | - | - | - | - | - | - |
| T32A02INC1 | PC2 | 56 | 58 | 46 | 38 | 33 | 30 | 27 | 20 |
| | PR2 | 63 | 65 | - | - | - | - | - | - |
| T32A02OUTC | PC0 | 54 | 56 | 44 | 36 | 31 | 28 | 25 | 18 |
| | PR0 | 61 | 63 | - | - | - | - | - | - |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| T32A03INA0 | PJ1 | 72 | 74 | 57 | 45 | 36 | 33 | 29 | 22 |
| T32A03INA1 | PJ2 | 73 | 75 | 58 | 46 | 37 | 34 | 30 | 23 |
| T32A03OUTA | PJ0 | 71 | 73 | 56 | 44 | 35 | 32 | 28 | 21 |
| T32A03INB0 | PJ4 | 75 | 77 | 60 | 48 | 39 | 36 | 32 | 25 |
| T32A03INB1 | PJ5 | 76 | 78 | 61 | 49 | 40 | 37 | 33 | 26 |
| T32A03OUTB | PJ3 | 74 | 76 | 59 | 47 | 38 | 35 | 31 | 24 |
| T32A03INC0 | PJ1 | 72 | 74 | 57 | 45 | 36 | 33 | 29 | 22 |
| T32A03INC1 | PJ2 | 73 | 75 | 58 | 46 | 37 | 34 | 30 | 23 |
| T32A03OUTC | PJ0 | 71 | 73 | 56 | 44 | 35 | 32 | 28 | 21 |

Table 4.9 T32A04, T32A05

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| T32A04INA0 | PK3 | 80 | 82 | 65 | 53 | 44 | 41 | 37 | 30 |
| T32A04INA1 | PK4 | 81 | 83 | 66 | 54 | 45 | 42 | 38 | - |
| T32A04OUTA | PK2 | 79 | 81 | 64 | 52 | 43 | 40 | 36 | 29 |
| T32A04INB0 | PK6 | 83 | 85 | 68 | 56 | - | - | - | - |
| T32A04INB1 | PK7 | 84 | 86 | 69 | - | - | - | - | - |
| T32A04OUTB | PK5 | 82 | 84 | 67 | 55 | 46 | 43 | 39 | - |
| T32A04INC0 | PK3 | 80 | 82 | 65 | 53 | 44 | 41 | 37 | 30 |
| T32A04INC1 | PK4 | 81 | 83 | 66 | 54 | 45 | 42 | 38 | - |
| T32A04OUTC | PK2 | 79 | 81 | 64 | 52 | 43 | 40 | 36 | 29 |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| T32A05INA0 | PN1 | 69 | 71 | 54 | 42 | - | - | - | - |
| T32A05INA1 | PN2 | 68 | 70 | 53 | 41 | - | - | - | - |
| T32A05OUTA | PN0 | 70 | 72 | 55 | 43 | - | - | - | - |
| T32A05INB0 | PN4 | 66 | 68 | 51 | - | - | - | - | - |
| T32A05INB1 | PN5 | 65 | 67 | - | - | - | - | - | - |
| T32A05OUTB | PN3 | 67 | 69 | 52 | 40 | - | - | - | - |
| T32A05INC0 | PN1 | 69 | 71 | 54 | 42 | - | - | - | - |
| T32A05INC1 | PN2 | 68 | 70 | 53 | 41 | - | - | - | - |
| T32A05OUTC | PN0 | 70 | 72 | 55 | 43 | - | - | - | - |

Table 4.10 TSPI0, TSPI1

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| TSPI0CSIN | PM3 | 22 | 24 | - | - | - | - | - | - |
| | PA3 | 15 | 17 | 14 | 10 | 10 | 9 | 8 | - |
| TSPI0CS0 | PM3 | 22 | 24 | - | - | - | - | - | - |
| | PA3 | 15 | 17 | 14 | 10 | 10 | 9 | 8 | - |
| TSPI0CS1 | PM4 | 21 | 23 | - | - | - | - | - | - |
| | PA4 | 14 | 16 | 13 | 9 | 9 | 8 | 7 | - |
| TSPI0RXD | PM2 | 23 | 25 | 18 | 14 | - | - | - | - |
| | PA2 | 16 | 18 | 15 | 11 | 11 | 10 | 9 | 5 |
| TSPI0TXD | PM1 | 24 | 26 | 19 | 15 | - | - | - | - |
| | PA1 | 17 | 19 | 16 | 12 | 12 | 11 | 10 | 6 |
| TSPI0SCK | PM0 | 25 | 27 | 20 | 16 | - | - | - | - |
| | PA0 | 18 | 20 | 17 | 13 | 13 | 12 | 11 | 7 |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| TSPI1CSIN | PL6 | 40 | 42 | - | - | - | - | - | - |
| | PB5 | 31 | 33 | - | - | - | - | - | - |
| TSPI1CS0 | PL6 | 40 | 42 | - | - | - | - | - | - |
| | PB5 | 31 | 33 | - | - | - | - | - | - |
| TSPI1CS1 | PL5 | 39 | 41 | - | - | - | - | - | - |
| | PB6 | 32 | 34 | - | - | - | - | - | - |
| TSPI1RXD | PP2 | 43 | 45 | 33 | - | - | - | - | - |
| | PB4 | 30 | 32 | 25 | 21 | 18 | 17 | 16 | - |
| TSPI1TXD | PP1 | 42 | 44 | 32 | - | - | - | - | - |
| | PB3 | 29 | 31 | 24 | 20 | 17 | 16 | 15 | - |
| TSPI1SCK | PP0 | 41 | 43 | 31 | - | - | - | - | - |
| | PB2 | 28 | 30 | 23 | 19 | 16 | 15 | 14 | - |

Table 4.11 UART0, UART1

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| UT0RXD | PA2 | 16 | 18 | 15 | 11 | 11 | 10 | 9 | 5 |
| | PA1 | 17 | 19 | 16 | 12 | 12 | 11 | 10 | 6 |
| | PM2 | 23 | 25 | 18 | 14 | - | - | - | - |
| | PM1 | 24 | 26 | 19 | 15 | - | - | - | - |
| UT0TXDA | PA1 | 17 | 19 | 16 | 12 | 12 | 11 | 10 | 6 |
| | PA2 | 16 | 18 | 15 | 11 | 11 | 10 | 9 | 5 |
| | PM1 | 24 | 26 | 19 | 15 | - | - | - | - |
| | PM2 | 23 | 25 | 18 | 14 | - | - | - | - |
| UT0TXDB | PA0 | 18 | 20 | 17 | 13 | 13 | 12 | 11 | 7 |
| | PM0 | 25 | 27 | 20 | 16 | - | - | - | - |
| UT0CTS_N | PM3 | 22 | 24 | - | - | - | - | - | - |
| | PM4 | 21 | 23 | - | - | - | - | - | - |
| UT0RTS_N | PM4 | 21 | 23 | - | - | - | - | - | - |
| | PM3 | 22 | 24 | - | - | - | - | - | - |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| UT1RXD | PJ2 | 73 | 75 | 58 | 46 | 37 | 34 | 30 | 23 |
| | PJ1 | 72 | 74 | 57 | 45 | 36 | 33 | 29 | 22 |
| | PK2 | 79 | 81 | 64 | 52 | 43 | 40 | 36 | 29 |
| | PK1 | 78 | 80 | 63 | 51 | 42 | 39 | 35 | 28 |
| UT1TXDA | PJ1 | 72 | 74 | 57 | 45 | 36 | 33 | 29 | 22 |
| | PJ2 | 73 | 75 | 58 | 46 | 37 | 34 | 30 | 23 |
| | PK1 | 78 | 80 | 63 | 51 | 42 | 39 | 35 | 28 |
| | PK2 | 79 | 81 | 64 | 52 | 43 | 40 | 36 | 29 |
| UT1TXDB | PJ0 | 71 | 73 | 56 | 44 | 35 | 32 | 28 | 21 |
| | PK0 | 77 | 79 | 62 | 50 | 41 | 38 | 34 | 27 |
| UT1CTS_N | PJ3 | 74 | 76 | 59 | 47 | 38 | 35 | 31 | 24 |
| | PJ4 | 75 | 77 | 60 | 48 | 39 | 36 | 32 | 25 |
| | PK3 | 80 | 82 | 65 | 53 | 44 | 41 | 37 | - |
| | PK4 | 81 | 83 | 66 | 54 | 45 | 42 | 38 | - |
| UT1RTS_N | PJ4 | 75 | 77 | 60 | 48 | 39 | 36 | 32 | 25 |
| | PJ3 | 74 | 76 | 59 | 47 | 38 | 35 | 31 | 24 |
| | PK4 | 81 | 83 | 66 | 54 | 45 | 42 | 38 | - |
| | PK3 | 80 | 82 | 65 | 53 | 44 | 41 | 37 | - |

Table 4.12 UART2

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| UT2RXD | PB3 | 29 | 31 | 24 | 20 | 17 | 16 | 15 | - |
| | PB2 | 28 | 30 | 23 | 19 | 16 | 15 | 14 | - |
| | PL1 | 35 | 37 | 27 | 23 | 20 | - | - | - |
| | PL0 | 34 | 36 | 26 | 22 | 19 | - | - | - |
| UT2TXDA | PB2 | 28 | 30 | 23 | 19 | 16 | 15 | 14 | - |
| | PB3 | 29 | 31 | 24 | 20 | 17 | 16 | 15 | - |
| | PL0 | 34 | 36 | 26 | 22 | 19 | - | - | - |
| | PL1 | 35 | 37 | 27 | 23 | 20 | - | - | - |
| UT2CTS_N | PB4 | 30 | 32 | - | - | - | - | - | - |
| | PB5 | 31 | 33 | - | - | - | - | - | - |
| | PL2 | 36 | 38 | 28 | 24 | - | - | - | - |
| | PL3 | 37 | 39 | 29 | 25 | - | - | - | - |
| UT2RTS_N | PB5 | 31 | 33 | - | - | - | - | - | - |
| | PB4 | 30 | 32 | - | - | - | - | - | - |
| | PL3 | 37 | 39 | 29 | 25 | - | - | - | - |
| | PL2 | 36 | 38 | 28 | 24 | - | - | - | - |

Table 4.13 I²C0, I²C1, I²C2

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| I2C0SDA | PC1 | 55 | 57 | 45 | 37 | 32 | 29 | 26 | 19 |
| I2C0SCL | PC0 | 54 | 56 | 44 | 36 | 31 | 28 | 25 | 18 |
| I2C1SDA | PA5 | 13 | 15 | 12 | 8 | 8 | 7 | 6 | - |
| I2C1SCL | PA4 | 14 | 16 | 13 | 9 | 9 | 8 | 7 | - |
| I2C2SDA | PL1 | 35 | 37 | 27 | 23 | 20 | - | - | - |
| I2C2SCL | PL0 | 34 | 36 | 26 | 22 | 19 | - | - | - |

Table 4.14 PMD+, A-ENC

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| EMG0_N | PK0 | 77 | 79 | 62 | 50 | 41 | 38 | 34 | 27 |
| OVV0_N | PK1 | 78 | 80 | 63 | 51 | 42 | 39 | 35 | 28 |
| UO0 | PJ0 | 71 | 73 | 56 | 44 | 35 | 32 | 28 | 21 |
| VO0 | PJ2 | 73 | 75 | 58 | 46 | 37 | 34 | 30 | 23 |
| WO0 | PJ4 | 75 | 77 | 60 | 48 | 39 | 36 | 32 | 25 |
| XO0 | PJ1 | 72 | 74 | 57 | 45 | 36 | 33 | 29 | 22 |
| YO0 | PJ3 | 74 | 76 | 59 | 47 | 38 | 35 | 31 | 24 |
| ZO0 | PJ5 | 76 | 78 | 61 | 49 | 40 | 37 | 33 | 26 |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| ENC0A | PA0 | 18 | 20 | 17 | 13 | 13 | 12 | 11 | 7 |
| ENC0B | PA1 | 17 | 19 | 16 | 12 | 12 | 11 | 10 | 6 |
| ENC0Z | PA2 | 16 | 18 | 15 | 11 | 11 | 10 | 9 | 5 |

Table 4.15 AINAx, DACx

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| AINA00 | PD0 | 4 | 6 | 3 | 3 | 3 | 3 | 3 | 2 |
| AINA01 | PD1 | 3 | 5 | 2 | 2 | 2 | 2 | 2 | 1 |
| AINA02 | PD2 | 2 | 4 | 1 | 1 | 1 | 1 | 1 | - |
| AINA03 | PD3 | 1 | 3 | - | - | - | - | - | - |
| AINA04 | PE0 | 100 | 2 | 80 | 64 | 52 | 48 | 44 | 32 |
| AINA05 | PE1 | 99 | 1 | 79 | 63 | 51 | 47 | 43 | 31 |
| AINA06 | PE2 | 98 | 100 | 78 | 62 | 50 | 46 | 42 | - |
| AINA07 | PE3 | 97 | 99 | 77 | 61 | 49 | 45 | 41 | - |
| AINA08 | PE4 | 96 | 98 | 76 | 60 | 48 | 44 | 40 | - |
| AINA09 | PE5 | 95 | 97 | 75 | - | - | - | - | - |
| AINA10 | PE6 | 94 | 96 | 74 | - | - | - | - | - |
| AINA11 | PF0 | 93 | 95 | - | - | - | - | - | - |
| AINA12 | PF1 | 92 | 94 | - | - | - | - | - | - |
| AINA13 | PF2 | 91 | 93 | - | - | - | - | - | - |
| AINA14 | PF3 | 90 | 92 | - | - | - | - | - | - |
| AINA15 | PF4 | 89 | 91 | - | - | - | - | - | - |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| DAC0 | PG0 | 7 | 9 | 6 | 6 | 6 | 6 | - | - |
| DAC1 | PG1 | 8 | 10 | 7 | - | - | - | - | - |

Table 4.16 TRGINx, RXINx, RTCOUT

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| TRGIN0 | PB1 | 27 | 29 | 22 | 18 | 15 | 14 | 13 | 9 |
| TRGIN1 | PA3 | 15 | 17 | 14 | 10 | 10 | 9 | 8 | - |
| TRGIN2 | PN3 | 67 | 69 | 52 | 40 | - | - | - | - |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| RXIN0 | PB1 | 27 | 29 | 22 | 18 | 15 | 14 | 13 | 9 |
| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| RTCOUT | PC2 | 56 | 58 | 46 | 38 | 33 | 30 | - | - |

Table 4.17 Debug pins

| Combination functional pin name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|---------------------------------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| TMS | PK2 | 79 | 81 | 64 | 52 | 43 | 40 | 36 | 29 |
| TCK | PK3 | 80 | 82 | 65 | 53 | 44 | 41 | 37 | 30 |
| TDO | PK4 | 81 | 83 | 66 | 54 | 45 | 42 | 38 | - |
| TDI | PK5 | 82 | 84 | 67 | 55 | 46 | 43 | 39 | - |
| TRST_N | PK6 | 83 | 85 | 68 | 56 | - | - | - | - |
| SWDIO | PK2 | 79 | 81 | 64 | 52 | 43 | 40 | 36 | 29 |
| SWCLK | PK3 | 80 | 82 | 65 | 53 | 44 | 41 | 37 | 30 |
| SWV | PK4 | 81 | 83 | 66 | 54 | 45 | 42 | 38 | - |
| TRACECLK | PM0 | 25 | 27 | 20 | 16 | - | - | - | - |
| TRACEDATA0 | PM1 | 24 | 26 | 19 | 15 | - | - | - | - |
| TRACEDATA1 | PM2 | 23 | 25 | 18 | 14 | - | - | - | - |
| TRACEDATA2 | PM3 | 22 | 24 | - | - | - | - | - | - |
| TRACEDATA3 | PM4 | 21 | 23 | - | - | - | - | - | - |

Table 4.18 Control Pins

| Pin Name | Port Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|----------|-----------|----------------|---------------|---------------|---------------|---------------|------------------------|---------------|---------------|
| X1 | PH0 | 48 | 50 | 38 | 30 | 25 | 22 | 21 | 14 |
| X2 | PH1 | 49 | 51 | 39 | 31 | 26 | 23 | 22 | 15 |
| XT1 | PH2 | 51 | 53 | 41 | 33 | 28 | 25 | - | - |
| XT2 | PH3 | 52 | 54 | 42 | 34 | 29 | 26 | - | - |
| EHCLKIN | PH0 | 48 | 50 | 38 | 30 | 25 | 22 | 21 | 14 |
| BOOT_N | PB0 | 26 | 28 | 21 | 17 | 14 | 13 | 12 | 8 |
| RESET_N | | 50 | 52 | 40 | 32 | 27 | 24 | 23 | 16 |
| MODE | | 53 | 55 | 43 | 35 | 30 | 27 | 24 | 17 |
| BSC | | 86 | 88 | 71 | 57 | 47 | - | - | - |

Table 4.19 Power Supply pins

| Pin Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
|----------|-------------------|------------------|------------------|------------------|------------------|------------------------------|------------------|------------------|
| DVDD5A | 44 | 46 | 34 | 26 | 21 | 18 | 17 | 10 |
| DVDD5B | 87 | 89 | 72 | 58 | - | - | - | - |
| DVDD5C | 10 | 12 | 9 | - | - | - | - | - |
| DVSSA | 47 | 49 | 37 | 29 | 24 | 21 | 20 | 13 |
| DVSSB | 88 | 90 | 73 | 59 | - | - | - | - |
| DVSSC | 9 | 11 | 8 | - | - | - | - | - |
| REGOUT1 | 46 | 48 | 36 | 28 | 23 | 20 | 19 | 12 |
| REGOUT2 | 45 | 47 | 35 | 27 | 22 | 19 | 18 | 11 |
| AVDD5 | 5 | 7 | 4 | 4 | 4 | 4 | 4 | 3 |
| AVSS | 6 | 8 | 5 | 5 | 5 | 5 | 5 | 4 |
| Pin Name | M3H6 (LQFP100) | M3H6 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP64) | M3H3 (LQFP52) | M3H2 (LQFP48) (VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) |
| PB7 | 33 | 35 | - | - | - | - | - | - |
| PC6 | 60 | 62 | 50 | - | - | - | - | - |
| PR3 | 64 | 66 | - | - | - | - | - | - |

4.3. Ports

The symbols of each table of the port have the following meanings.

The right-hand side of the port shows specification with the symbol.

The symbols have the following meanings.

- Input/Output: Input or/and Output of Port
Input: Input port
Output: Output port
I/O: Input/Output port
- PU/PD: Programmable pull-up/pull-down
PU: Programmable pull-up is selectable
PD: Programmable pull-down is selectable
- OD: Programmable open-drain output
Yes: Support
No: Non support
- 5V_T: 5V-tolerant
Yes: Support
N/A: Not available
- SMT/CMOS: Input gate
SMT: Schmitt trigger input
CMOS: CMOS input
- Under Reset: Port state under Reset
Hi-z: High impedance
PU: Pull-up
PD: Pull-down
- After Reset: Port state after Reset
Hi-z: High impedance
PU: Pull-up
PD: Pull-down

4.3.1. Port Specification Table

Table 4.20 Port names, and specifications of Port A, B, C, D, E, F

| Port Name | Input/Output | PU/PD | OD | 5V_T | SMT/CMOS | Under Reset | After Reset |
|-----------|--------------|--------------|-----|------|----------|-------------|-------------|
| PA0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PA1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PA2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PA3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PA4 | I/O | PU/PD | YES | YES | SMT | Hi-z | Hi-z |
| PA5 | I/O | PU/PD | YES | YES | SMT | Hi-z | Hi-z |
| PA6 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PA7 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PB0 | Output | PU/PD (Note) | YES | N/A | SMT | Hi-z (Note) | Hi-z |
| PB1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PB2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PB3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PB4 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PB5 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PB6 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PB7 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PC0 | I/O | PU/PD | YES | YES | SMT | Hi-z | Hi-z |
| PC1 | I/O | PU/PD | YES | YES | SMT | Hi-z | Hi-z |
| PC2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PC3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PC4 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PC5 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PC6 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PD0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PD1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PD2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PD3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PE0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PE1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PE2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PE3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PE4 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PE5 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PE6 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PF0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PF1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PF2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PF3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PF4 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |

Note: combination with BOOT_N. When RESET_N=0, Pull-up resistor is enabled.
When RESET_N=1, the pin state is Hi-z with internal reset.

Table 4.21 Port names, and specifications of Port G, J, K, L, M

| Port Name | Input/Output | PU/PD | OD | 5V_T | SMT/CMOS | Under Reset | After Reset |
|-----------|--------------|-------|-----|------|----------|----------------|----------------|
| PG0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PG1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PH0 | Input | PD | N/A | N/A | SMT | Hi-z | Hi-z |
| PH1 | Input | PD | N/A | N/A | SMT | Hi-z | Hi-z |
| PH2 | Input | PD | N/A | N/A | SMT | Hi-z | Hi-z |
| PH3 | Input | PD | N/A | N/A | SMT | Hi-z | Hi-z |
| PJ0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PJ1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PJ2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PJ3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PJ4 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PJ5 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PK0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PK1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PK2 | I/O | PU/PD | YES | N/A | SMT | PU(Note) | PU(Note) |
| PK3 | I/O | PU/PD | YES | N/A | SMT | PD(Note) | PD(Note) |
| PK4 | I/O | PU/PD | YES | N/A | SMT | Hi-z (Note) | Hi-z (Note) |
| PK5 | I/O | PU/PD | YES | N/A | SMT | PU(Note) | PU(Note) |
| PK6 | I/O | PU/PD | YES | N/A | SMT | PU(Note) | PU(Note) |
| PK7 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PL0 | I/O | PU/PD | YES | YES | SMT | Hi-z | Hi-z |
| PL1 | I/O | PU/PD | YES | YES | SMT | Hi-z | Hi-z |
| PL2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PL3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PL4 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PL5 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PL6 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PM0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PM1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PM2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PM3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PM4 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PM5 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PM6 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |

Note: It is assigned to a debugging pin in the state of the initial stage. (PK2:TMS/SWDIO, PK3:TCK/SWCLK, PK4:TDO/SWV, PK5:TDI, PK6: TRST_N)

Table 4.22 Port names, and specifications of Port N, P, R

| Port Name | Input/Output | PU/PD | OD | 5V_T | SMT/CMOS | Under Reset | After Reset |
|-----------|--------------|-------|-----|------|----------|-------------|-------------|
| PN0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PN1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PN2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PN3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PN4 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PN5 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PP0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PP1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PP2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PP3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PR0 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PR1 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PR2 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |
| PR3 | I/O | PU/PD | YES | N/A | SMT | Hi-z | Hi-z |

5. Functional Description and Operation Description

5.1. Reference Manuals

For more information on the product of TMPM3H Group(1), please refer to Reference Manuals below;

Table 5.1 Reference Manuals for TMPM3H Group(1)

| Reference Manual | IP Symbol | Category |
|--|---------------|------------|
| Port (TMPM3H group(1)) | PORT-M3H(1) | System |
| Memory Map (TMPM3H group(1)) | MMAP-M3H(1) | System |
| Exception (TMPM3H group(1)) | EXCEPT-M3H(1) | System |
| Clock Control and operation mode (TMPM3H group(1)) | CG-M3H(1)-D | System |
| Product Information (TMPM3H group(1)) | PINFO-M3H(1) | System |
| Power supply and Reset operation (TMPM3H group(1)) | RESET-M3H(1) | System |
| Flash Memory (128KB Code FLASH and 32KB Data FLASH) | FLASH128_32-A | Peripheral |
| Trimming Circuit | TRM-A | Peripheral |
| Oscillation Frequency Detector | OFD-A | Peripheral |
| Voltage Detection Circuit | LVD-A | Peripheral |
| Digital Noise Filter Circuit | DNF-A | Peripheral |
| Debug Interface | DEBUG-A | Peripheral |
| DMA Controller | DMAC-B | Peripheral |
| Asynchronous Serial Communication Circuit | UART-C | Peripheral |
| Serial Peripheral Interface | TSPI-B | Peripheral |
| I ² C interface | I2C-B | Peripheral |
| 8-bit Digital to Analog Converter | DAC-A | Peripheral |
| 12-bit Analog to Digital Converter | ADC-A | Peripheral |
| Programmable Motor Control Circuit plus | PMD+-A | Peripheral |
| Advanced Encoder Input Circuit | A-ENC-A | Peripheral |
| 32-bit Timer Event Counter | T32A-B | Peripheral |
| Real Time Clock | RTC-A | Peripheral |
| Clock Selective Watchdog Timer | SIWDT-A | Peripheral |
| Remote Control Signal Preprocessor | RMC-A | Peripheral |
| Boundary Scan | BSC-A | Peripheral |

5.2. Processor Core

The TMPM3H Group(1) incorporates a high-performance 32-bit processor core (Arm Cortex-M3 core).

For the operation of the processor core, refer to the Arm documentation set of the Arm "Cortex-M" series processor. This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M3 core revision used in the TMPM3H Group(1) is shown as below:

For details of the CPU core and the architecture, refer to the documentation of the Arm in the following URL:

<http://infocenter.arm.com/help/index.jsp>

Table 5.2 Core revision

| Group name | Core revision |
|-----------------|---------------|
| TMPM3H Group(1) | r2p1 |

5.2.2. Configurable Options

In the Cortex-M3 core, some blocks can be selected to implement. The following table shows the configurations of the TMPM3H Group(1).

Table 5.3 Configurable options and their implementations

| Configurable option | Implementation |
|--------------------------------|--|
| FWB | Literal comparator: 2 Instruction comparator: 6 |
| DWT | Comparator: 4 |
| ITM | Available |
| MPU | Available |
| ETM | Available |
| AHB-AP | Available |
| AHB trace macro cell interface | Not available |
| TPIU | Available |
| WIC | Not available |
| Debug port | JTAG/serial wire |
| Bit band | Available |
| Sequential control of AHB | Not available |

5.3. Clock Control and Operation mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low-power consumption mode as operation modes. Power consumption can be decreased by mode transition.

The outline of the clock control circuit is as follows:

- Internal high-speed oscillation circuit: 10MHz
- Selectable from the external high-speed oscillation circuit or internal high-speed oscillation circuit.
- PLL (Clock Multiplication Circuit): Capable of 40 MHz output by changing the multiplication ratio according to the frequency of the high-speed oscillation circuit
- Clock gear: The high-speed clock can be divided by 1/1, 1/2, 1/4, 1/8, or 1/16 and the clock is used as the system clock (fsys).
- Low-power consumption mode:
 - IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can enable or disable operation in the IDLE mode.
 - STOP1: Except some peripheral circuits, all the internal circuits including the internal oscillator are brought to a stop in STOP1 mode. External low frequency oscillator can oscillate. RTC and RMC can be used.
 - STOP2: This mode halts voltage supply, retaining some peripheral circuits operation. External low frequency oscillator can oscillate (RTC can be used.), and wake-up by I²C slave address matching.

5.4. Flash Memory (Code FLASH, Data FLASH)

The code flash stores instruction code, and CPU reads instruction code and executes. The data flash stores data, and even if a power supply is off, data can be kept.

It has the dual mode that possible to write and erase a data flash while executing an order by a code flash, and it's also possible to continue executing an application program during writing or erasing data flash.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by the 3rd person.

5.5. Oscillation Circuit

External High Speed Oscillator (EHOSC): Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.

External Low Speed Oscillator (ELOSC): Connect crystal resonator (32.768 kHz) to terminals. Use clock source for Real Time Clock or Power consumption mode.

Internal High Speed Oscillator 1(IHOSC1): Oscillation frequency is 10MHz. Use clock source for System clock.

Internal High Speed Oscillator 2(IHOSC2): Oscillation frequency is 10MHz. Use clock source for OFD and SIWDT.

Table 5.4 Built-in Oscillator

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|--------|------|------|------|------|------|------|------|
| EHOSC | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ELOSC | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |
| IHOSC1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| IHOSC2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The trimming function can adjust frequency of the internal high-speed oscillator 1 (IHOSC1).

In the coarse trimming, -20.4% to +33.0% adjustment by 0.8%-step is feasible. In the delicate trimming, -0.8% to +0.7% adjustment by 0.1%-step is feasible.

Table 5.5 Built-in TRM

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----|------|------|------|------|------|------|------|
| TRM | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.7. Oscillation Frequency Detection Circuit (OFD)

The oscillation frequency detection circuit (OFD) is a function that detects an abnormal state of the clock. It measures the external high-speed oscillation (f_{EHOSC}) or high-speed clock (f_c) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.

The upper limit and the lower limit of detection frequency ranges can be specified respectively.

Table 5.6 Built-in OFD

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----|------|------|------|------|------|------|------|
| OFD | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be chosen from eight kinds. LVD is set to enable from the Reset state at the Power-on.

Table 5.7 Built-in LVD

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----|------|------|------|------|------|------|------|
| LVD | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.9. Digital Noise Filter (DNF)

The digital noise canceler circuit can eliminate noise of input signals from external interrupt pins at the certain range. The noise of the High level / Low level input of the external interrupt signal INTx is removed.

Table 5.8 Number of External Interrupt (Built-in DNF)

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|------------------------------|------|------|------|------|------|------|------|
| Number of External Interrupt | 16 | 15 | 11 | 8 | 7 | 6 | 6 |

5.10. Debug Interface (DEBUG)

TMPM3H group(1) contain Interface for connect debug tool, which is the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N). These are connected with the Debug tool and used for program development. And also it contains the trace clock (TRACECLK) and data output (TRACEDATA0to3) to reduce the Debug Process.

Table 5.9 Built-in Debug Interface

| Pin Name | Port | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|------------|------|------|------|------|------|------|------|------|
| TMS/SWDIO | PK2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| TCK/SWCLK | PK3 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| TDO/SWV | PK4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| TDI | PK5 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| TRST_N | PK6 | ✓ | ✓ | ✓ | - | - | - | - |
| TRACECLK | PM0 | ✓ | ✓ | ✓ | - | - | - | - |
| TRACEDATA0 | PM1 | ✓ | ✓ | ✓ | - | - | - | - |
| TRACEDATA1 | PM2 | ✓ | ✓ | ✓ | - | - | - | - |
| TRACEDATA2 | PM3 | ✓ | - | - | - | - | - | - |
| TRACEDATA3 | PM4 | ✓ | - | - | - | - | - | - |

Note: ✓: Available, -: N/A

5.11. DMA Controller (DMAC)

The DMAC is the peripheral function to move the data between peripheral functions and the memory, or between memories. These operations are performed separately from the CPU control; thus, the Load of CPU can greatly be reduced by using the DMA.

TMPM3H Group (1) product has one DMA controller (DMAC) unit, and there are up to 32 channels of activation factors per unit.

Table 5.10 Built-in DMAC

| UNIT | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|--------|------|------|------|------|------|------|------|
| UNIT A | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.12. Asynchronous Serial Communication Circuit (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first / LSB first and reversal of data polarity can be performed and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8-stage at transmission; and on 8-stage at reception.

The telecommunication control by CTS/RTS and half clock mode are supported.

Table 5.11 Built-in UART

| Channel | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----------|------|------|------|------|------|------|------|
| Channel 0 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |

Note1: ✓: Available, -: N/A

Note2: External pins are not same by product. Please refer to section "2 Pin Assignment".

5.13. Serial Peripheral Interface (TSPI)

The TSPI supports two communication methods and enables to perform serial communication between other devices at high speed. The SPI bus type, which uses a CS (Chip Select) signal at communications, and SIO bus type, which does not use a CS signal at communications can be selected.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There are an 8-stage 16-bit FIFO for reception and transmission, each. The TSPI supports master and slave communications.

Table 5.12 Built-in TSPI

| Channel | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----------|------|------|------|------|------|------|------|
| Channel 0 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |

Note1: ✓: Available, -: N/A

Note2: External pins are not same by product. Please refer to section "2 Pin Assignment".

5.14. I²C Interface (I²C)

I²C is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports STD mode (Max 100kbps), Fast mode (Max 400kbps), and Fast mode plus; Fm+ (Max 1Mbps).

Channel 0 provides the address match wake up function. Depending on the setting, the MCU can receive data even in low-power consumption mode including IDLE, STOP1, or STOP2 mode and can return to normal mode by the Slave address match wake up function. (Note2)

Table 5.13 Built-in I²C

| Channel | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-------------------|------|------|------|------|------|------|------|
| Channel 0 (Note2) | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | - |
| Channel 2 | ✓ | ✓ | ✓ | ✓ | - | - | - |

Note1: ✓: Available, -: N/A

Note2: The address match wake up function is available.

5.15. 8-bit Digital-to-Analog Converter (DAC)

The DAC is an R-2R type 8-bit digital-to-analog converter that can output the specified voltage. A buffer amplifier is not incorporated.

Table 5.14 Built-in DAC

| Channel | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----------|------|------|------|------|------|------|------|
| Channel 0 | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |
| Channel 1 | ✓ | ✓ | - | - | - | - | - |

Note: ✓: Available, -: N/A

5.16. 12-bit Analog-to-Digital Converter (ADC)

The ADC is a successive-approximation analog-to-digital converter. It supports maximum 16 analog inputs. The combination of a conversion result register and analog input can be programmed in each startup trigger of AD conversion. A startup trigger for analog-to-digital conversion can be selected from software or peripheral functions (PMD trigger outputs, timer/event counter outputs, port inputs).

The monitor function is also available and it can generate an interrupt request when the compare conditions are matched.

Table 5.15 Built-in ADC

| UNIT | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|--------|------|------|------|------|------|------|------|
| UNIT A | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

Table 5.16 Number of analog inputs for ADC

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-------------------------|------|------|------|------|------|------|------|
| Analog Inputs Pin count | 16 | 10 | 8 | 8 | 8 | 8 | 4 |

5.17. Motor Control Circuit Plus (PMD+)

The motor control circuit plus (PMD+) enables users to control brushless DC motors easily. It incorporates the three-phase pulse modulation circuit and dead-time circuit, and easily generates waveforms for motor control by operating with the ADC in a coordinated fashion.

It also provides the over-voltage detection input and abnormal detection input to support safety measures.

Table 5.17 Built-in PMD+

| Channel | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----------|------|------|------|------|------|------|------|
| Channel 0 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.18. Advanced Encoder Input Circuit (A-ENC)

The advanced encoder input circuit (A-ENC) supports an incremental encoder to acquire the motor position easily. The noise canceller is installed in the input pins, so that the signals from an incremental encoder or Hall sensor can be input directly.

The A-ENC provides six operation modes: encoder mode, sensor modes (3 kinds), timer mode, and phase counter mode.

Table 5.18 Built-in A-ENC

| Channel | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----------|------|------|------|------|------|------|------|
| Channel 0 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.19. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter respectively. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A have a interval timer, event counter, input capture, 2-phase counter input, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.19 Built-in T32A

| Channel | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----------|------|------|------|------|------|------|------|
| Channel 0 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 1 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 3 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 4 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Channel 5 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note1: ✓: Available, -: N/A

Note2: External pins are not same by product. Please refer to section "2 Pin Assignment".

5.20. Real Time Clock (RTC)

The RTC is a peripheral function that has a second counter, clock function, and leap-year calendar function. It also has the alarm function that generates an interrupt on a specified time and date.

Since the RTC operates on a low-speed external oscillation clock, it can operate in low-power consumption mode such as IDLE, STOP1 or STOP2 modes. In addition, the MCU can be returned from low-power consumption mode by an interrupt request of the RTC.

The RTC easily corrects a gain/loss of the clock caused by an error of low-speed oscillation frequency using the clock correction function.

Table 5.20 Built-in RTC

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----|------|------|------|------|------|------|------|
| RTC | ✓ | ✓ | ✓ | ✓ | ✓ | - | - |

Note: ✓: Available, -: N/A

5.21. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock ($f_{sys}/4$), internal oscillator 1 (f_{IHOSC1}), or internal oscillator 2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, change of a register can be forbidden until reset starts by setting to protected mode.(the count-clear function is possible)

Table 5.21 Built-in SIWDT

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|--------------|------|------|------|------|------|------|------|
| SIWDT | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.22. Remote signal receive Circuit (RMC)

The RMC is a peripheral function that receives signals excluding carrier signal from remote control reception signals. The RMC detects a leader signal to receive 72 bits data in a collective manner. Two data formats can be received: synchronous format and fixed-synchronous phase format.

In addition, it contains a digital noise canceller to avoid external noise.

Since the RMC operates on a low-frequency clock, it can operate in low power consumption mode, such as IDLE mode or STOP1 mode according to the setting (except STOP2). The MCU can also be returned from low-power consumption mode by an interrupt request of the RMC.

Table 5.22 Built-in RMC

| Channel | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|-----------------|------|------|------|------|------|------|------|
| Channel0 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Note: ✓: Available, -: N/A

5.23. Boundary Scan (BSC)

Boundary-Scan support the on-board Test. The TMPM3H group(1) provides a boundary-scan interface that is compatible with Joint Test Action Group (JTAG) specifications and uses the industry-standard JTAG protocol (IEEE Standard 1149.1·1990 <Includes IEEE Standard 1449.1a·1993>).

Table 5.23 Built-in BSC

| | M3H6 | M3H5 | M3H4 | M3H3 | M3H2 | M3H1 | M3H0 |
|----------------------|------|------|------|------|------|------|------|
| Boundary Scan | ✓ | ✓ | ✓ | ✓ | - | - | - |

Note: ✓: Available, -: N/A

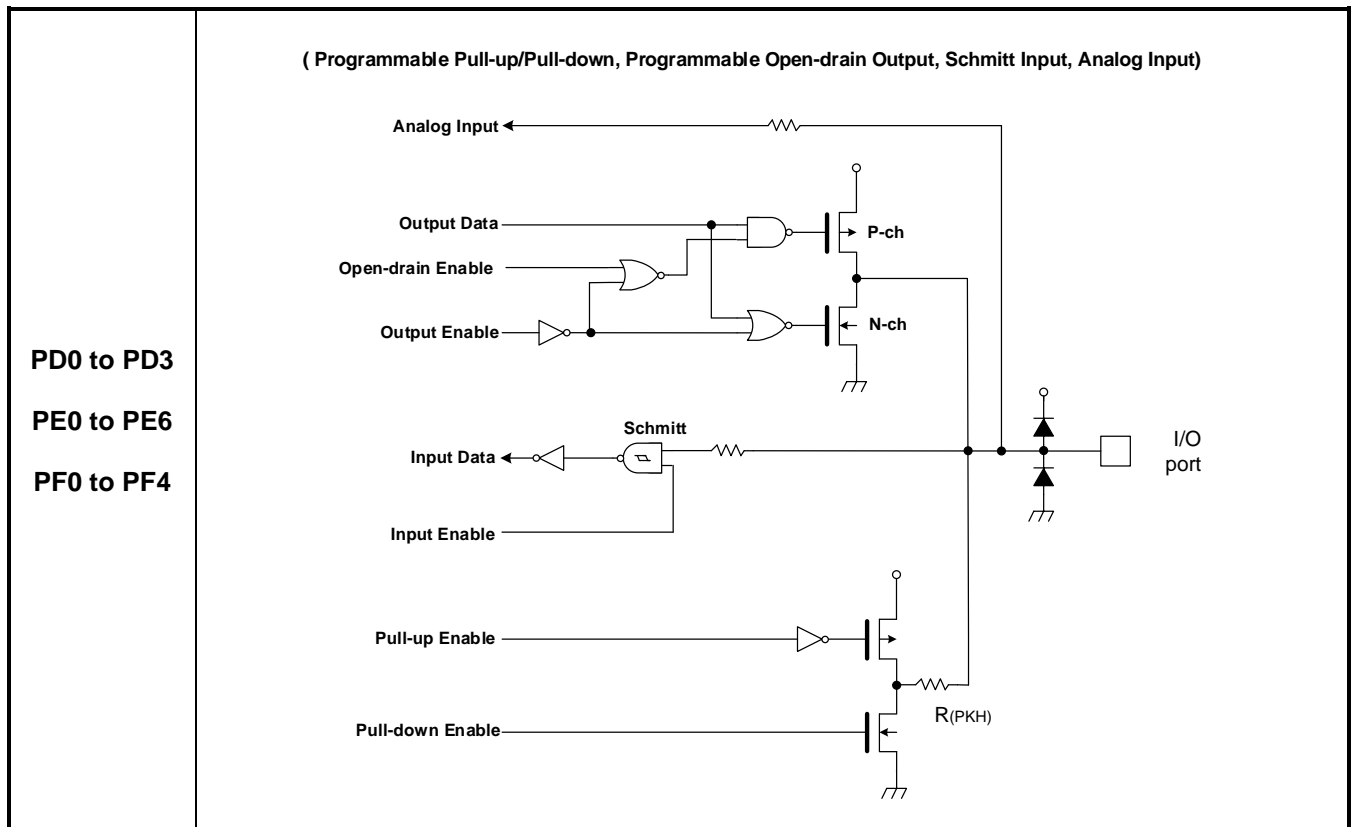
6. Equivalent Circuit

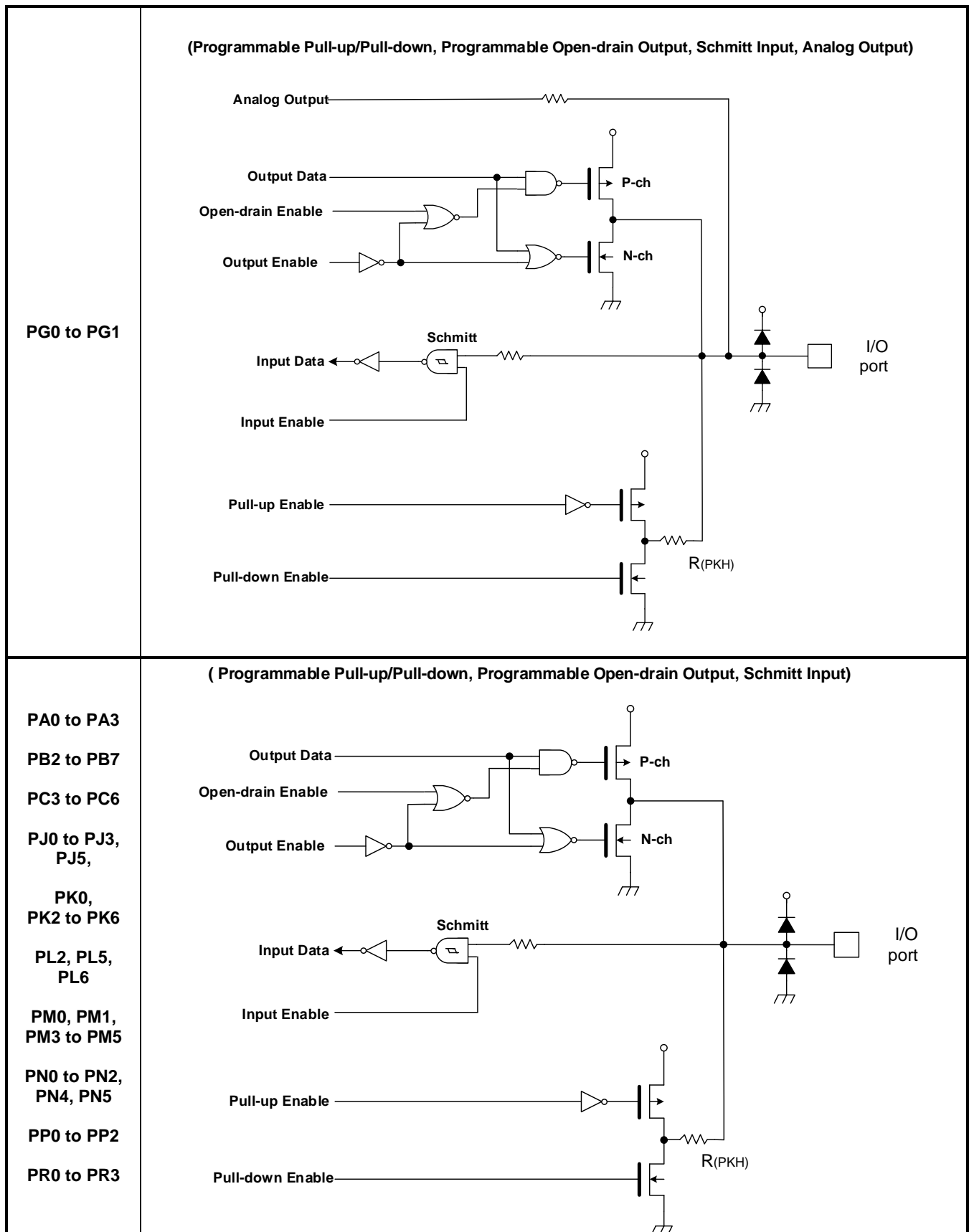
Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCXX] series.

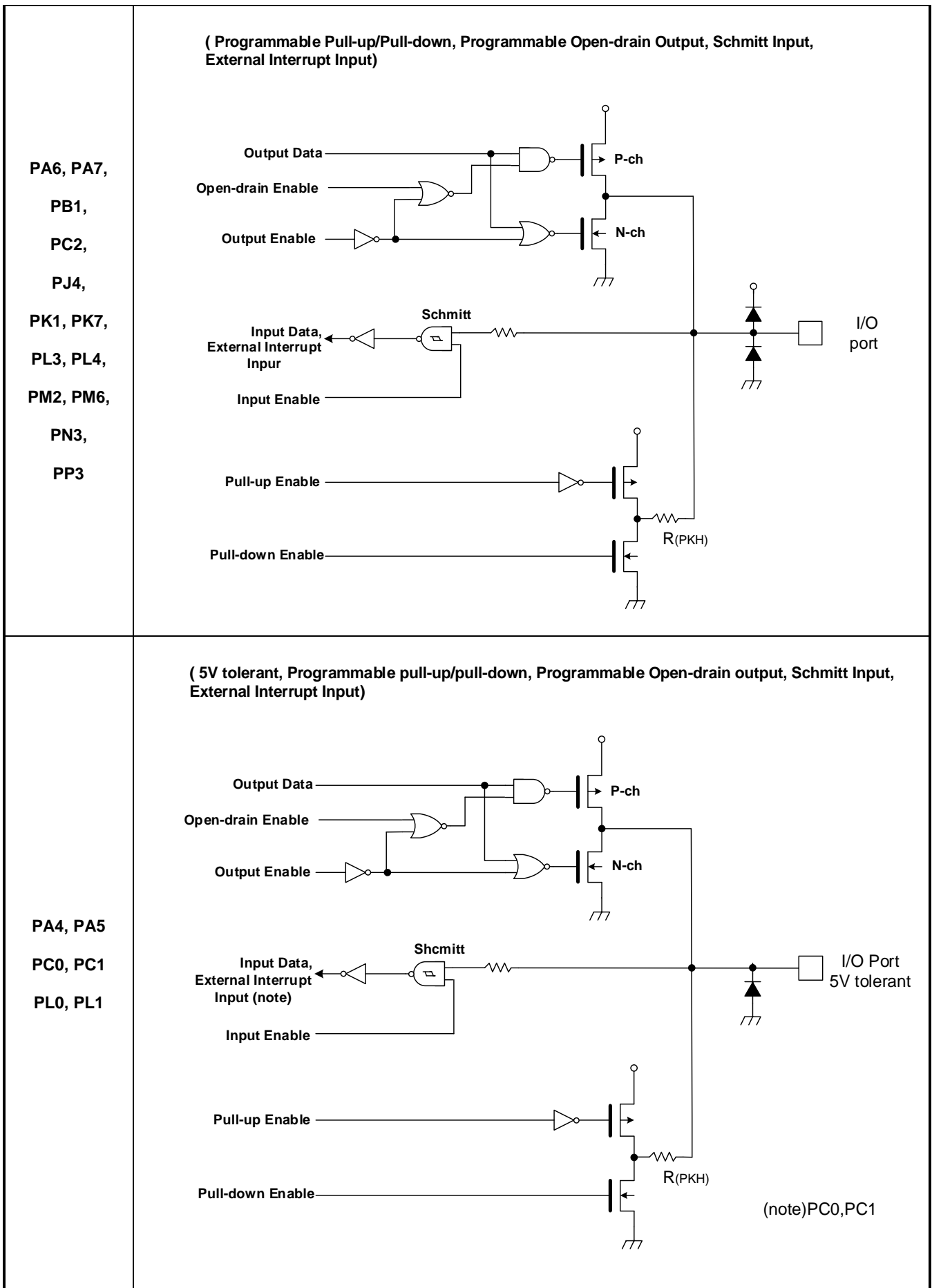
The input protection resistance ranges from several tens of Ω to several hundred Ω . Feedback resistor and Damping resistor are shown with a typical value.

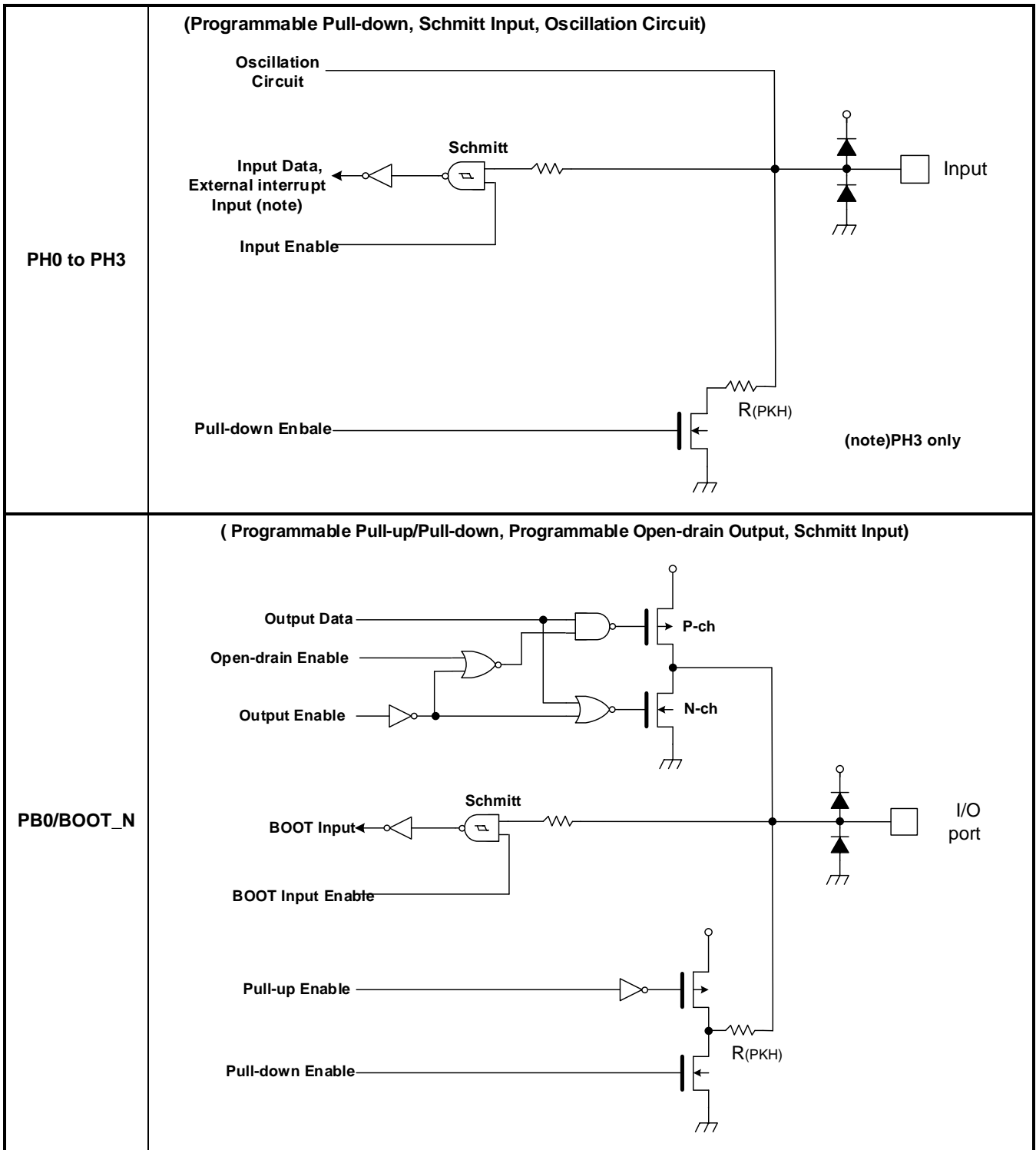
Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

6.1. Port

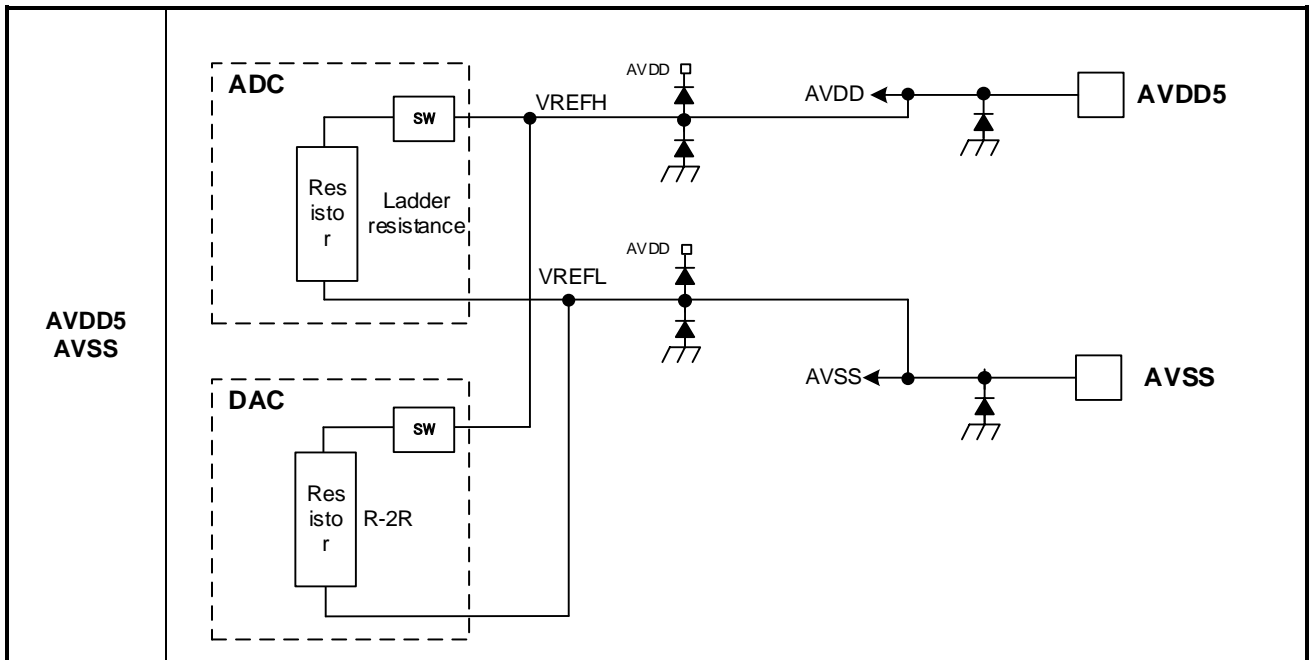






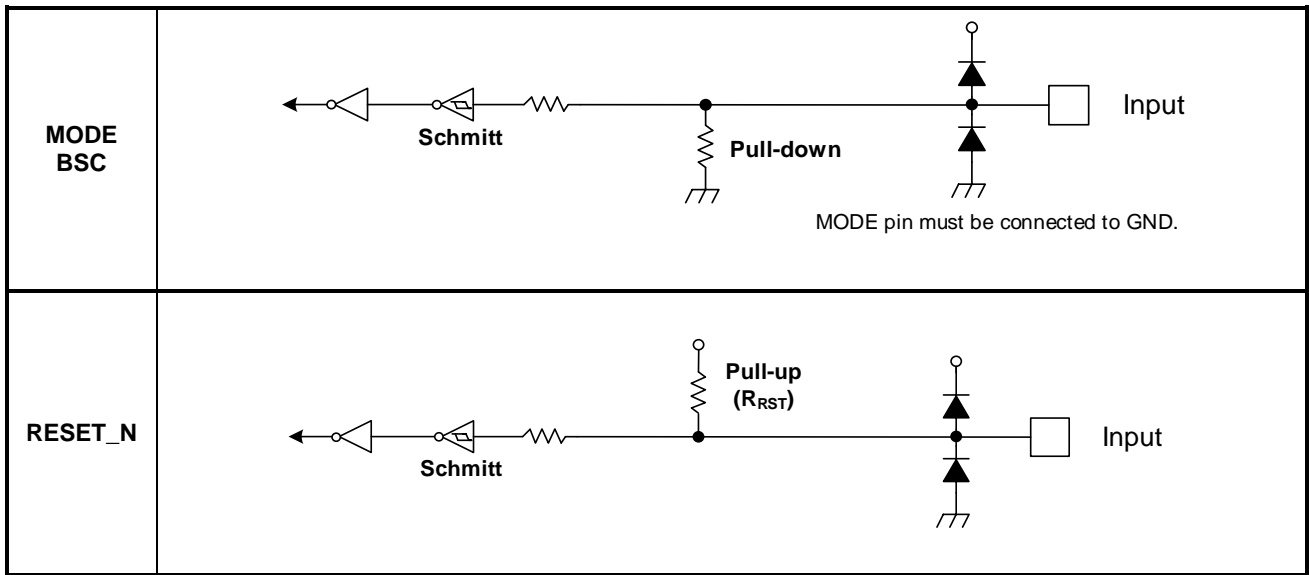


6.2. Analog Power pin

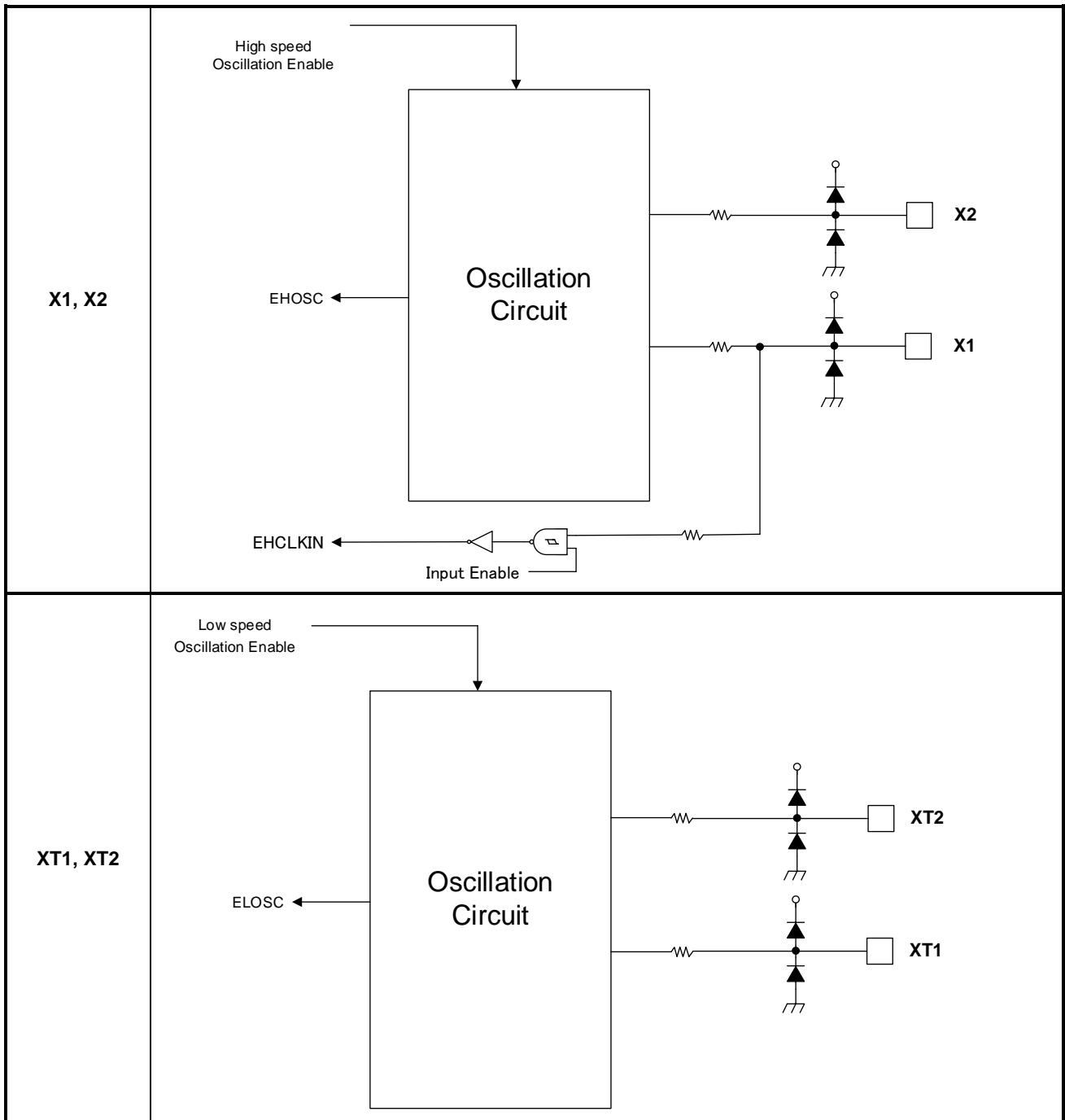


Note: SW: ON/OFF Switch Circuit

6.3. Control Pin



6.4. Clock control



7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

| Parameter | | Symbol | Rating | Unit |
|---|--|--------------------------------------|-------------------------------------|------|
| Power supply voltage | | DVDD5A DVDD5B DVDD5C | -0.3 to 6.0 | V |
| | | AVDD5 | -0.3 to DVDD5 (Note1) | |
| Capacitor pin voltage for voltage maintenance | | REGOUT1 | -0.3 to 1.7 | V |
| | | REGOUT2 | -0.3 to 3.9 | |
| Input voltage | PA0to3,PA6to7, PB1to7, PC2to6,PH0to3,PJ0to5, PK0to7,PL2to6,PM0to6, PN0to5,PP0to3,PR0to3, MODE,RESET_N,BOOT_N, BSC | V _{IN1} V _{IN2} | -0.3 to DVDD5+0.3(≤6.0V) (Note1) | V |
| | PD0to3, PE0to6, PF0to4, PG0to1 | V _{IN3} | -0.3 to AVDD5+0.3(≤6.0V) | |
| | PA4to5, PC0to1,PL0to1 | V _{IN4} | -0.3 to 6.0 | |
| Low level output current | Per pin PA0to3,PA6to7, PB0to7, PC2to6,PJ0to5, PK0to7,PL2to6,PM0to6, PN0to5,PP0to3,PR0to3 | I _{OL} | 5 | mA |
| | Per Pin PA4to5, PC0to1,PL0to1 | I _{OL4} | 25 | |
| | Total | ΣI _{OL} | 50 | |
| High level output current | Per pin PA0to7, PB0to7, PC0to6,PJ0to5, PK0to7, PL0to6, PM0to6, PN0to5,PP0to3, PR0to3 | I _{OH} | -5 | mA |
| | Total | ΣI _{OH} | -50 | |
| Power consumption (Ta= 85°C) | | PD | 500 | mW |
| Soldering temperature | | T _{SOLDER} | 260 | °C |
| Storage temperature | | T _{STG} | -55 to 125 | °C |
| Operational temperature | | T _{OPR} | -40 to 85 | °C |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C. DVDD5 and AVDD5 are used at the same voltage.

Note2: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

7.2. DC Electrical Characteristics (1/2)

$$4.5V \leq DVDD5=AVDD5 \leq 5.5V$$

$$DVSS = AVSS=0V$$

$$T_a = -40 \text{ to } 85 \text{ } ^\circ\text{C}$$

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit | |
|---------------------------|------------------------|--|--------------------------|-----------|------------|------|---|
| Power supply voltage | VDD | $f_{osc} = 6 \text{ to } 12\text{MHz}$ $f_{sys} = 1 \text{ to } 40\text{MHz}$ $f_s = 30 \text{ to } 34\text{kHz}$ | 4.5 | - | 5.5 | V | |
| Low level Input voltage | V_{IL1} V_{IL2} | PA0 to 3, PA6 to 7, PB1 to 7, PC2 to 6, PH0 to 3, PJ0 to 5, PK0 to 7, PL2 to 6, PM0 to 6, PN0 to 5, PP0 to 3, PR0 to 3, MODE, RESET_N, BOOT_N, BSC | -0.3 | - | DVDD5×0.25 | V | |
| | V_{IL3} | PD0 to 3, PE0 to 6, PF0 to 4, PG0 to 1 | | | AVDD5×0.25 | | |
| | V_{IL4} | PA4 to 5, PC0 to 1, PL0 to 1 | | | DVDD5×0.3 | | |
| High level Input voltage | V_{IH1} V_{IH2} | PA0 to 3, PA6 to 7, PB1 to 7, PC2 to 6, PH0 to 3, PJ0 to 5, PK0 to 7, PL2 to 6, PM0 to 6, PN0 to 5, PP0 to 3, PR0 to 3, MODE, RESET_N, BOOT_N, BSC | DVDD5×0.75 | - | DVDD5+0.3 | V | |
| | V_{IH3} | PD0 to 3, PE0 to 6, PF0 to 4, PG0 to 1 | | | AVDD5×0.75 | | |
| | V_{IH4} | PA4 to 5, PC0 to 1, PL0 to 1 | | | DVDD5×0.7 | | |
| Low level output voltage | V_{OL1} V_{OL2} | PA0 to 7, PB0 to 7, PC0 to 6, PJ0 to 5, PK0 to 7, PL0 to 6, PM0 to 6, PN0 to 5, PP0 to 3, PR0 to 3 | DVDD5=4.5V IOL=1.6mA | - | - | 0.4 | V |
| | V_{OL3} | PD0 to 3, PE0 to 6, PF0 to 4, PG0 to 1 | AVDD5=4.5V IOL=1.6mA | - | - | 0.4 | |
| | V_{OL4} | PA4 to 5, PC0 to 1, PL0 to 1 | DVDD5=4.5V IOL=8mA | - | - | 1.0 | |
| High level output voltage | V_{OH1} V_{OH2} | PA0 to 7, PB0 to 7, PC0 to 6, PJ0 to 5, PK0 to 7, PL0 to 6, PM0 to 6, PN0 to 5, PP0 to 3, PR0 to 3, PA4 to 5, | DVDD5=4.5V IOL=-1.6mA | DVDD5-0.4 | - | - | V |
| | V_{OH3} | PD0 to 3, PE0 to 6, PF0 to 4, PG0 to 1 | AVDD5=4.5V IOL=-1.6mA | AVDD5-0.4 | - | - | |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Typ. value is in $T_a = 25 \text{ } ^\circ\text{C}$, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

4.5V ≤ DVDD5=AVDD5 ≤ 5.5 V
DVSS=AVSS=0V
Ta= -40 to 85°C

| Parameter | | Symbol | Conditions | Min | Typ. | Max | Unit |
|--|---|-------------------|--|----------------|------|---------------|------|
| Input leak current | | I _{LI} | 0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5 | -5 | 0.05 | 5 | μA |
| Output leak current | | I _{LO} | 0.2 ≤ VIN ≤ DVDD5-0.2 0.2 ≤ VIN ≤ AVDD5-0.2 | -10 | 0.05 | 10 | |
| Schmitt trigger Input width | | VTH | DVDD5=AVDD5=5.0V | - | 1.0 | - | V |
| Reset pull-up resistor | | RRST | | 25 | 30 | 100 | kΩ |
| Programmable pull-up/-down resistor | | PKH | Pull-up | 25 | 30 | 100 | kΩ |
| | | | Pull-down | 25 | 50 | 100 | |
| Pin capacity (except power supply pin) | | C _{IO} | fc =1MHz | - | - | 10 | pF |
| Low level output current | Per pin except below ports | I _{OL} | DVDD5=5V AVDD5=5V | - | - | 2 (Note4) | mA |
| | Per pin PA4to5, PC0to1, PL0to1 | I _{OL4} | DVDD5=5V | - | - | 12 (Note4) | |
| | Total of PC0 to 6, PJ0 to 5, PK0 to 7,PN0 to 5, PP3, PR0 to 3 | ΣI _{OL1} | DVDD5=5V | - | - | 35 (Note5) | |
| | Total of PA0 to7, PB0 to7, PM0 to6, PL0 to6, PP0 to2 | ΣI _{OL2} | DVDD5=5V | - | - | 35 (Note5) | |
| | Total of PD0 to3,PE0 to6, PF0 to4,PG0 to1 | ΣI _{OL3} | AVDD5=5V | - | - | 20 (Note5) | |
| High level output current | per Pin | I _{OH} | DVDD5=5V AVDD5=5V | -2 (Note4) | - | - | mA |
| | Total of PC0 to 6, PJ0 to 5, PK0 to 7,PN0 to 5, PP3, PR0 to 3 | ΣI _{OH1} | DVDD5=5V | -35 (Note5) | - | - | |
| | Total of PA0 to7, PB0 to7, PM0 to6, PL0 to6, PP0 to2 | ΣI _{OH2} | DVDD5=5V | -35 (Note5) | - | - | |
| | Total of PD0 to3,PE0 to6, PF0 to4,PG0 to1 | ΣI _{OH3} | AVDD5=5V | -20 (Note5) | - | - | |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted

Note3: Apply same voltage to DVDD5 and AVDD5.

Note4: The current sum total of a terminal should not exceed the sum total of each group current.

Note5: The sum total of each group current should not exceed absolute maximum rating.

2.7V ≤ DVDD5=AVDD5 < 4.5V

DVSS = AVSS=0V

Ta=-40 to 85 °C

| Parameter | | Symbol | Conditions | Min | Typ. | Max | Unit |
|---------------------------|---|--------------------------------------|--|------------|------|------------|------|
| Power supply voltage | DVDD5A,DVDD5B,DVDD5C AVDD5 | VDD | f _{osc} = 6 to 12MHz f _{sys} = 1 to 40MHz fs = 30 to 34kHz | 2.7 | - | 4.5 | V |
| Low level Input voltage | PA0 to 3,PA6 to 7,PB1 to 7, PC2 to 6,PH0 to 3,PJ0 to 5, PK0 to 7,PL2 to 6, PM0 to 6, PN0 to 5,PP0 to 3,PR0 to 3, MODE,RESET_N,BOOT_N, BSC | V _{IL1} V _{IL2} | | -0.3 | - | DVDD5×0.25 | V |
| | PD0 to 3, PE0 to 6 PF0 to 4, PG0 to 1 | V _{IL3} | AVDD5×0.25 | | | | |
| | PA4 to 5, PC0 to 1, PL0 to 1 | V _{IL4} | DVDD5×0.3 | | | | |
| High level Input voltage | PA0 to 3,PA6 to 7,PB1 to 7, PC2 to 6, PH0 to 3,PJ0 to 5, PK0 to 7,PL2 to 6, PM0 to 6, PN0 to 5,PP0 to 3,PR0 to 3, MODE,RESET_N,BOOT_N, BSC | V _{IH1} V _{IH2} | | DVDD5×0.75 | - | DVDD5+0.3 | V |
| | PD0 to 3, PE0 to 6, PF0 to 4, PG0 to 1 | V _{IH3} | AVDD5×0.75 | | | AVDD5+0.3 | |
| | PA4 to 5, PC0 to 1, PL0 to 1 | V _{IH4} | DVDD5×0.7 | | | DVDD5+0.3 | |
| Low level output voltage | PA0 to 7,PB0 to 7,PC0 to 6, PJ0 to 5, PK0 to 7,PL0 to 6, PM0 to 6 ,PN0 to 5, PP0 to 3, PR0 to 3 | V _{OL1} V _{OL2} | DVDD5=2.7V IOL= 0.8mA | - | - | 0.4 | V |
| | PD0 to 3,PE0 to 6,PF0 to 4, PG0 to 1 | V _{OL3} | AVDD5=2.7V IOL= 0.8mA | - | - | 0.4 | |
| | PA4 to 5,PC0 to 1, PL0 to 1 | V _{OL4} | DVDD5=2.7V IOL= 4mA | - | - | 1.0 | |
| High level output voltage | PA0 to 7,PB0 to 7,PC0 to 6, PJ0 to 5,PK0 to 7,PL0 to 6, PM0 to 6,PN0 to 5, PP0 to 3, PR0 to 3, PA4 to 5, | V _{OH1} V _{OH2} | DVDD5=2.7V IOL= -0.8mA | DVDD5-0.4 | - | - | V |
| | PD0 to 3, PE0 to 6,PF0 to 4, PG0 to 1 | V _{OH3} | AVDD5=2.7V IOL= -0.8mA | AVDD5-0.4 | - | - | |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

2.7V ≤ DVDD5=AVDD5 < 4.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

| Parameter | | Symbol | Conditions | Min | Typ. | Max | Unit |
|--|---|-------------------|--|----------------|------|---------------|------|
| Input leak current | | I _{LI} | 0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5 | -5 | 0.05 | 5 | μA |
| Output leak current | | I _{LO} | 0.2 ≤ VIN ≤ DVDD5-0.2 0.2 ≤ VIN ≤ AVDD5-0.2 | -10 | 0.05 | 10 | |
| Schmitt trigger Input width | | V _{TH} | DVDD5=AVDD5=3V | - | 0.5 | - | V |
| Reset pull-up resistor | | RRST | | 25 | 100 | 200 | kΩ |
| Programmable pull-up/-down resistor | | PKH | Pull-up | 25 | 100 | 200 | |
| | | | Pull-down | 25 | 100 | 200 | |
| Pin capacity (except power supply pin) | | C _{IO} | fc =1MHz | - | - | 10 | pF |
| Low level output current | Per pin except below ports | I _{OL} | DVDD5=3V AVDD5=3V | - | - | 1 (Note4) | mA |
| | Per pin PA4to5, PC0to1, PL0to1 | I _{OL4} | DVDD5=3V | - | - | 6 (Note4) | |
| | Total of PC0 to 6, PJ0 to 5, PK0 to 7,PN0 to 5, PP3, PR0 to 3 | ΣI _{OL1} | DVDD5=3V | - | - | 18 (Note5) | |
| | Total of PA0 to7,PB0 to7, PM0 to6, PL0 to6, PP0 to2 | ΣI _{OL2} | DVDD5=3V | - | - | 18 (Note5) | |
| | Total of PD0 to3,PE0 to6, PF0 to4,PG0 to1 | ΣI _{OL3} | AVDD5=3V | - | - | 10 (Note5) | |
| High level output current | per Pin | I _{OH} | DVDD5=3V AVDD5=3V | -1 (Note4) | - | - | mA |
| | Total of PC0 to 6, PJ0 to 5, PK0 to 7,PN0 to 5, PP3, PR0 to 3 | ΣI _{OH1} | DVDD5=3V | -18 (Note5) | - | - | |
| | Total of PA0 to7, PB0 to7, PM0 to6, PL0 to6, PP0 to2 | ΣI _{OH2} | DVDD5=3V | -18 (Note5) | - | - | |
| | Total of PD0 to3,PE0 to6, PF0 to4,PG0 to1 | ΣI _{OH3} | AVDD5=3V | -10 (Note5) | - | - | |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

Note4: The current sum total of a terminal should not exceed the sum total of each group current.

Note5: The sum total of each group current should not exceed absolute maximum rating.

7.3. DC Electrical Characteristics (2/2)

Ta = -40 to 85°C

| Parameter | Symbol | Conditions | | | | Min | Typ. (Note2) | Max | Unit |
|-----------|-----------------|--------------------------|---|----------------------|---|-----|--------------|------|------|
| | | Supply voltage | High-speed oscillator | Low-speed oscillator | Operating condition | | | | |
| Normal | I _{DD} | DVDD5= AVDD5= 5.5V | Refer to the table 7.2 and 7.3 for detail | | | - | 9.5 | 12.5 | mA |
| IDLE | | | Oscillation | Oscillation | Refer to the table 7.2 and 7.3 for detail | - | 1.2 | 3.7 | |
| STOP1 | | | Stop | Oscillation | | - | 140 | 1900 | μA |
| STOP2 | | | | Stop | | - | 13 | 100 | |
| | | | | | - | 12 | 100 | | |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

Note4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit)

| | | NORMAL | IDLE | STOP1 | STOP2 | |
|---|--|---------------------------------|------|-------|----------|-----------|
| | | | | | LOSC run | LOSC stop |
| Pin setting | DVDD5= AVDD5= | 5.0V(Typ.), 5.5V(max) | | | | |
| | X1,X2 | Oscillator connected (10MHz) | | | | |
| | XT1,XT2 | Oscillator connected(32.768kHz) | | | | |
| | Input pins | Fixed | | | | |
| | Output pins | Open | | | | |
| Operation condition (Oscillation Circuit) | System clock (fsys) | 40MHz | Stop | | | |
| | External High-speed frequency oscillator (EHOSC) | Oscillation | Stop | | | |
| | Internal High-speed frequency oscillator (IHOSC) | Stop | | | | |
| | PLL | run(4times) | Stop | | | |
| | Low-speed oscillator (ELOC) | Oscillation | | | | Stop |

Table 7.3 IDD measurement condition (CPU, Peripheral)

| Peripheral | unit number | NORMAL | IDLE | STOP1 | STOP2 |
|-------------------|-------------|--|------|------------------|-----------|
| | | | | LOSC oscillation | LOSC stop |
| CPU | 1 | Run (Dhrystone Ver.2.1) | | Stop | |
| DMAC | 1 | (Request from UARTch0 TX, destination: RAM) | | Stop | |
| ADC | 1 | Run (1.5μs, Repeated conversion) | | Stop | |
| DAC | 2 | Run | | Stop | |
| T32A | 6 | All Ch: Run | | Stop | |
| PMD+ | 1 | Run | | Stop | |
| A-ENC | 1 | Run | | Stop | |
| RTC | 1 | | Run | | |
| SIWDT | 1 | Run | | Stop | |
| UART | 3 | All ch: UART, Transmission(2.5Mbps) | | Stop | |
| I ² C | 3 | | | Stop | |
| TSPI | 2 | Ch0, Ch1: Transmission(20MHz) | | Stop | |
| RMC | 1 | Run | | Stop | |
| LVD | 1 | | | Stop | |
| OFD | 1 | | | Stop | |
| Input Output Port | - | Run | | Stop | |

f_{sys}=40MHz

T_a=-40 to 85°C

| Item | Symbol | Condition | Min | Typ. | Max | Unit |
|--------------------------------------|-------------------|-----------|-----|------|-----|------|
| Current consumption (ADC,DAC run) | I _{AVDD} | AVDD=5.0V | - | 3.3 | 4 | mA |
| | | AVDD=3.0V | - | 2 | 3.2 | |

7.4. 12-bit AD Converter Characteristics

DVDD5=AVDD5=2.7V to 5.5V

DVSS=AVSS=0V

Ta= -40 to 85°C

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|---------------------------------------|-------------------|---|-----------|------|---------------|------|
| Analog reference voltage (+) | AVDD5 (VREFH) | | AVDD5-0.3 | - | AVDD5+0.3 | V |
| Analog input voltage | VAIN | | AVSS | - | AVDD5 (VREFH) | V |
| Integral nonlinearity error (INL) | - | 4.5 ≤ AVDD5 ≤ 5.5 AIN load resistor = 600 Ω AIN load capacity ≥ 0.1 μF Conversion time = 1.5 μs | -3.5 | - | 3.5 | LSB |
| Differential nonlinearity error (DNL) | | | -2 | - | 2.5 | |
| Zero-scale error | | | -1.5 | - | 5 | |
| Full-scale error | | | -5 | - | 6 | |
| Total errors | | | -6 | - | 6 | |
| Integral nonlinearity error (INL) | - | 2.7 ≤ AVDD5 < 4.5 AIN load resistor = 600 Ω AIN load capacity ≥ 0.1 μF Conversion time = 2.95 μs | -4 | - | 4 | LSB |
| Differential nonlinearity error (DNL) | | | -2 | - | 4 | |
| Zero-scale error | | | -3 | - | 6.5 | |
| Full-scale error | | | -6 | - | 7.5 | |
| Total errors | | | -7.5 | - | 7.5 | |
| Stable time | t _{sta} | After [ADMOD0]<DACON>= 1 is set. | 3 | - | - | μs |
| Conversion time | t _{conv} | 4.5V ≤ AVDD5 ≤ 5.5V SCLK=40MHz (Note3) | 1.5 | - | 16.3 | |
| | | 2.7V ≤ AVDD5 < 4.5V SCLK=40MHz (Note3) | 2.95 | - | 16.65 | |

Note1: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 4096 [V]

Note2: This is the characteristic in case only AD converter is operation

Note3: For detail of setting, refer to "Analog to Digital Converter" of the reference manual.

DVDD5=AVDD5=2.7V to 5.5V

DVSS=AVSS=0V

Ta= -40 to 85°C

| Parameter | Conditions | Min | Typ. | Max | Unit |
|-----------------|---------------|-----|------|-----|------|
| Reference power | ch18 selected | 1.1 | - | 1.3 | V |

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.5. 8-bit DA Converter Characteristics

DVDD5=AVDD5=2.7V to 5.5V

DVSS=AVSS=0V

Ta= -40 to 85°C

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|---------------------------------------|------------------|-------------------------------------|-----------|------|-----------|------|
| Analog reference voltage (+) | AVDD5 (VREFH) | | AVDD5-0.3 | - | AVDD5+0.3 | V |
| Integral nonlinearity error (INL) | - | 4.5V ≤ AVDD5 ≤ 5.5V Rload = 10MΩ | -1 | - | +1 | LSB |
| Differential nonlinearity error (DNL) | | | -1 | - | +1 | |
| Total errors | | | -1 | - | +1 | |
| Integral nonlinearity error (INL) | - | 2.7V ≤ AVDD5 < 4.5V Rload = 10MΩ | -2 | - | +2 | LSB |
| Differential nonlinearity error (DNL) | | | -1 | - | +1 | |
| Total errors | | | -2 | - | +2 | |
| Stable time | t _{sta} | Cload = 20pF | 4.5 | - | - | μs |

Note1; DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5V, unless otherwise noted.

Note3: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 256 [V]

Note4: This is the characteristic in case only DA converter is operating.

7.6. Characteristics of Internal processing at RESET

DVSS=AVSS=0V
Ta= -40to 85°C

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|------------------------------------|--------------------|-------------------------------------|------|------|------|-------|
| Internal Initialized time | t _{INIT} | Power-On | - | - | 2.15 | ms |
| | | STOP2 Release by RESET with RESET_N | - | - | 1.8 | |
| | | STOP2 Release by Interrupt | - | - | 1.55 | |
| Internal processing time for Reset | t _{IRST} | | 0.16 | - | 0.2 | |
| Waiting time till CPU running | t _{CPUWT} | Cold Reset | 12 | - | 15 | μs |
| | | Warm Reset | 55 | - | 90 | |
| Power-on rising gradient | V _{PON} | | 0.01 | - | 100 | mV/μs |

7.7. Characteristics of Power-on Reset

DVSS=AVSS=0V
Ta= -40 to 85°C

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit |
|-----------------------|-------------------|------------|------|------|------|------|
| Detection voltage | V _{PREL} | Power-up | 2.25 | 2.4 | 2.55 | V |
| | V _{PDET} | Power-down | 2.2 | 2.35 | 2.5 | |
| Detection pulse width | T _{PDET} | | 200 | - | - | μs |

7.8. Characteristics of Voltage Detection Circuit

DVDD5=AVDD5=2.7V to 5.5V

DVSS=AVSS=0V

Ta= -40 to 85°C

| Parameter | Symbol | Conditions | Min | Typ. | Max | Unit | |
|-------------------------------|-------------------------|--------------------|------------|------|------|------|----|
| Detection voltage | V _{LVL0} | Power-up | 2.55 | 2.65 | 2.75 | V | |
| | | Power-down | 2.5 | 2.6 | 2.7 | | |
| | V _{LVL1} | Power-up | 2.65 | 2.75 | 2.85 | V | |
| | | Power-down | 2.6 | 2.7 | 2.8 | | |
| | V _{LVL2} | Power-up | 2.75 | 2.85 | 2.95 | V | |
| | | Power-down | 2.7 | 2.8 | 2.9 | | |
| | V _{LVL3} | Power-up | 2.85 | 2.95 | 3.05 | V | |
| | | Power-down | 2.8 | 2.9 | 3.0 | | |
| | V _{LVL4} | Power-up | 3.75 | 3.85 | 3.95 | V | |
| | | Power-down | 3.7 | 3.8 | 3.9 | | |
| | V _{LVL5} | Power-up | 3.95 | 4.05 | 4.15 | V | |
| | | Power-down | 3.9 | 4.0 | 4.1 | | |
| | V _{LVL6} | Power-up | 4.15 | 4.25 | 4.35 | V | |
| | | Power-down | 4.1 | 4.2 | 4.3 | | |
| | V _{LVL7} | Power-up | 4.35 | 4.45 | 4.55 | V | |
| | | Power-down | 4.3 | 4.4 | 4.5 | | |
| | Detection response time | t _{VDDT1} | Power-down | - | 50 | 200 | μs |
| | Detection Release time | t _{VDDT2} | Power-up | - | 250 | - | |
| Setup time | t _{LV DEN} | | - | - | 100 | | |
| Detection Minimum pulse width | t _{LVDPW} | | 200 | - | - | | |

7.9. AC Electrical Characteristics

7.9.1. Serial Peripheral Interface (TSPI)

7.9.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Output level: High = $0.8 \times DVDD5$, Low = $0.2 \times DVDD5$
- Input level: High = $0.75 \times DVDD5$, Low = $0.25 \times DVDD5$
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of k1 is specified with [TSPIxFMTR0]<CSSCKDL[3:0]>; the value of k2 is specified with [TSPIxFMTR0]<SCKCSDL[3:0]>. These values are 1 to 16.

(1) Master mode

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V

| Parameter | Symbol | Calculation | | fsys = 40MHz k1=k2=1 | | Unit |
|--|--------------------|--------------------------------------|--------------------------------------|-------------------------|-----|------|
| | | Min | Max | Min | Max | |
| TSPIxSCK output frequency | f _{CYC} | - | 20 | - | 20 | MHz |
| TSPIxSCK output cycle | t _{CYC} | 50 | - | 50 | - | ns |
| TSPIxSCK low level output pulse width | t _{WL} | (t _{CYC} /2) - 13 | - | 12 | - | |
| TSPIxSCK high level output pulse width | t _{WH} | (t _{CYC} /2) - 13 | - | 12 | - | |
| TSPIxCSn output ← TSPIxSCK rise/fall time | t _{CSU} | (t _{CYC} × k1) - 20 | (t _{CYC} × k1) + 15 | 30 | 65 | |
| TSPIxSCK rise/fall time → TSPIxCSn hold time | t _{CHD} | (t _{CYC} × (k2 + 0.5)) - 20 | - | 55 | - | |
| TSPIxRXD Input ← TSPIxSCK rise/fall time | t _{DSU} | 35 - T(Notes) | - | 10 | - | |
| TSPIxSCK rise/fall time → TSPIxRXD hold time | t _{DHD} | T (Notes) | - | 25 | - | |
| TSPIxSCK rise/fall time → TSPIxTXD delay time | t _{ODLY1} | -18 | - | -18 | - | |
| TSPIxSCK rise/fall time → TSPIxTXD delay time | t _{ODLY2} | - | 16 | - | 16 | |
| TSPIxCSIN fall → TSPIxTXD delay time | t _{ODLY3} | (t _{CYC} × (k1 - 0.5)) - 25 | (t _{CYC} × (k1 - 0.5)) + 17 | 0 | 42 | |

Note: In this case [TSPIxCR]<RXDLY>=0

2.7V ≤ DVDD5=AVDD5 < 4.5V
for TSP11, TSP12, TSP13

| Parameter | Symbol | Calculation | | fsys = 40MHz k1=k2=1 | | Unit |
|--|--------------------|--------------------------------------|--------------------------------------|-------------------------|-----|------|
| | | Min | Max | Min | Max | |
| TSP1xSCK output frequency | f _{CYC} | - | 20 | - | 20 | MHz |
| TSP1xSCK output cycle | t _{CYC} | 50 | - | 50 | - | ns |
| TSP1xSCK low level output pulse width | t _{WL} | (t _{CYC} /2) - 16 | - | 9 | - | |
| TSP1xSCK high level output pulse width | t _{WH} | (t _{CYC} /2) - 16 | - | 9 | - | |
| TSP1xCSn output ← TSP1xSCK rise/fall time | t _{CSU} | (t _{CYC} × k1) - 20 | (t _{CYC} × k1) + 20 | 30 | 70 | |
| TSP1xSCK rise/fall time → TSP1xCSn hold time | t _{CHD} | (t _{CYC} × (k2 + 0.5)) - 20 | - | 55 | - | |
| TSP1xRXD Input ← TSP1xSCK rise/fall time | t _{DSU} | 46 - T(Notes) | - | 21 | - | |
| TSP1xSCK rise/fall time → TSP1xRXD hold time | t _{DHD} | T (Notes) | - | 25 | - | |
| TSP1xSCK rise/fall time → TSP1xTXD delay time | t _{ODLY1} | -24 | - | -24 | - | |
| TSP1xSCK rise/fall time → TSP1xTXD delay time | t _{ODLY2} | - | 21 | - | 21 | |
| TSP1xCSIN fall → TSP1xTXD delay time | t _{ODLY3} | (t _{CYC} × (k1 - 0.5)) - 25 | (t _{CYC} × (k1 - 0.5)) + 21 | 0 | 46 | |

Note: In this case [TSP1xCR2] < RXDLY > = 0

2.7V ≤ DVDD5=AVDD5 < 4.5V
for TSP10

| Parameter | Symbol | Calculation | | fsys = 40MHz k1=k2=1 | | Unit |
|--|--------------------|--------------------------------------|--------------------------------------|-------------------------|-----|------|
| | | Min | Max | Min | Max | |
| TSP1xSCK output frequency | f _{CYC} | - | 20 | - | 20 | MHz |
| TSP1xSCK output cycle | t _{CYC} | 50 | - | 50 | - | ns |
| TSP1xSCK low level output pulse width | t _{WL} | (t _{CYC} /2) - 16 | - | 9 | - | |
| TSP1xSCK high level output pulse width | t _{WH} | (t _{CYC} /2) - 16 | - | 9 | - | |
| TSP1xCSn output ← TSP1xSCK rise/fall time | t _{CSU} | (t _{CYC} × k1) - 34 | (t _{CYC} × k1) + 20 | 16 | 70 | |
| TSP1xSCK rise/fall time → TSP1xCSn hold time | t _{CHD} | (t _{CYC} × (k2 + 0.5)) - 20 | - | 55 | - | |
| TSP1xRXD Input ← TSP1xSCK rise/fall time | t _{DSU} | 46 - T(Notes) | - | 21 | - | |
| TSP1xSCK rise/fall time → TSP1xRXD hold time | t _{DHD} | T (Notes) | - | 25 | - | |
| TSP1xSCK rise/fall time → TSP1xTXD delay time | t _{ODLY1} | -24 | - | -24 | - | |
| TSP1xSCK rise/fall time → TSP1xTXD delay time | t _{ODLY2} | - | 21 | - | 21 | |
| TSP1xCSIN fall → TSP1xTXD delay time | t _{ODLY3} | (t _{CYC} × (k1 - 0.5)) - 39 | (t _{CYC} × (k1 - 0.5)) + 24 | -14 | 49 | |

Note: In this case [TSP1xCR2] < RXDLY > = 0

(2) Slave mode

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V

| Parameter | Symbol | Calculation | | fsys = 40MHz k1=1 | | Unit |
|--|--------------------|--|-------------------------------------|----------------------|-----|------|
| | | Min | Max | Min | Max | |
| TSPIxSCK Input frequency | f _{CYC} | - | 10 | - | 10 | MHz |
| TSPIxSCK Input cycle | t _{CYC} | 100 | - | 100 | - | ns |
| TSPIxSCK low level Input pulse width | t _{WL} | t _{CYC} / 2 - 13 | - | 37 | - | |
| TSPIxSCK high level Input pulse width | t _{WH} | t _{CYC} / 2 - 13 | - | 37 | - | |
| TSPIxCSIN Input ← TSPIxSCK rise/fall time | t _{CSU1} | (t _{CYC} × (k1 + 0.5)) +20 | - | 170 | - | |
| TSPIxCSIN Input ← TSPIxSCK rise/fall time | t _{CSU2} | (t _{CYC} × k1) - 20 | - | 80 | - | |
| TSPIxSCK rise/fall time → TSPIxCSIN hold time | t _{CHD} | 5 | - | 5 | - | |
| TSPIxRXD Input ← TSPIxSCK rise/fall time | t _{DSU} | 7 | - | 7 | - | |
| TSPIxSCK rise/fall → TSPIxRXD hold time | t _{DHD} | 10 | - | 10 | - | |
| TSPIxSCK rise/fall → TSPIxTXD delay time | t _{ODLY1} | 0 | - | 0 | - | |
| TSPIxSCK rise/fall → TSPIxTXD delay time | t _{ODLY2} | - | 36 | - | 36 | |
| TSPIxCSIN fall → TSPIxTXD delay time | t _{ODLY3} | - | (t _{CYC} × (k1 - 0.5)) + 5 | - | 55 | |
| TSPIxCSIN high level input pulse width | t _{WDIS} | T × 2 + 20 | - | 70 | - | |

2.7V ≤ DVDD5=AVDD5 < 4.5V

| Parameter | Symbol | Calculation | | fsys = 40MHz k1=1 | | Unit |
|--|--------------------|--|-------------------------------------|----------------------|-----|------|
| | | Min | Max | Min | Max | |
| TSPIxSCK Input frequency | f _{CYC} | - | 10 | - | 10 | MHz |
| TSPIxSCK Input cycle | t _{CYC} | 100 | - | 100 | - | ns |
| TSPIxSCK low level Input pulse width | t _{WL} | t _{CYC} / 2 - 13 | - | 37 | - | |
| TSPIxSCK high level Input pulse width | t _{WH} | t _{CYC} / 2 - 13 | - | 37 | - | |
| TSPIxCSIN Input ← TSPIxSCK rise/fall time | t _{CSU1} | (t _{CYC} × (k1 + 0.5)) +20 | - | 170 | - | |
| TSPIxCSIN Input ← TSPIxSCK rise/fall time | t _{CSU2} | (t _{CYC} × k1) - 20 | - | 80 | - | |
| TSPIxSCK rise/fall time → TSPIxCSIN hold time | t _{CHD} | 5 | - | 5 | - | |
| TSPIxRXD Input ← TSPIxSCK rise/fall time | t _{DSU} | 7 | - | 7 | - | |
| TSPIxSCK rise/fall → TSPIxRXD hold time | t _{DHD} | 10 | - | 10 | - | |
| TSPIxSCK rise/fall → TSPIxTXD delay time | t _{ODLY1} | 0 | - | 0 | - | |
| TSPIxSCK rise/fall → TSPIxTXD delay time | t _{ODLY2} | - | 48 | - | 48 | |
| TSPIxCSIN fall → TSPIxTXD delay time | t _{ODLY3} | - | (t _{CYC} × (k1 - 0.5)) + 5 | - | 55 | |
| TSPIxCSIN high level input pulse width | t _{WDIS} | T × 2 + 20 | - | 70 | - | |

(1) 1st clock edge sampling (Master)

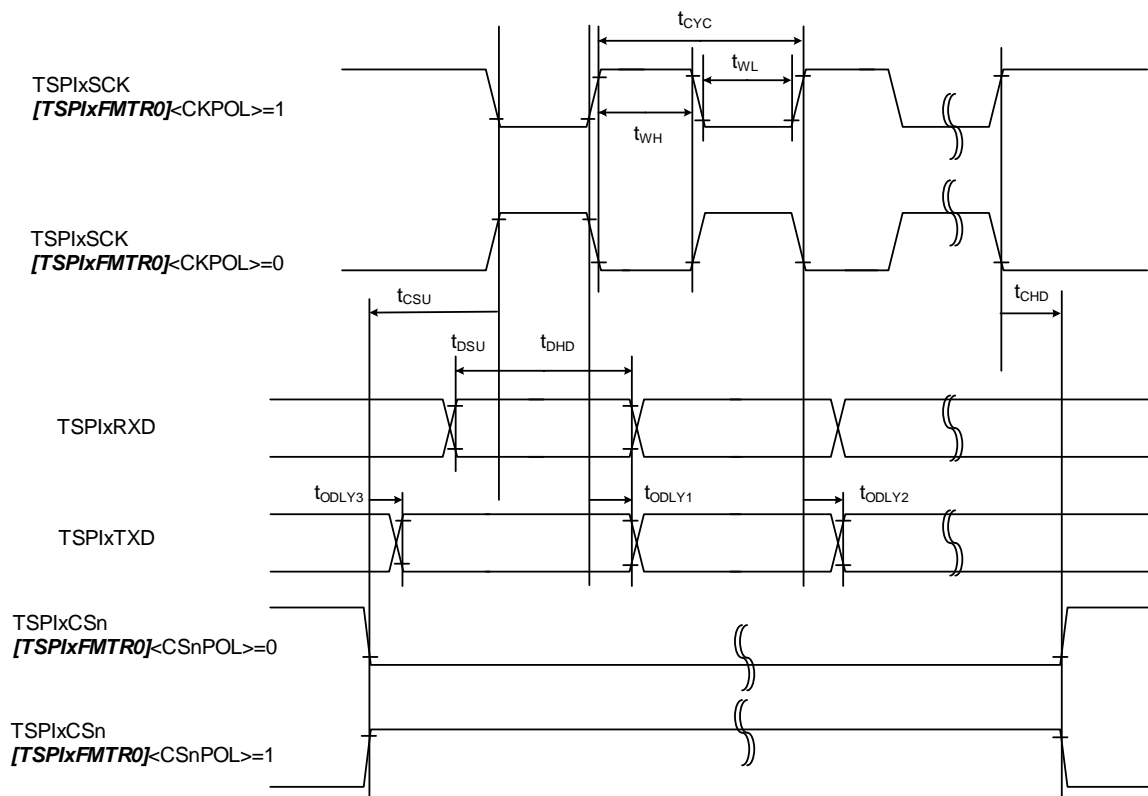


Figure 7.1 1st clock edge sampling (Master)

(2) 2nd clock edge sampling (Master)

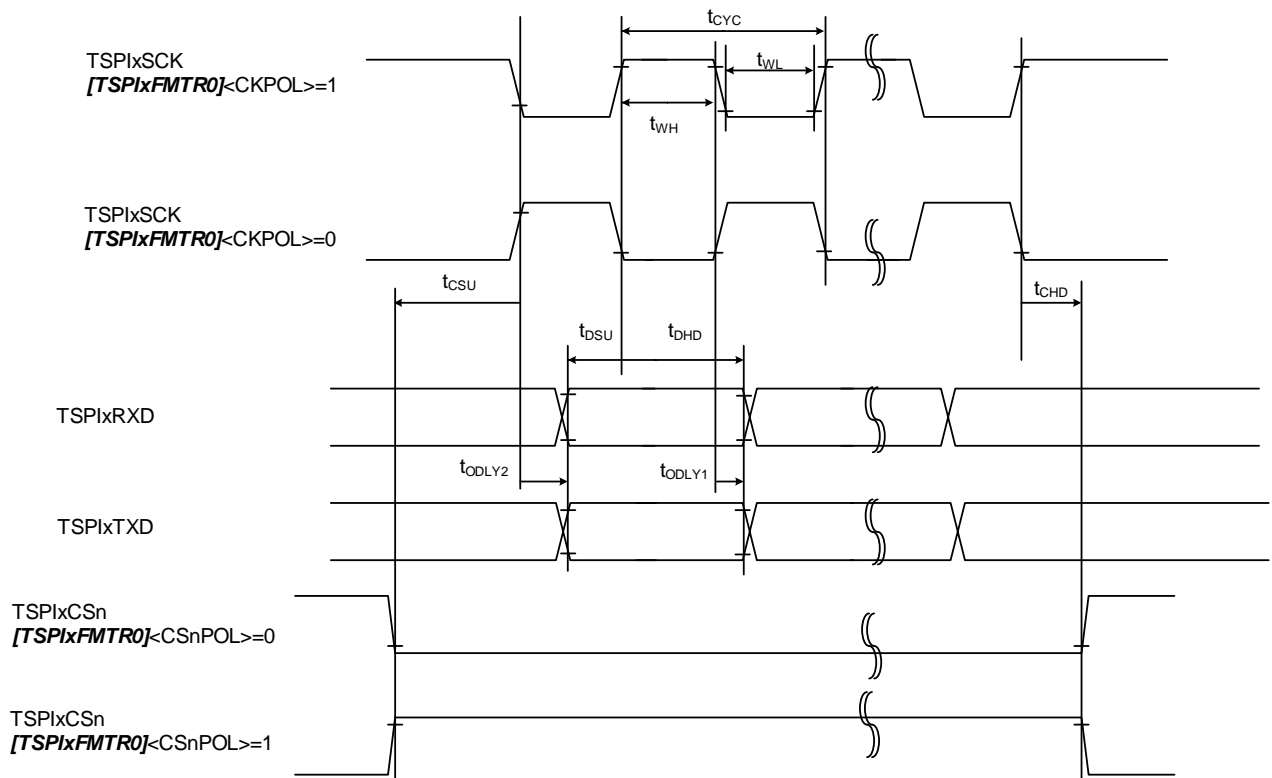


Figure 7.2 2nd clock edge sampling (Master)

(3) 2nd clock edge sampling (slave)

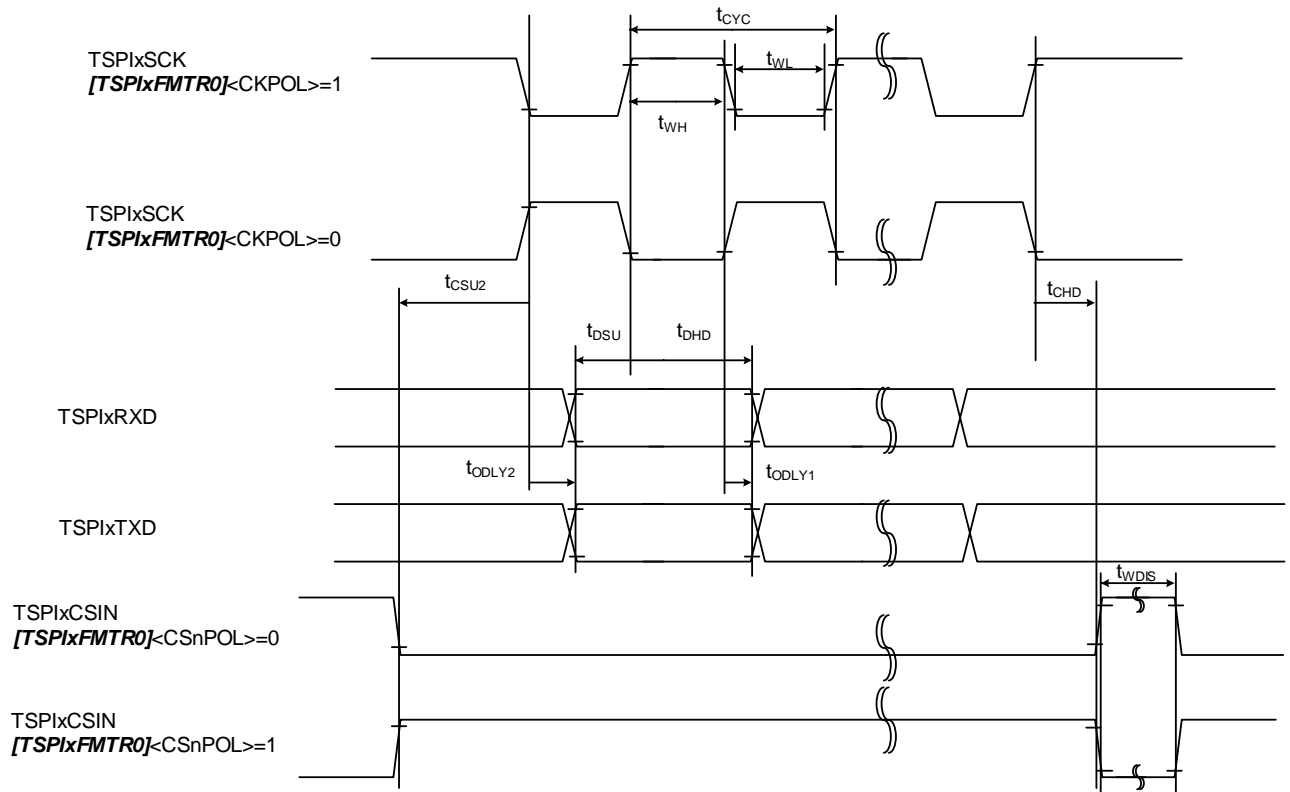


Figure 7.3 2nd clock edge sampling (Slave)

7.9.2. I²C Interface (I²C)

7.9.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7v to 5.5V
- Ta = -40 to 85°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.2.2. AC Electrical Characteristics

T indicates the Operation clock cycle of I²C. The I²C operation clock is as same as the system clock (fsys) cycle. It is depend on the Clock Gear setup.

The value of n is the SCL output clock frequency specified with $[I2CxCR]<SCK>$. The value of p is the prescaler dividing ratio specified with $[I2CxPRS]<PRsCK>$.

| Parameter | Symbol | Standard mode | | Fast mode | | Fast mode+ | | Unit |
|--|----------------------|---------------|-----|-----------|-----|------------|------|------|
| | | Min | Max | Min | Max | Min | Max | |
| SCL clock frequency | f _{SCL} | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| Start condition hold time | t _{HD, STA} | 4.0 | - | 0.6 | - | 0.26 | - | μs |
| SCL clock Low width (Input) (Note1) | t _{LOW} | 4.7 | - | 1.3 | - | 0.5 | - | |
| SCL clock High width (Input) (Note2) | t _{HIGH} | 4.0 | - | 0.6 | - | 0.26 | - | |
| Re-start condition setup time (Note5) | t _{SU, STA} | 4.7 | - | 0.6 | - | 0.26 | - | |
| Data hold time (Input) (Note3, 4) | t _{HD, DAT} | 0 | - | 0 | - | 0 | - | |
| Data setup time | t _{SU, DAT} | 250 | - | 100 | - | 50 | - | ns |
| Stop condition setup time | t _{SU, STO} | 4.0 | - | 0.6 | - | 0.26 | - | μs |
| Bus free time between stop condition and start condition (Note5) | t _{BUF} | 4.7 | - | 1.3 | - | 0.5 | - | |

Note1: SCL clock low level width (output): $p \times (2^{n+1}+10)/T$ ($[I2CxOP]<NFSEL>=0$)

Note2: SCL clock high level width(output): $p \times (2^{n+1}+6)/T$ ($[I2CxOP]<NFSEL>=0$)

On I²C bus standard, the maximum speed of standard mode/fast mode/fast mode+ is 100kHz/400 kHz/1MHz respectively. Note that an internal SCL clock frequency is determined by the fsys and the calculation of Note1 and Note2 above-mentioned.

Note3: The data hold time (output) is equal to four cycles of the prescaler clock (Tprscck) started from the internal SCL.

Note4: On I²C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/td on the SCL/SDA should be included in the data hold time.

Note5: Depends on the software.

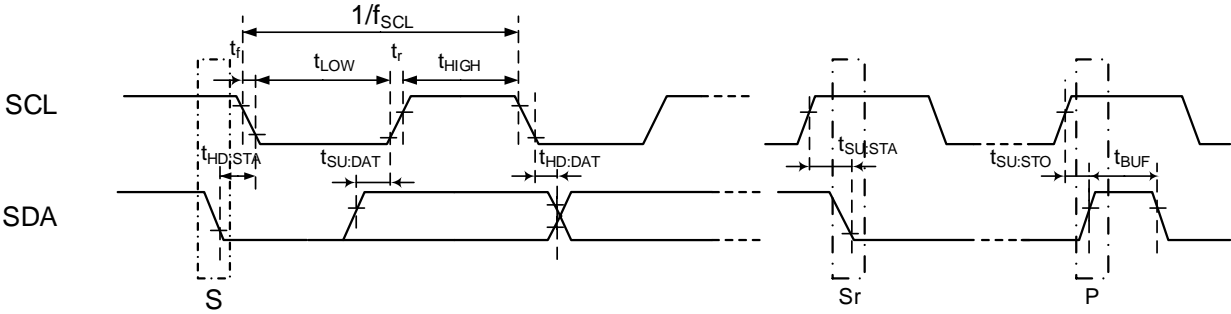


Figure 7.4 AC timing of I²C

7.9.3. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.9.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = $0.75 \times DVDD5$, Low = $0.25 \times DVDD5$
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.3.2. AC Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as $\Phi T0$ clock. This cycle is depending on the Prescaler Clock setting.

- (1) Operation other than the pulse count

| Parameter | Symbol | Calculation | | $\Phi T0=40$ MHz | | Unit |
|------------------------|-------------------|-------------|-----|------------------|-----|------|
| | | Min | Max | Min | Max | |
| Low level pulse width | t _{VCKL} | 2T + 20 | - | 70 | - | ns |
| High level pulse width | t _{VCKH} | 2T + 20 | - | 70 | - | |

- (2) At the pulse count

| Parameter | Symbol | Calculation | | $\Phi T0=40$ MHz In this case, NF=4 | | Unit |
|------------------------|-------------------|-------------|-----|--|-----|------|
| | | Min | Max | Min | Max | |
| Pulse cycle | t _{DCYC} | 1000 | - | 1000 | - | ns |
| Low level pulse width | t _{PWL} | 500 | - | 500 | - | |
| High level pulse width | t _{PWH} | 500 | - | 500 | - | |
| Input setup | t _{ABS} | (NF+1)×T+20 | - | 145 | - | |
| Input hold | t _{ABH} | (NF+1)×T+20 | - | 145 | - | |

NF Value is depend on the $[T32AxPLSCR]<NF[1:0]>$ setting as follows.

| $[T32AxPLSCR]<NF[1:0]>$ | NF Value of Formula |
|-------------------------|---------------------|
| 00 | 0 |
| 01 | 2 |
| 10 | 4 |
| 11 | 8 |

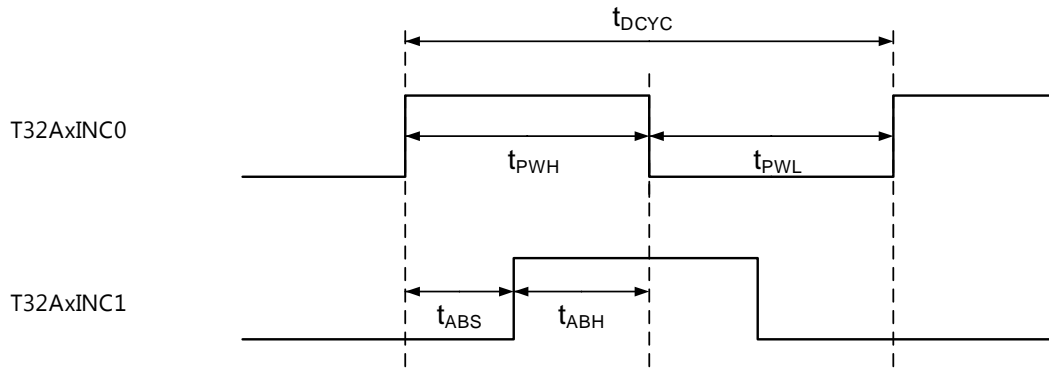


Figure 7.5 Count Pulse input

7.9.4. External Interrupt

7.9.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40°C to 85°C
- Input level: High = $0.75 \times DVDD5$, Low = $0.25 \times DVDD5$
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.4.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL, IDLE mode

| Parameter | Symbol | Calculation | | fsys=40 MHz | | Unit |
|------------------------|--------------|-------------|-----|-------------|-----|------|
| | | Min | Max | Min | Max | |
| Low level pulse width | t_{INTAL1} | T + 100 | - | 125 | - | ns |
| High level pulse width | t_{INTAH1} | T + 100 | - | 125 | - | |

(2) STOP1, STOP2 mode

| Parameter | Symbol | Calculation | | fsys=40 MHz | | Unit |
|------------------------|--------------|-------------|-----|-------------|-----|------|
| | | Min | Max | Min | Max | |
| Low level pulse width | t_{INTCL2} | 125 | - | 125 | - | ns |
| High level pulse width | t_{INTCH2} | 125 | - | 125 | - | |

7.9.5. Trigger Input (TRGINx)

7.9.5.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5 = 2.7V to 5.5V
- Ta = -40°C to 85°C
- Input level: High = $0.75 \times DVDD5$, Low = $0.25 \times DVDD5$
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.5.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

| Parameter | Symbol | Calculation | | fsys=40 MHz | | Unit |
|------------------------|------------------|-------------|-----|-------------|-----|------|
| | | Min | Max | Min | Max | |
| Low level pulse width | t _{ADL} | 2T + 20 | - | 70 | - | ns |
| High level pulse width | t _{ADH} | 2T + 20 | - | 70 | - | |

7.9.6. Debug Communication

7.9.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40°C to 85°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.6.2. SWD Interface

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V

| Parameter | Symbol | Min | Max | Unit |
|--|-----------|-----|-----|------|
| CLK cycle | t_{dck} | 100 | - | ns |
| Output data hold from on the rising edge of CLK | t_{d1} | 4 | - | |
| Output data valid from on the rising edge of CLK | t_{d2} | - | 30 | |
| Rising edge of CLK from input data valid | t_{ds} | 20 | - | |
| Input data hold from on the rising edge of CLK | t_{dh} | 15 | - | |

2.7V ≤ DVDD5=AVDD5 < 4.5V

| Parameter | Symbol | Min | Max | Unit |
|--|-----------|-----|-----|------|
| CLK cycle | t_{dck} | 100 | - | ns |
| Output data hold from on the rising edge of CLK | t_{d1} | 4 | - | |
| Output data valid from on the rising edge of CLK | t_{d2} | - | 42 | |
| Rising edge of CLK from input data valid | t_{ds} | 20 | - | |
| Input data hold from on the rising edge of CLK | t_{dh} | 15 | - | |

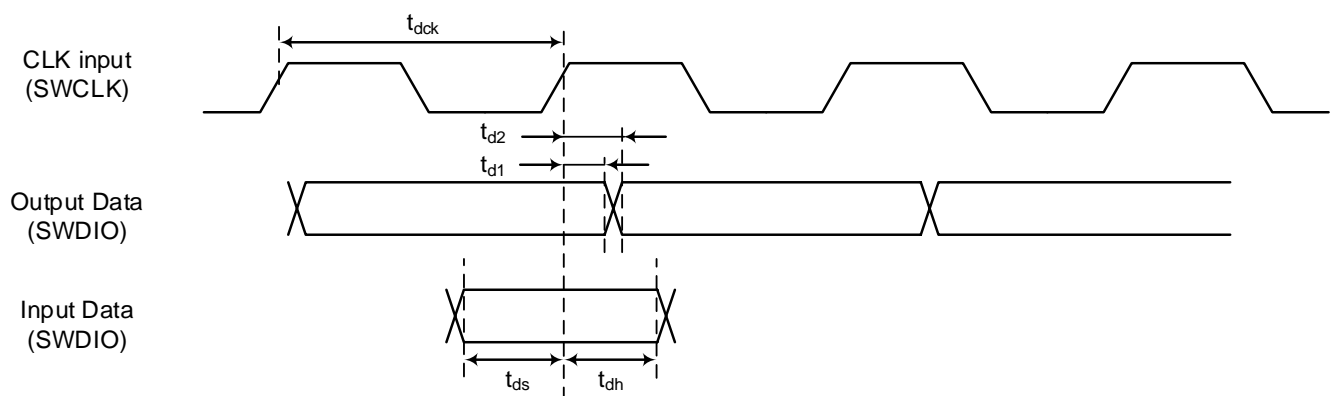


Figure 7.6 SWD waveform

7.9.6.3. JTAG Interface

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V

| Parameter | Symbol | Min | Max | Unit |
|---|-----------|-----|-----|------|
| CLK cycle | t_{dck} | 100 | - | ns |
| Output data hold from on the falling edge of CLK | t_{d3} | 4 | - | |
| Output data valid from on the falling edge of CLK | t_{d4} | - | 33 | |
| Rising edge of CLK from input data valid | t_{ds} | 20 | - | |
| Input data hold from on the rising edge of CLK | t_{dh} | 15 | - | |

2.7V ≤ DVDD5=AVDD5 < 4.5V

| Parameter | Symbol | Min | Max | Unit |
|---|-----------|-----|-----|------|
| CLK cycle | t_{dck} | 100 | - | ns |
| Output data hold from on the falling edge of CLK | t_{d3} | 4 | - | |
| Output data valid from on the falling edge of CLK | t_{d4} | - | 45 | |
| Rising edge of CLK from input data valid | t_{ds} | 20 | - | |
| Input data hold from on the rising edge of CLK | t_{dh} | 15 | - | |

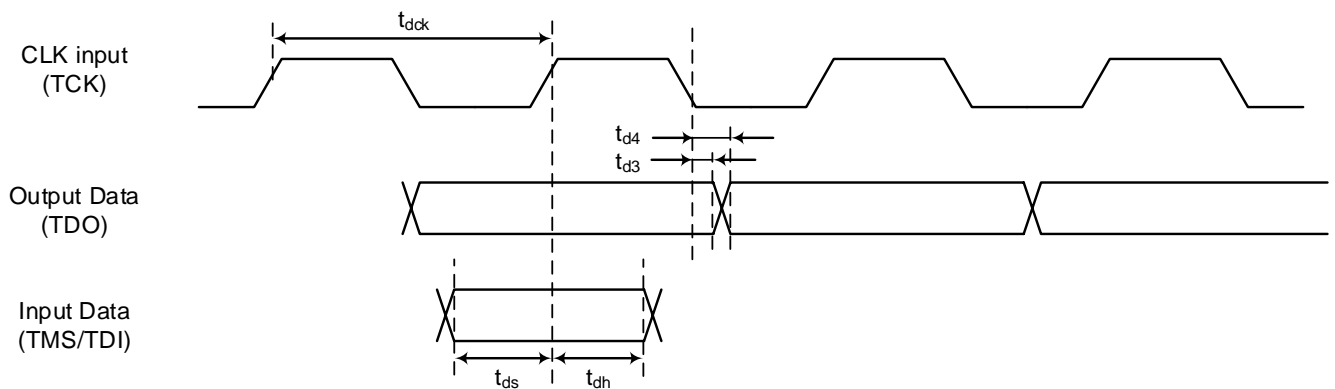


Figure 7.7 JTAG waveform

7.9.6.4. ETM Trace

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V

| Parameter | Symbol | Min | Max | Unit |
|--|--------------|-----|-----|------|
| TRACECLK cycle | t_{clk} | 50 | - | ns |
| Data valid from rising on TRACECLK | t_{setupr} | 2 | - | |
| TRACEDATA hold from on the rising edge of TRACECLK | t_{holdr} | 1 | - | |
| TRACEDATA valid from on the falling edge of TRACECLK | t_{setupf} | 2 | - | |
| TRACEDATA hold from on the falling edge of TRACECLK | t_{holdf} | 1 | - | |

2.7V ≤ DVDD5=AVDD5 < 4.5V

| Parameter | Symbol | Min | Max | Unit |
|--|--------------|-----|-----|------|
| TRACECLK cycle | t_{clk} | 100 | - | ns |
| Data valid from rising on TRACECLK | t_{setupr} | 2 | - | |
| TRACEDATA hold from on the rising edge of TRACECLK | t_{holdr} | 1 | - | |
| TRACEDATA valid from on the falling edge of TRACECLK | t_{setupf} | 2 | - | |
| TRACEDATA hold from on the falling edge of TRACECLK | t_{holdf} | 1 | - | |

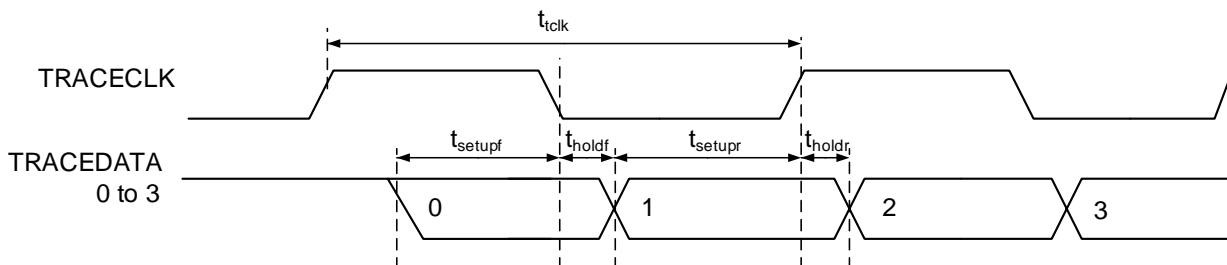


Figure 7.8 Trace signal waveform

7.9.7. SCOUT Pin

7.9.7.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5= AVDD5= 2.7V to 5.5V
- Ta = -40°C to 85°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.7.2. AC Electrical Characteristics

"T" in the table indicates the cycle of the SCOUT output waveform.

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V

| Parameter | Symbol | Calculation | | SCOUT = 20MHz | | Unit |
|------------------------|------------------|-------------|-----|---------------|-----|------|
| | | Min | Max | Min | Max | |
| Low level pulse width | t _{SCL} | 0.5T- 10 | - | 15 | - | ns |
| High level pulse width | t _{SCH} | 0.5T- 10 | - | 15 | - | |

2.7V ≤ DVDD5=AVDD5 < 4.5V

| Parameter | Symbol | Calculation | | SCOUT = 20MHz | | Unit |
|------------------------|------------------|-------------|-----|---------------|-----|------|
| | | Min | Max | Min | Max | |
| Low level pulse width | t _{SCL} | 0.5T- 12 | - | 13 | - | ns |
| High level pulse width | t _{SCH} | 0.5T- 12 | - | 13 | - | |

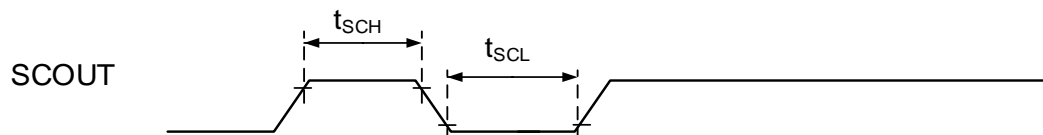


Figure 7.9 SCOUT wave output

7.9.8. Noise Filter Characteristics

| Parameter | Condition | Min | Typ. | Max | Unit |
|--------------------|---|-----|------|-----|------|
| Noise cancel width | DVDD5 = 2.7 to 5.5V Ta = -40 to 85°C | 15 | 30 | 60 | ns |

7.9.9. External Clock Input

7.9.9.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40°C to 85°C
- Input level: High = $0.75 \times DVDD5$, Low = $0.25 \times DVDD5$
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.9.2. AC Electrical Characteristics

| Parameter | Symbol | Min | Typ. | Max | Unit |
|----------------------------------|---------------|-----|------|-----|------|
| Clock frequency($1/t_{ehcin}$) | $f_{EHCLKIN}$ | 6 | - | 20 | MHz |
| Clock duty | - | 45 | - | 55 | % |
| Clock rise time | t_r | - | - | 10 | ns |
| Clock fall time | t_f | - | - | 10 | ns |

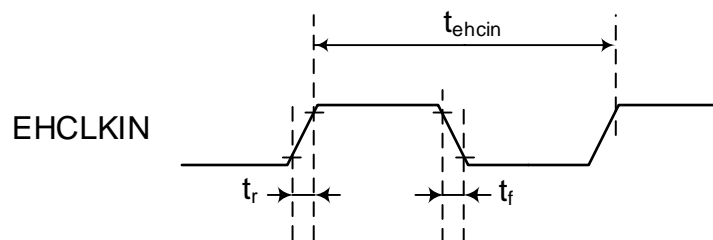


Figure 7.10 External clock input waveform

7.10. Flash Memory Characteristics

7.10.1. Code Flash

DVDD5=2.7V to 5.5V
Ta=-40 to 85°C

| Parameter | Condition | Min | Typ. | Max | Unit |
|------------------|------------------------|-----|------|--------|--------|
| Endurance | | - | - | 10,000 | cycles |
| Programming time | Word Program time | - | 29.5 | - | μs |
| Erase time | Page Erase time | 1.1 | - | 4.3 | ms |
| | Block Erase time | 8.6 | - | 34 | |
| | Area Erase time(Note2) | - | 9.2 | - | |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: No block with effective protection.

7.10.2. Data Flash

DVDD5=2.7V to 5.5V
Ta=-40 to 85°C

| Parameter | Condition | Min | Typ. | Max | Unit |
|------------------|------------------------|------|------|---------|--------|
| Endurance | | - | - | 100,000 | cycles |
| Programming time | | - | 64.7 | - | μs |
| Erase time | Page Erase time | 1 | - | 3.9 | ms |
| | Block Erase time | 15.4 | - | 62.1 | |
| | Area Erase time(Note2) | - | 9.2 | - | |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: No block with effective protection.

7.10.3. Chip Erase

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

| Parameter | Condition | Min | Typ. | Max | Unit |
|-----------------|--|------|------|------|------|
| Chip Erase time | Erasing of Code Flash, Data Flash, Protect Bits(Code), Protect Bits(Data), User Information Area and Security bits | 23.4 | - | 62.7 | ms |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: When Chip Erase command executes, no block with effective protection.

7.11. Regulator

| Parameter | Condition | Min | Typ. | Max | Unit |
|----------------------------------|--------------------------------------|-----|------|-----|------|
| Capacitance of REGOUT1 capacitor | DVDD5=2.7V to 5.5V Ta=-40 to 85°C | - | 4.7 | - | μF |
| Capacitance of REGOUT2 capacitor | | - | 4.7 | - | |

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.12. Oscillation Circuit

7.12.1. Internal Oscillator

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|-----------------------|---------------------|---------------------------------|-----|------|-----|------|
| Oscillation frequency | f _{IHOSC1} | Factory out, IC data (Note2) | - | 10 | - | MHz |
| | f _{IHOSC2} | | - | 10 | - | |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Not included the influence depend on the variations after Factory shipping. Please execute oscillator adjustment by the trimming register, if trimming of IHOSC1 is required. However, IHOSC2 cannot execute trimming.

7.12.2. External Oscillator

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|-----------------------|--------------------|-----------|-----|------|-----|------|
| Oscillation frequency | f _{EHOSC} | | 6 | - | 12 | MHz |
| | f _{ELOSC} | | 30 | - | 34 | kHz |

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

7.12.3. Oscillation Circuit

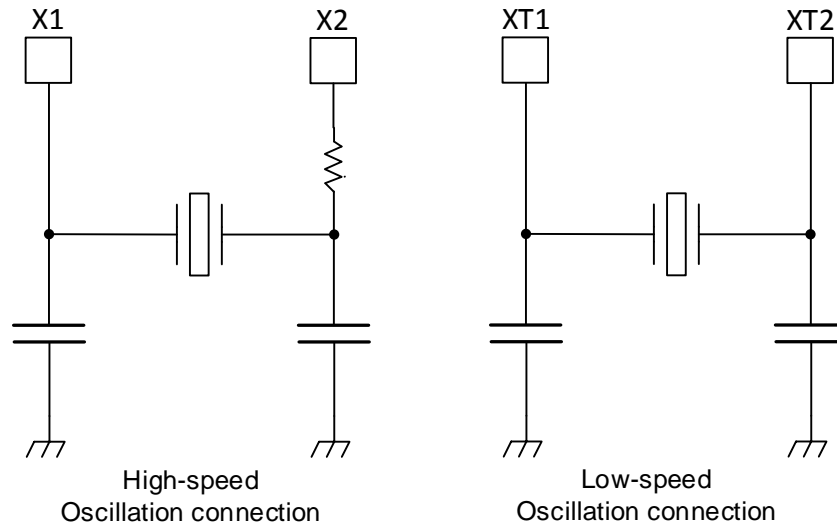


Figure 7.11 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer to this information when selecting external parts.

7.12.4. Ceramic Oscillator

This product has been evaluated by the ceramic oscillator by Murata Manufacturing Co., Ltd.

Please refer to the Murata Website for details.

7.12.5. Crystal Oscillator

This product has been evaluated by the crystal oscillator by KYOCERA Corporation.

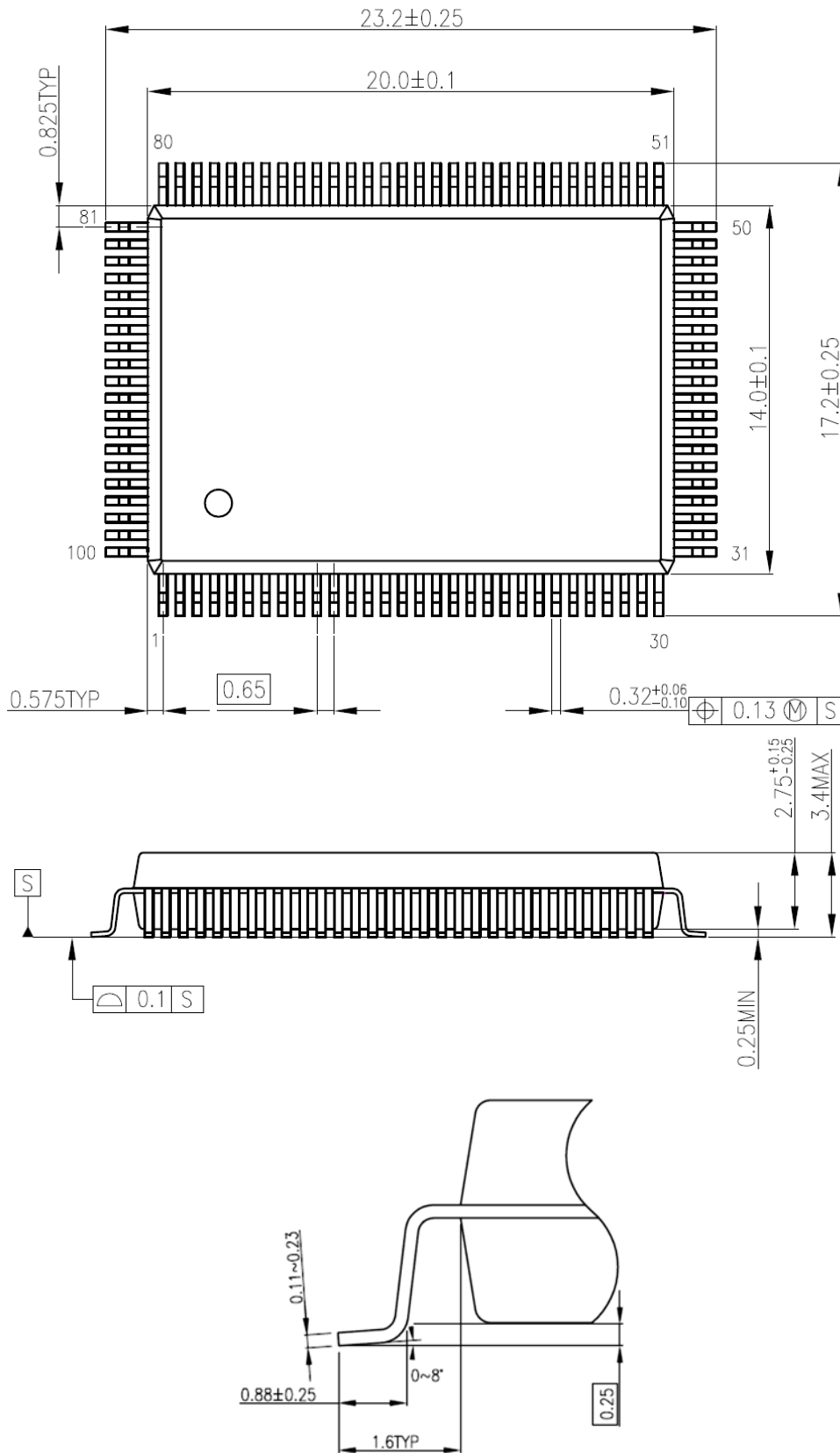
Please refer to the KYOCERA Website for details.

7.12.6. Precautions for designing printed circuit board

Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

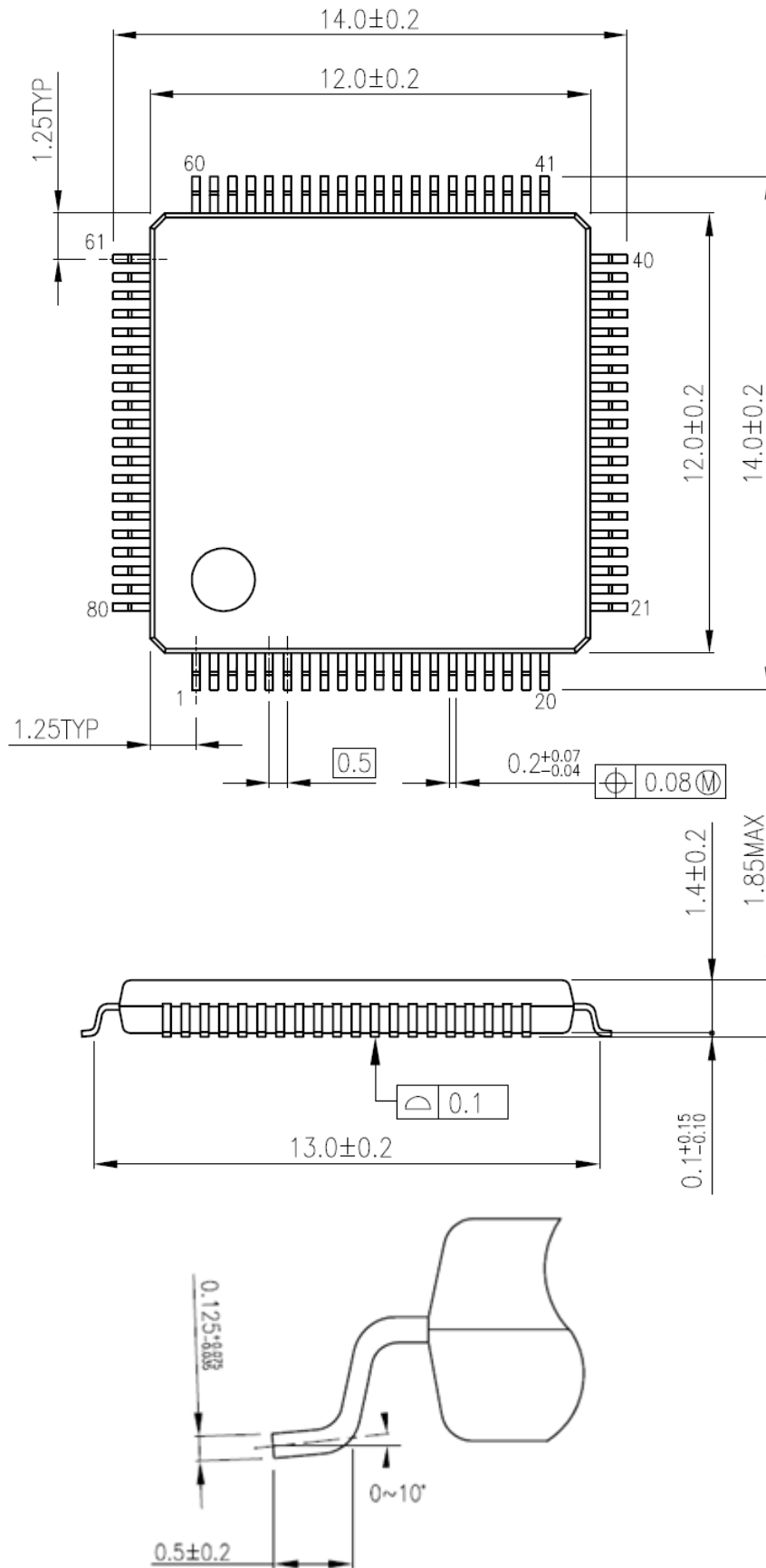
8.2. P-QFP100-1420-0.65-001

Unit: mm



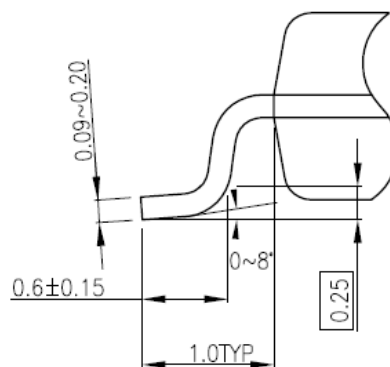
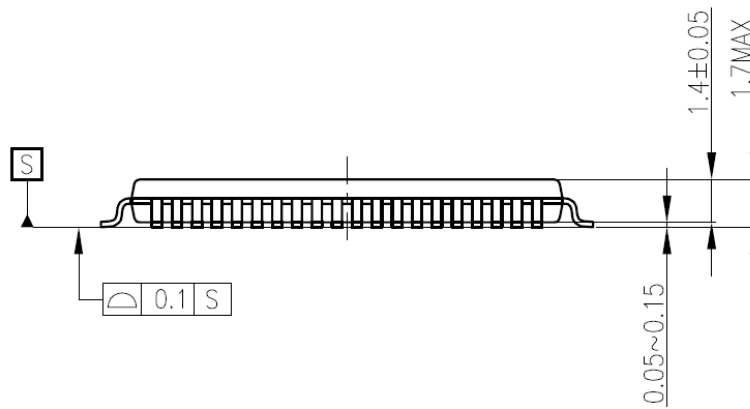
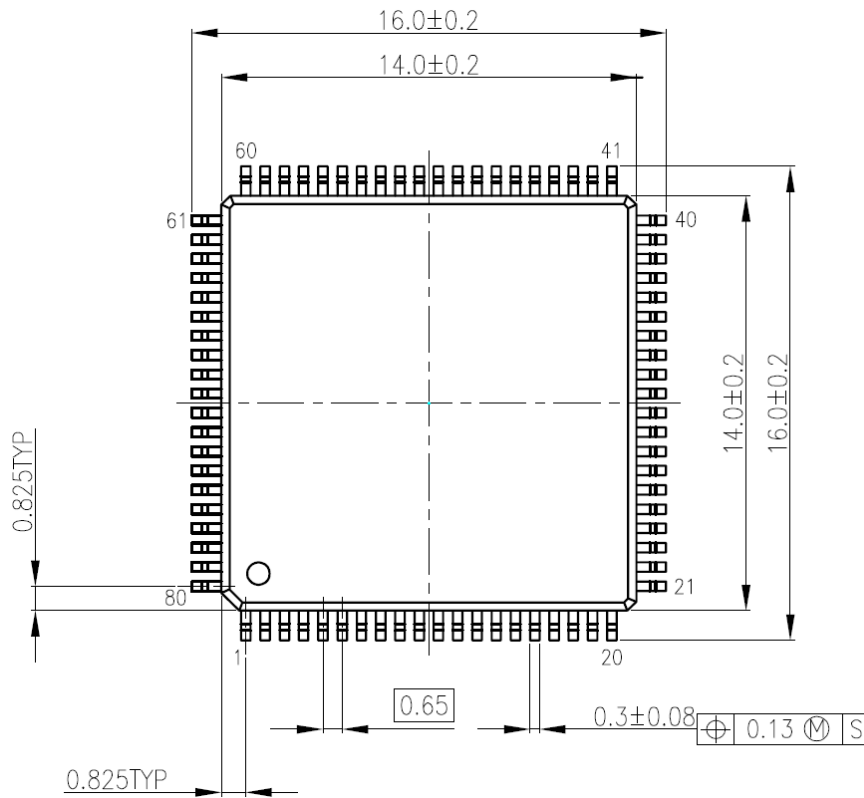
8.3. LQFP80-P-1212-0.50F

Unit: mm



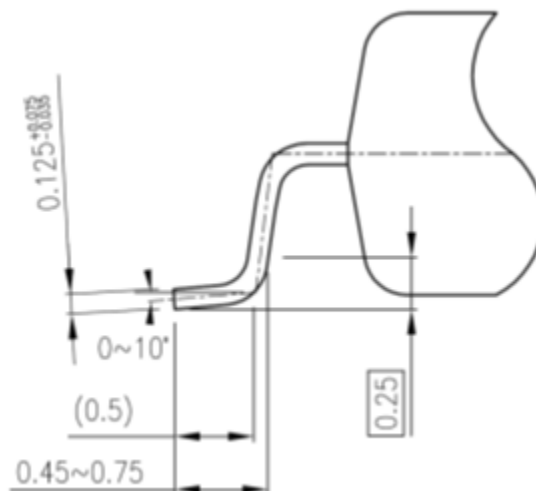
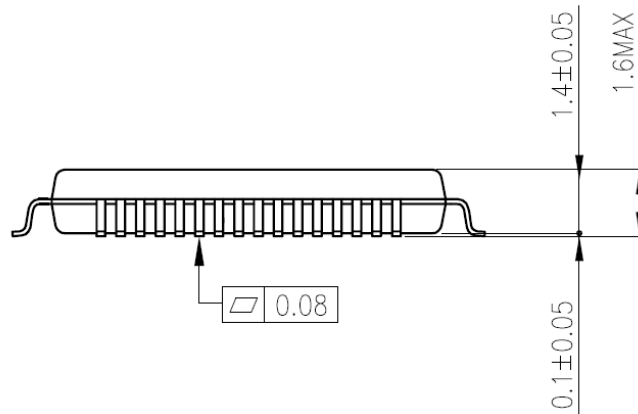
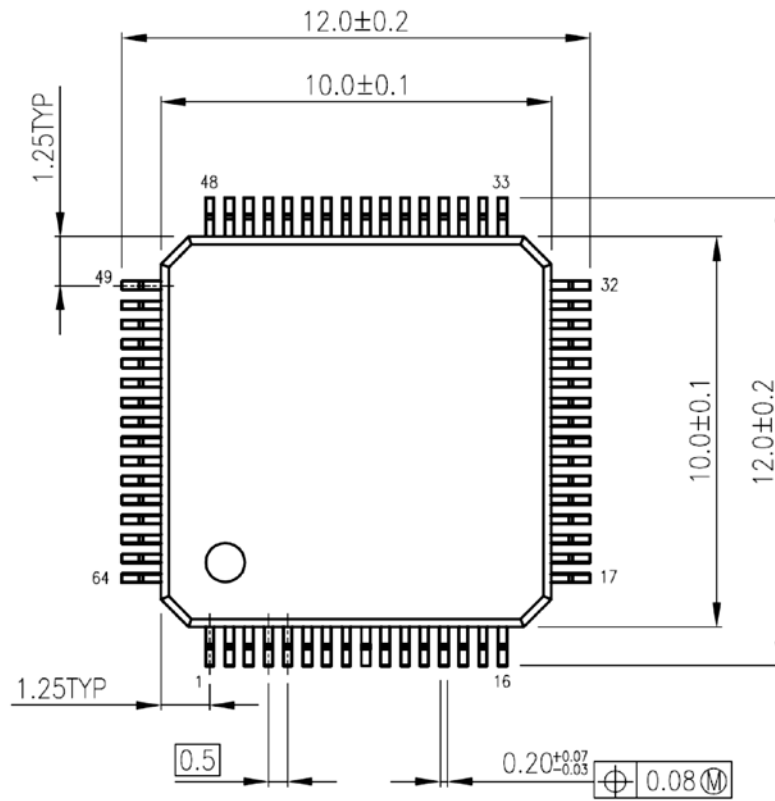
8.4. P-LQFP80-1414-0.65-001

Unit: mm



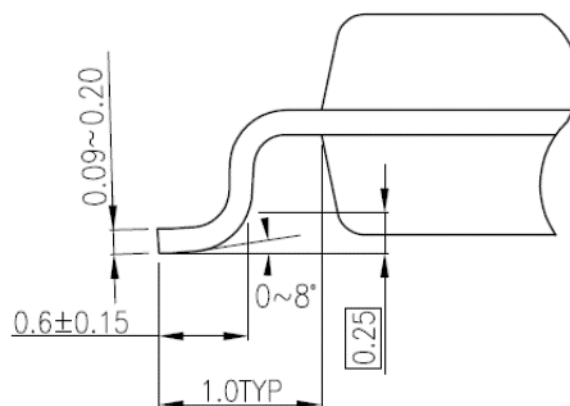
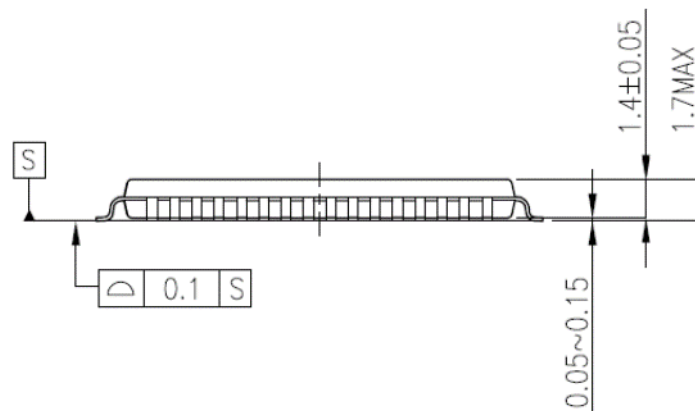
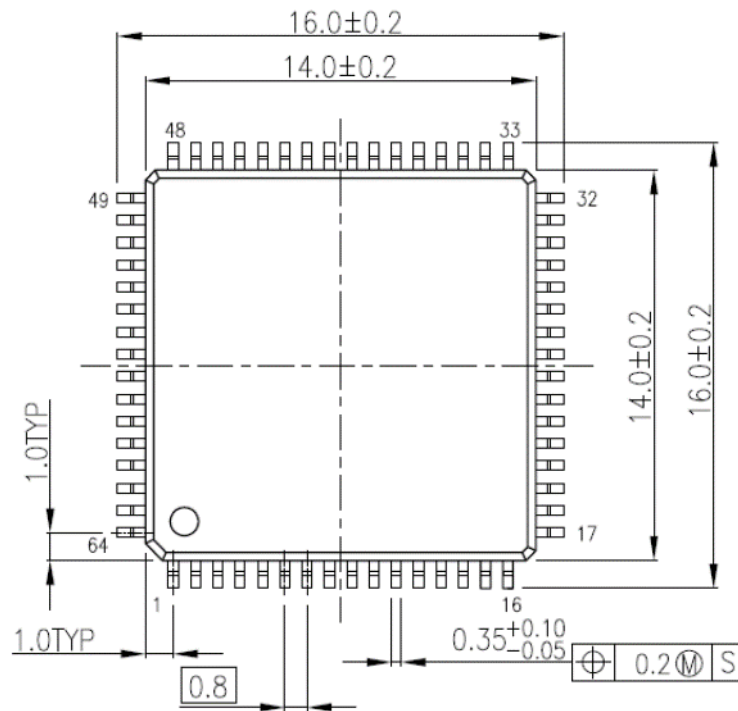
8.5. LQFP64-P-1010-0.50E

Unit: mm



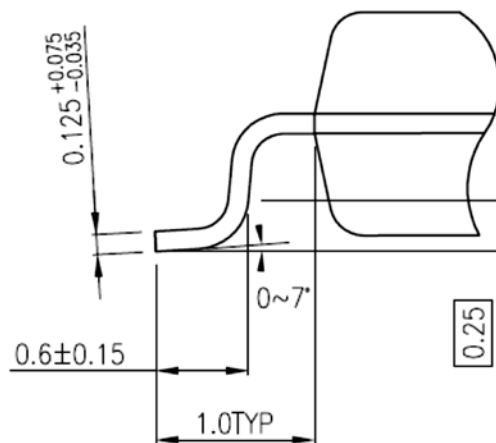
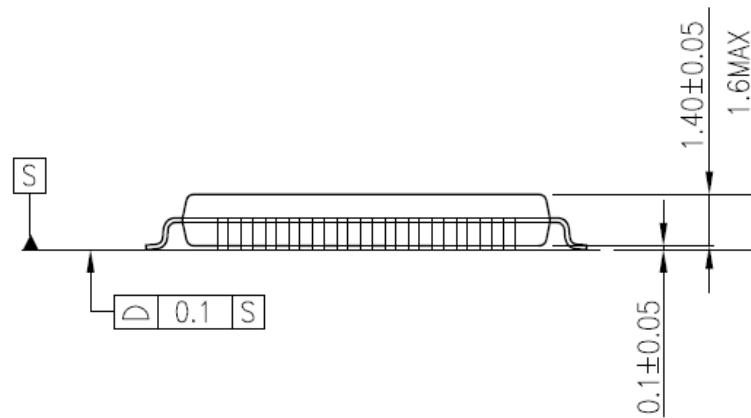
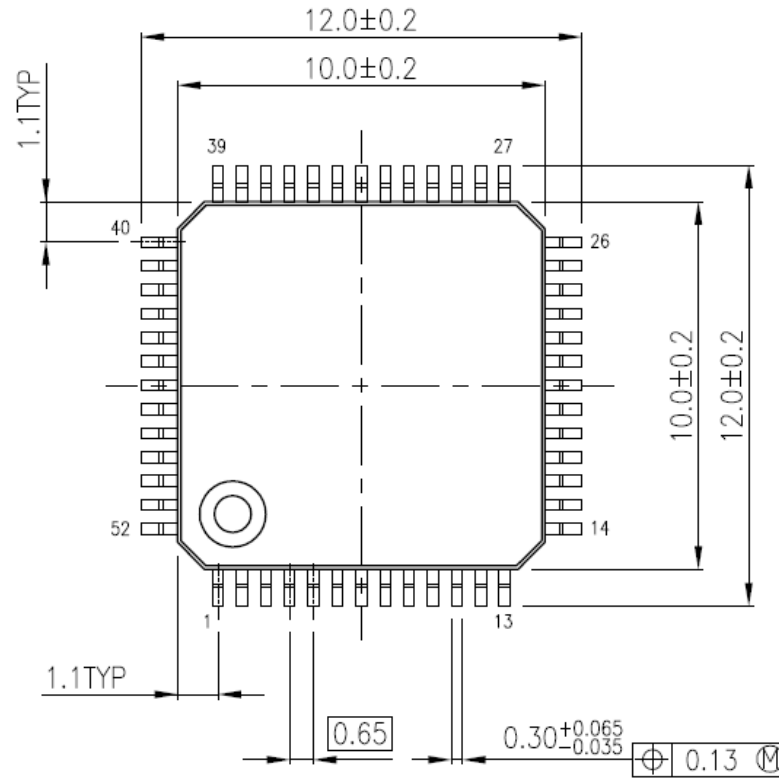
8.6. P-LQFP64-1414-0.80-002

Unit: mm



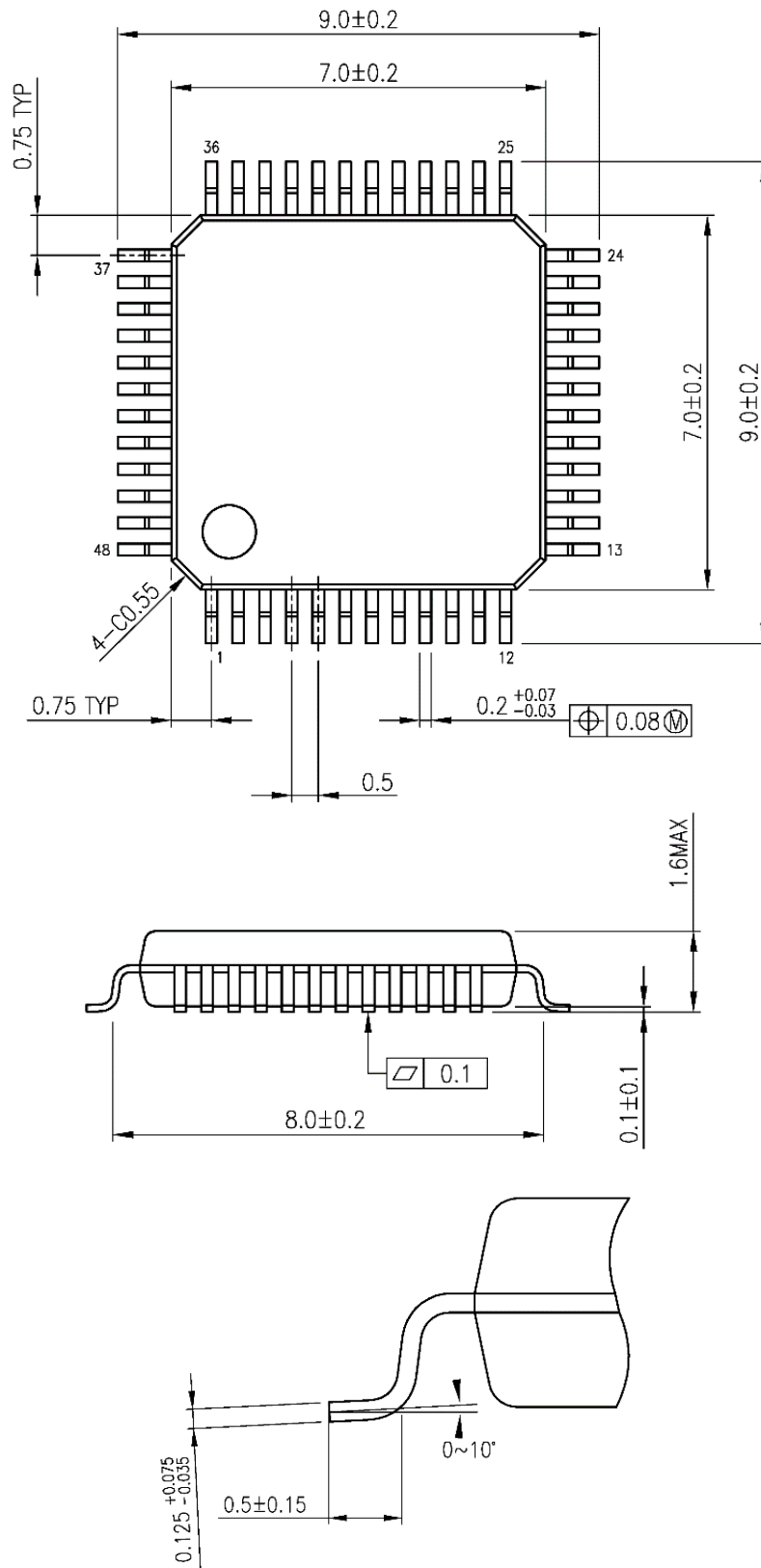
8.7. P-LQFP52-1010-0.65-001

Unit: mm



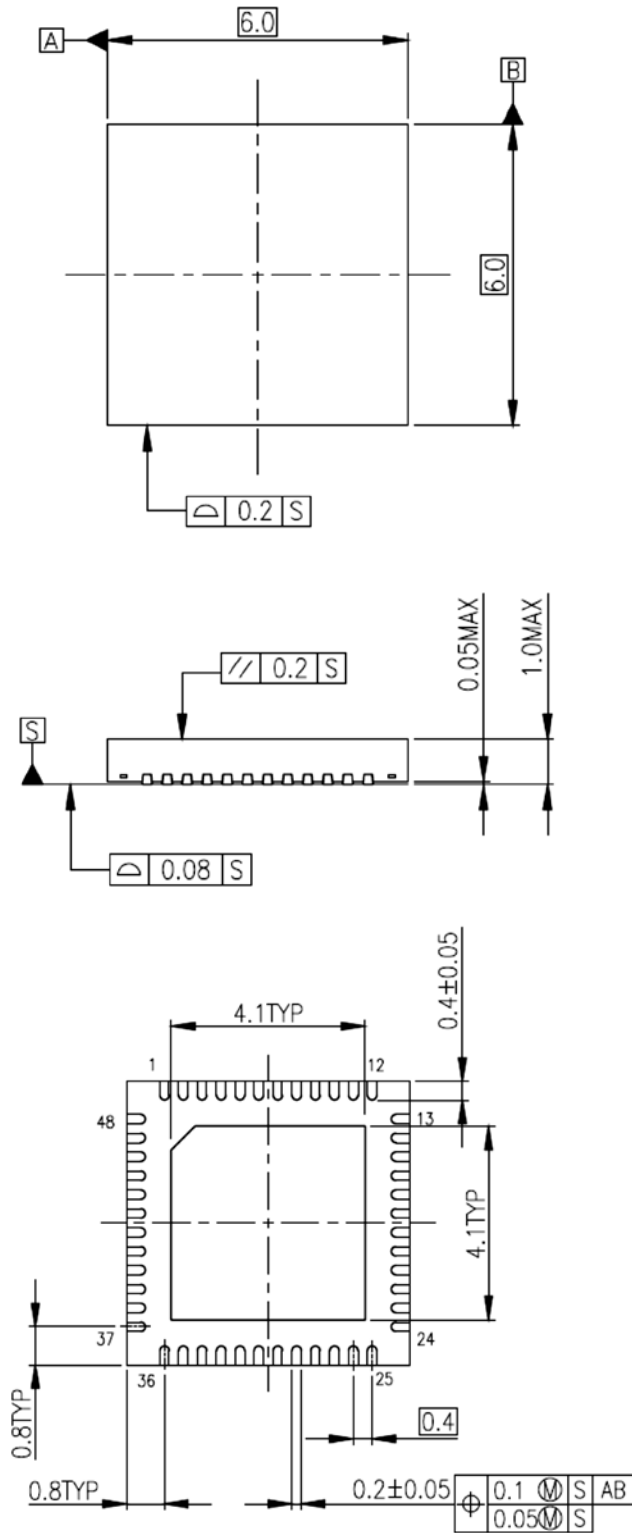
8.8. LQFP48-P-0707-0.50C

Unit: mm



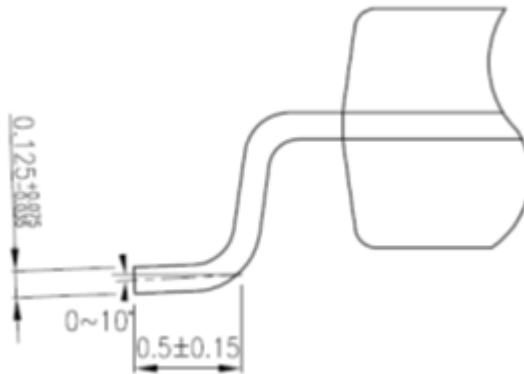
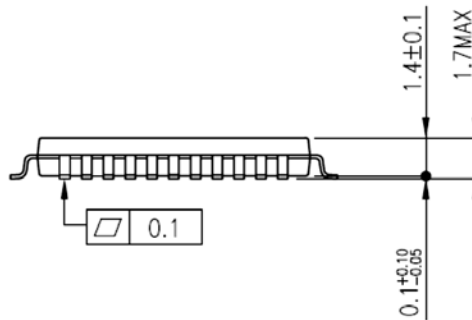
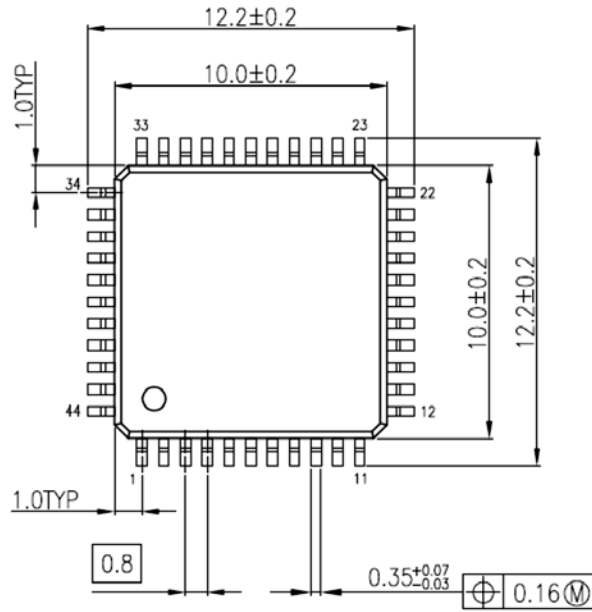
8.9. P-VQFN48-0606-0.40-003

Unit: mm



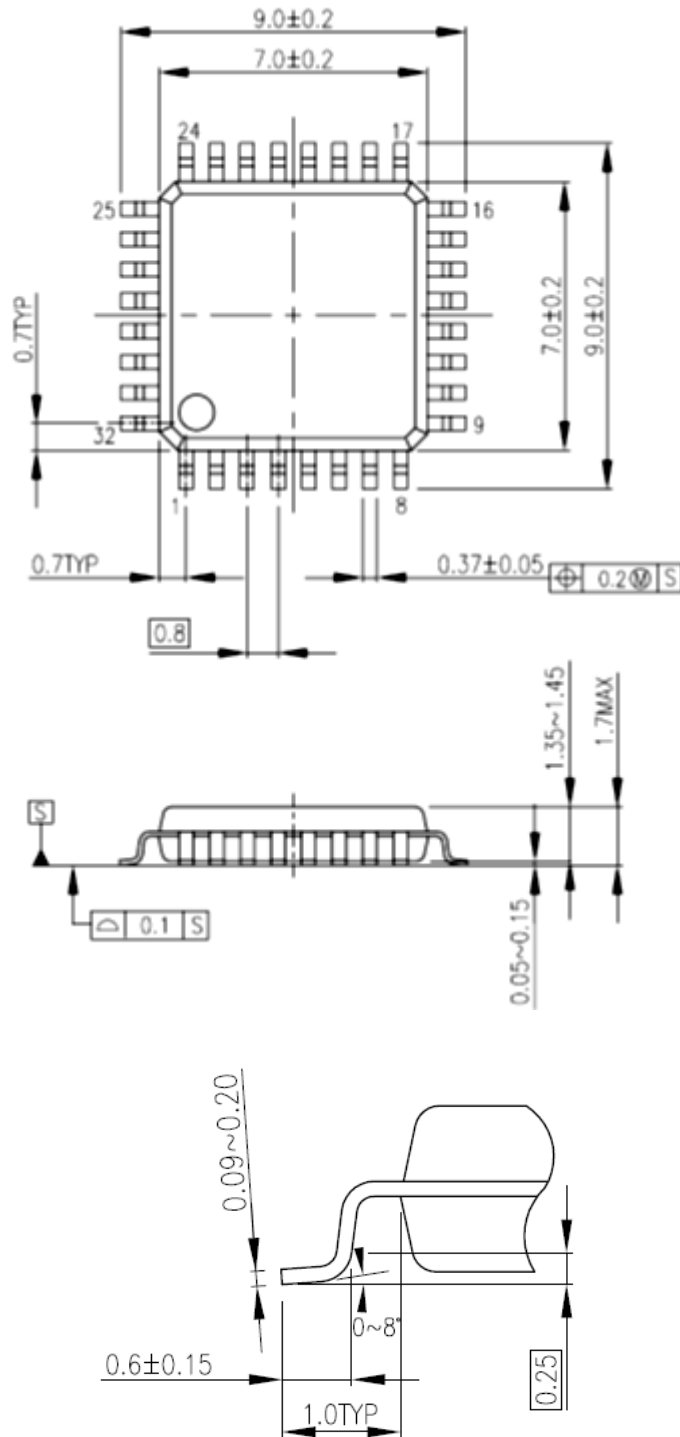
8.10. LQFP44-P-1010-0.80A

Unit: mm



8.11. P-LQFP32-0707-0.80-002

Unit: mm



9. Precautions

This Page explains general precautions on the use of Toshiba MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of document has higher priority.

(1) The MCUs' operation at power-on

At power-on, internal state of the MCUs is unstable. Therefore, the state of the pins is undefined until the reset operation is completed.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.

Also, when a reset is performed by the internal power-on reset, pins of the MCUs that use the internal power-on reset are undefined until power supply voltage reaches the voltage at which power-on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch-up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

10. Revision History

Table 10.1 Revision History

| Revision | Date | Description |
|----------|------------|--|
| Rev.1.0 | 2017-5-10 | New Release |
| Rev.2.0 | 2017-08-01 | <p>Revised Company Name and related contents</p> <p>Revised ARM Logo/Trademark, character</p> <p>Revised Features: UART(number of FIFO stage)</p> <p>TSPI(number of FIFO stage)</p> <p>5.5 OFD (fIHOSC1 → fEHOSC)</p> <p>5.12 UART number of FIFO stage</p> <p>7.9.1 TSPI "K2" → "k2"</p> <p>7.9.2.3 T32A "unit change "uS" → "ns"</p> |
| Rev.3.0 | 2018-04-12 | <p>Features: Asynchronous Serial Interface(UART)</p> <p>Corrected to "2.4Mbps (Max)" -> "2.5Mbps (Max)".</p> <p>Terms and Abbreviations: Corrected</p> <p>1. Block Diagram: Corrected the DMAC in Figure 1.1</p> <p>3.1. List of Memory Sizes: Added Code Flash Size to Table 3.1</p> <p>4.2. Functional Pin and Ports Assignment (Pin Number):</p> <p>Corrected to "terminal" -> "pin".</p> <p>Added PB7, PC6 and PR3 of Table 4.19</p> <p>4.3. Ports: Corrected to "State under" -> "Under"</p> <p>Corrected to "State after " -> "After"</p> <p>4.3.1. Port Specification Table: Corrected PB0 of Table 4.20.</p> <p>Corrected PH1, PH3 of Table 4.21.</p> <p>5.1. Reference Manuals: "(Version x)" in Table 5.1 has been deleted.</p> <p>Corrected to "CG-M3H(1)-B" -> "CG-M3H(1)-D" in Table 5.1.</p> <p>5.5. Oscillation Circuit: (EHOSC), (ELOSC) added.</p> <p>5.6. Trimming Circuit (TRM):</p> <p>Corrected to "oscillator (IHOSC1) " -> "oscillator 1 (IHOSC1) "</p> <p>5.7. Oscillation Frequency Detection Circuit (OFD): Corrected to "the external reference clock (fEHOSC) " -> "the internal reference clock (fIHOSC2) "</p> <p>5.9. Digital Noise Filter (DNF): Deleted ("The noise ---- 0.35 to 22.4 μs. ")</p> <p>5.11. DMA Controller (DMAC): Corrected to "DMAC has the 32 channels ----" -> "TMPM3H Group (1) product has one DMA". Deleted "DMA requests of ---- circuit (TRGSEL). "</p> <p>5.14. I²C Interface (I²C): Corrected to "I²C bus Interface" -> "I²C Interface ".</p> <p>5.17. Motor Control Circuit Plus (PMD+):</p> <p>Corrected to "Motor Control Circuit" -> "5.17. Motor Control Circuit Plus"</p> <p>5.21. Clock Selective Watchdog Timer (SIWDT): Corrected to "The WDT is" -> "The SIWDT is".</p> <p>Corrected to "internal oscillator (fIHOSC1), or internal oscillator for the OFD (fIHOSC2) " -> "internal oscillator 1 (fIHOSC1), or internal oscillator 2 for the OFD (fIHOSC2) "</p> <p>6.1. Port: PA6, PA7 ..., PA4, PA5 ..., PH 0 to PH 3 have been corrected</p> <p>6.3. Control Pin: Added "MODE pin must be connected to GND" to MODE BSC.</p> <p>Delete "MODE" "RESET" in the circuit diagram.</p> <p>6.4. Clock control: X1, X2 have been corrected</p> <p>7.1. Absolute Maximum Ratings: Table 7.1</p> <p>AVDD 5 in the Symbol column: "-0.3 to 6.0"->"-0.3 to DVDD5 (Note1) "</p> <p>VIN1 VIN2 in the Symbol column: " (Note1) " Added</p> <p>(Note1) description added</p> <p>7.2. DC Electrical Characteristics (1/2)</p> <p>Corrected parameter "Input leak current". (4.5V ≤DVDD5=AVDD5≤ 5.5 V)</p> <p>Corrected parameter "Output leak current". (4.5V ≤DVDD5=AVDD5≤ 5.5 V)</p> <p>Corrected parameter "Schmitt trigger Input width". (4.5V ≤DVDD5=AVDD5≤ 5.5 V)</p> <p>Corrected parameter " Low level output voltage ". (2.7V ≤DVDD5=AVDD5< 4.5V)</p> <p>Corrected parameter "Schmitt trigger Input width". (2.7V ≤DVDD5=AVDD5< 4.5V)</p> <p>7.3. DC Electrical Characteristics (2/2)</p> <p>Deleted "LOSC = Low Speed Oscillator" in Table 7.2.</p> <p>Corrected Item "Power consumption " -> "Current consumption".</p> <p>7.4. 12-bit AD Converter Characteristics: Corrected of table (Condition, Value, Note)</p> <p>7.5. 8-bit DA Converter Characteristics: Corrected of table (Condition)</p> <p>7.6. Characteristics of Internal processing at RESET:</p> <p>Minimum value of Power-on rising gradient "-" -> "0.01"</p> <p>7.8. Characteristics of Voltage Detection Circuit:</p> <p>The maximum value of "Detection response time" was corrected. ("250"->"200 ")</p> |

| | | |
|---------|------------|--|
| | | <p>7.9.1.2. AC Electrical Characteristics: Figures 7.1 to 7.4 have been corrected. ("<CKPOL>=0"->"<CKPOL>=1", "<CKPOL>=1"->"<CKPOL>=0")</p> <p>7.9.2. I²C Interface (I²C): Corrected to " I²C Bus " -> " I²C Interface " Deleted "- Pull-up resistor: 200 Ω"</p> <p>7.9.3. 32-bit Timer Event Counter (T32A) Corrected to "32-bit Timer/Event Counter" -> "32-bit Timer Event Counter"</p> <p>7.9.3.2. AC Characteristics: Corrected "tPWH" -> "tPWL", "tPWL" -> "tPWH" The signal name in Figure 7.6 has been corrected. "PHCxIN0" -> "T32AxINA0 T32AxINB0 T32AxINC0" "PHCxIN1" -> "T32AxINA1 T32AxINB1 T32AxINC1"</p> <p>7.9.4.1. AC Measurement Conditions: "▪ Ta = -40 °C to 85 °C " added.</p> <p>7.9.4.2. AC Electrical Characteristics: Corrected to "(5) STOP1···" -> "(2) STOP1···"</p> <p>7.9.5.1. AC Measurement Conditions: "▪ Ta = -40 °C to 85 °C " added.</p> <p>7.9.6.1. AC Measurement Conditions: "▪ Ta = -40 °C to 85 °C " added.</p> <p>7.9.7.1. AC Measurement Conditions: "▪ Ta = -40 °C to 85 °C " added.</p> <p>7.9.9.1. AC Measurement Conditions: "▪ Ta = -40 °C to 85 °C " added.</p> <p>7.10.3. Chip Erase: Minimum value of Chip Erase time " 22.7" -> " 23.4" Maximum value of Chip Erase time " 35.2" -> " 62.7"</p> <p>7.12.4. Ceramic Oscillator: Deleted of URL</p> <p>7.12.5. Crystal Oscillator: Corrected of explanation. Deleted of URL. Part Naming Conventions: Update</p> <p>10. Revision History: Added table number "10.1"</p> |
| Rev.4.0 | 2018-08-20 | <p>Features: Added "Commercial Production Date: 2017-06"</p> <p>Conventions Modified explanation of trademark</p> <p>3. Memory Map: Corrected "Flash for code" -> "Code Flash" in Figure 3.1.</p> <p>4.1.1. Peripheral Function Pins: Deleted "(TRGSEL)" in Table 4.1.</p> <p>5.14. I²C Interface (I²C): Corrected Note2 in Table 5.13. (Note2: The address match wake up function is available.)</p> <p>7.3. DC Electrical Characteristics (2/2): Corrected operating condition in IDLE. Corrected "Transmission(2.4Mbps)" -> "Transmission(2.5Mbps)" of "UART" term in Table 7.3.</p> <p>7.4. 12-bit AD Converter Characteristics: Changed the position of (Note3) in "conversion time" term.</p> <p>7.9.1.2. AC Electrical Characteristics: Corrected "TSPIxTXD hold time" -> "TSPIxTXD delay time" of "tODLY1" term in Table. Deleted "(2) 1st clock edge sampling (Slave)" and Table 7.2.</p> <p>7.9.3.2. AC Characteristics: Deleted signal name in Figure 7.5 (T32AxINA0, T32AxINB0, T32AxINA1, T32AxINB1)</p> <p>RESTRICTIONS ON PRODUCT USE Modified contents</p> |
| Rev 4.1 | 2019-07-10 | <p>Revised the information of Commercial Production.</p> <p>4.1.1 Table 4.1 modified the function description of UART CTS&RTS. modified the peripheral function column of I2C</p> <p>4.1.3 Table 4.3 modified the function description of BOOT</p> <p>4.1.5 Capacitors between power supply pins added new section</p> <p>6.3 modified the contents of RESET</p> <p>7.6 modified the Warm Reset Min Value of tCPUWT (from 70 to 55)</p> <p>7.9.1.2 modified the condition contents for operation clock.</p> <p>7.9.3.2 modified the condition contents for operation clock.</p> <p>7.9.6.2 modified the Parameter contents. Added the Fig 7.6 of SWD waveform</p> <p>7.9.6.3 modified the Parameter contents. Revised the Fig 7.7 of JTAG waveform</p> <p>7.12.1 revised the Note2 about trimming of IHOSC1/2.</p> <p>Appendix List of All Pins Modified contents, new notification added Part Naming Conventions Revised contents</p> |

Appendix

List of All pins

Combination Function A to B: These are the functions which become effective without setting up port function registers.
Combination Function 1 to 6: These are the functions which become effective with setting up port function registers.
The noise filters in the table do not include noise cancelers, digital noise filters (DNF), etc.

List of All pins(1)

| M3H0 (LQFP100) | M3H0 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP84) | M3H3 (LQFP82) | M3H2 (LQFP48 VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) | Port Name | Combination FunctionA | Combination FunctionB | Combination Function1 | Combination Function2 | Combination Function3 | Combination Function4 | Combination Function5 | Combination Function6 | PU/PD | OD | 5V_T | SMT/OMOS | Noise Filter | Status under RESET | Status after RESET |
|----------------|---------------|---------------|---------------|---------------|----------------------|---------------|---------------|-----------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------|-----|------|----------|--------------|--------------------|--------------------|
| 1 | 3 | - | - | - | - | - | - | PD3 | AINA03 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 2 | 4 | 1 | 1 | 1 | 1 | 1 | - | PD2 | AINA02 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 3 | 5 | 2 | 2 | 2 | 2 | 2 | 1 | PD1 | AINA01 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 4 | 6 | 3 | 3 | 3 | 3 | 3 | 2 | PDO | AINA00 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 5 | 7 | 4 | 4 | 4 | 4 | 4 | 3 | AVDD5 | | | | | | | | | - | - | - | - | - | - | - |
| 6 | 8 | 5 | 5 | 5 | 5 | 5 | 4 | AVSS | | | | | | | | | - | - | - | - | - | - | - |
| 7 | 9 | 6 | 6 | 6 | 6 | 6 | - | PG0 | DAC0 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 8 | 10 | 7 | - | - | - | - | - | PG1 | DAC1 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 9 | 11 | 8 | - | - | - | - | - | DVSSG | | | | | | | | | - | - | - | - | - | - | - |
| 10 | 12 | 9 | - | - | - | - | - | DVDD5C | | | | | | | | | - | - | - | - | - | - | - |
| 11 | 13 | 10 | - | - | - | - | - | PA7 | | INT11 | | | | | | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 12 | 14 | 11 | 7 | 7 | - | - | - | PA6 | | INT07 | | | | | | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 13 | 15 | 12 | 8 | 8 | 7 | 6 | - | PA5 | | I2C1SDA | | | | T32A00INB1 | | | PU/PD | YES | YES | SMT | N/A | Hi-z | Hi-z |
| 14 | 16 | 13 | 9 | 9 | 8 | 7 | - | PA4 | | I2C1SCL | | | TSPI0CS1 | T32A00INB0 | | | PU/PD | YES | YES | SMT | N/A | Hi-z | Hi-z |
| 15 | 17 | 14 | 10 | 10 | 9 | 8 | - | PA3 | | | TSPI0CSN | TSPI0CS0 | T32A00OUTB | | TRGNH | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 16 | 18 | 15 | 11 | 11 | 10 | 9 | 5 | PA2 | | UT0RXD | UT0TXDA | TSPI0RXD | T32A00INA1 | T32A00INC1 | ENC0B | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 17 | 19 | 16 | 12 | 12 | 11 | 10 | 6 | PA1 | | UT0TXDA | UT0RXD | TSPI0TXD | T32A00INA0 | T32A00INC0 | ENC0B | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 18 | 20 | 17 | 13 | 13 | 12 | 11 | 7 | PA0 | | UT0TXDB | | TSPI0SCK | T32A00OUTA | T32A00OUTC | ENC0A | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 19 | 21 | - | - | - | - | - | - | PM6 | | INT15 | | | | | | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 20 | 22 | - | - | - | - | - | - | PM5 | | | | | | T32A00INB1 | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 21 | 23 | - | - | - | - | - | - | PM4 | | UT0RTS_N | UT0CTS_N | TSPI0CS1 | T32A00INB0 | | TRACEATA3 | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 22 | 24 | - | - | - | - | - | - | PM3 | | UT0CTS_N | UT0RTS_N | TSPI0CS0 | T32A00OUTB | TSPI0CSN | TRACEATA2 | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 23 | 25 | 18 | 14 | - | - | - | - | PM2 | | INT09 | UT0RXD | UT0TXDA | TSPI0RXD | T32A00INA1 | T32A00INC1 | TRACEATA1 | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 24 | 26 | 19 | 15 | - | - | - | - | PM1 | | UT0TXDA | UT0RXD | TSPI0TXD | T32A00INA0 | T32A00INC0 | TRACEATA0 | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 25 | 27 | 20 | 16 | - | - | - | - | PM0 | | UT0TXDB | | TSPI0SCK | T32A00OUTA | T32A00OUTC | TRACECLK | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 26 | 28 | 21 | 17 | 14 | 13 | 12 | 8 | PB0 | BOOT_N | | | | | T32A01OUTA | T32A01OUTC | SCOUT | PU/PD | YES | N/A | SMT | N/A | Hi-z>Note1 | Hi-z |
| 27 | 29 | 22 | 18 | 15 | 14 | 13 | 9 | PB1 | | INT03 | RXIN0 | | | T32A01INA0 | T32A01INC0 | TRGN0 | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 28 | 30 | 23 | 19 | 16 | 15 | 14 | - | PB2 | | UT2TXDA | UT2RXD | TSPI1SCK | T32A01INA1 | T32A01INC1 | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 29 | 31 | 24 | 20 | 17 | 16 | 15 | - | PB3 | | UT2RXD | UT2TXDA | TSPI1TXD | T32A01OUTB | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 30 | 32 | 25 | 21 | 18 | 17 | 16 | - | PB4 | | UT2CTS_N(注3) | UT2RTS_N(注3) | TSPI1RXD | T32A01INB0 | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 31 | 33 | - | - | - | - | - | - | PB5 | | UT2RTS_N | UT2CTS_N | TSPI1CS0 | T32A01INB1 | TSPI1CSN | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 32 | 34 | - | - | - | - | - | - | PB6 | | | | | TSPI1CS1 | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 33 | 35 | - | - | - | - | - | - | PB7 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 34 | 36 | 26 | 22 | 19 | - | - | - | PL0 | | UT2TXDA | UT2RXD | I2C2SCL | | | | PU/PD | YES | YES | SMT | N/A | Hi-z | Hi-z | |
| 35 | 37 | 27 | 23 | 20 | - | - | - | PL1 | | UT2RXD | UT2TXDA | I2C2SDA | | | | PU/PD | YES | YES | SMT | N/A | Hi-z | Hi-z | |
| 36 | 38 | 28 | 24 | - | - | - | - | PL2 | | UT2CTS_N | UT2RTS_N | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z | |
| 37 | 39 | 29 | 25 | - | - | - | - | PL3 | | INT08 | UT2RTS_N | UT2CTS_N | | | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z | |
| 38 | 40 | 30 | - | - | - | - | - | PL4 | | INT12 | | | | | | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 39 | 41 | - | - | - | - | - | - | PL5 | | TSPI1CS1 | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 40 | 42 | - | - | - | - | - | - | PL6 | | TSPI1CS0 | TSPI1CSN | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 41 | 43 | 31 | - | - | - | - | - | PP0 | | TSPI1SCK | | T32A01OUTA | T32A01OUTC | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 42 | 44 | 32 | - | - | - | - | - | PP1 | | TSPI1TXD | | T32A01INA0 | T32A01INC0 | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 43 | 45 | 33 | - | - | - | - | - | PP2 | | TSPI1RXD | | T32A01INA1 | T32A01INC1 | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 44 | 46 | 34 | 26 | 21 | 18 | 17 | 10 | DVDD5A | | | | | | | | | - | - | - | - | - | - | - |
| 45 | 47 | 35 | 27 | 22 | 19 | 18 | 11 | REGOUT2 | | | | | | | | | - | - | - | - | - | - | - |
| 46 | 48 | 36 | 28 | 23 | 20 | 19 | 12 | REGOUT1 | | | | | | | | | - | - | - | - | - | - | - |
| 47 | 49 | 37 | 29 | 24 | 21 | 20 | 13 | DVSSA | | | | | | | | | - | - | - | - | - | - | - |
| 48 | 50 | 38 | 30 | 25 | 22 | 21 | 14 | PH0 | X1 | EHOLKIN | | | | | | | PD | N/A | N/A | SMT | N/A | Hi-z | Hi-z |
| 49 | 51 | 39 | 31 | 26 | 23 | 22 | 15 | PH1 | X2 | | | | | | | | PD | N/A | N/A | SMT | N/A | Hi-z | Hi-z |
| 50 | 52 | 40 | 32 | 27 | 24 | 23 | 16 | RESET_N | | | | | | | | | PU | - | - | SMT | - | - | - |
| 51 | 53 | 41 | 33 | 28 | 25 | - | - | PH2 | XT1 | | | | | | | | PD | N/A | N/A | SMT | N/A | Hi-z | Hi-z |
| 52 | 54 | 42 | 34 | 29 | 26 | - | - | PH3 | XT2 | INT06 | | | | | | | PD | N/A | N/A | SMT | YES | Hi-z | Hi-z |
| 53 | 55 | 43 | 35 | 30 | 27 | 24 | 17 | MODE | | | | | | | | | PD | N/A | N/A | SMT | N/A | - | - |
| 54 | 56 | 44 | 36 | 31 | 28 | 25 | 18 | PC0 | | INT00 | I2C0SCL | | T32A02OUTA | T32A02OUTC | | | PU/PD | YES | YES | SMT | YES | Hi-z | Hi-z |
| 55 | 57 | 45 | 37 | 32 | 29 | 26 | 19 | PC1 | | INT01 | I2C0SDA | | T32A02INA0 | T32A02INC0 | | | PU/PD | YES | YES | SMT | YES | Hi-z | Hi-z |
| 56 | 58 | 46 | 38 | 33 | 30 | 27 | 20 | PC2 | | INT02 | | | T32A02INA1 | T32A02INC1 | RTCOU(注2) | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 57 | 59 | 47 | 39 | 34 | 31 | - | - | PC3 | | | | | T32A02OUTB | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 58 | 60 | 48 | - | - | - | - | - | PC4 | | | | | T32A02INB0 | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 59 | 61 | 49 | - | - | - | - | - | PC5 | | | | | T32A02INB1 | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 60 | 62 | 50 | - | - | - | - | - | PC6 | | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |

Note1: When the RESET_N pin is "Low", a built-in pull-up resistor becomes effective.

Note2: The RTCOUT is invalid in the M3H1 and M3H0.

Note3: The UT2CTS_N/UT2RTS_N of PB4 is invalid in the M3H5, M3H4, M3H3, M3H2, M3H1 and M3H0.

List of All pins(2)

| M3H0 (LQFP100) | M3H0 (QFP100) | M3H5 (LQFP80) | M3H4 (LQFP84) | M3H3 (LQFP52) | M3H2 (LQFP48 VQFN48) | M3H1 (LQFP44) | M3H0 (LQFP32) | Port Name | Combination FunctionA | Combination FunctionB | Combination Function1 | Combination Function2 | Combination Function3 | Combination Function4 | Combination Function5 | Combination Function6 | PU/PD | OD | 5V_T | SMT/ OMOS | Noise Filter | Status under RESET | Status after RESET |
|-------------------|------------------|------------------|------------------|------------------|----------------------------|------------------|------------------|--------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|-------|-----|------|--------------|-----------------|--------------------------|--------------------------|
| 61 | 63 | - | - | - | - | - | - | PR0 | | | | | T32A020UTA | T32A020UTC | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 62 | 64 | - | - | - | - | - | - | PR1 | | | | | T32A020NA0 | T32A020NC0 | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 63 | 65 | - | - | - | - | - | - | PR2 | | | | | T32A020NA1 | T32A020NC1 | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 64 | 66 | - | - | - | - | - | - | PR3 | | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 65 | 67 | - | - | - | - | - | - | PN5 | | | | | T32A050NB1 | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 66 | 68 | 51 | - | - | - | - | - | PN4 | | | | | T32A050NB0 | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 67 | 69 | 52 | 40 | - | - | - | - | PN3 | | INT10 | | | T32A050UTB | | TRGN2 | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 68 | 70 | 53 | 41 | - | - | - | - | PN2 | | | | | T32A050NA1 | T32A050NC1 | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 69 | 71 | 54 | 42 | - | - | - | - | PN1 | | | | | T32A050NA0 | T32A050NC0 | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 70 | 72 | 55 | 43 | - | - | - | - | PN0 | | | | | T32A050UTA | T32A050UTC | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 71 | 73 | 56 | 44 | 35 | 32 | 28 | 21 | PJ0 | | | UT1TXDB | | T32A030UTA | T32A030UTC | U00 | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 72 | 74 | 57 | 45 | 36 | 33 | 29 | 22 | PJ1 | | | UT1TXDA | UT1RXD | T32A030NA0 | T32A030NC0 | X00 | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 73 | 75 | 58 | 46 | 37 | 34 | 30 | 23 | PJ2 | | | UT1RXD | UT1TXDA | T32A030NA1 | T32A030NC1 | V00 | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 74 | 76 | 59 | 47 | 38 | 35 | 31 | 24 | PJ3 | | | UT1CTS_N | UT1RTS_N | T32A030UTB | | Y00 | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 75 | 77 | 60 | 48 | 39 | 36 | 32 | 25 | PJ4 | | INT04 | UT1RTS_N | UT1CTS_N | T32A030NB0 | | W00 | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 76 | 78 | 61 | 49 | 40 | 37 | 33 | 26 | PJ5 | | | | | T32A030NB1 | | Z00 | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 77 | 79 | 62 | 50 | 41 | 38 | 34 | 27 | PK0 | | | UT1TXDB | | | | EMQ0_N | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 78 | 80 | 63 | 51 | 42 | 39 | 35 | 28 | PK1 | | INT05 | UT1TXDA | UT1RXD | | | OVV0_N | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 79 | 81 | 64 | 52 | 43 | 40 | 36 | 29 | PK2 | | | UT1RXD | UT1TXDA | T32A040UTA | T32A040UTC | TMS/SWDIO | | PU/PD | YES | N/A | SMT | N/A | PU | PU |
| 80 | 82 | 65 | 53 | 44 | 41 | 37 | 30 | PK3 | | | UT1CTS_N(注1) | UT1RTS_N(注1) | T32A040NA0 | T32A040NC0 | TCK/SWCLK | | PU/PD | YES | N/A | SMT | N/A | PD | PD |
| 81 | 83 | 66 | 54 | 45 | 42 | 38 | - | PK4 | | | UT1RTS_N | UT1CTS_N | T32A040NA1 | T32A040NC1 | TDO/SWV | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 82 | 84 | 67 | 55 | 46 | 43 | 39 | - | PK5 | | | | | T32A040UTB | | TDI | | PU/PD | YES | N/A | SMT | N/A | PU | PU |
| 83 | 85 | 68 | 56 | - | - | - | - | PK6 | | | | | T32A040NB0 | | TRST_N | | PU/PD | YES | N/A | SMT | N/A | PU | PU |
| 84 | 86 | 69 | - | - | - | - | - | PK7 | | INT13 | | | T32A040NB1 | | | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 85 | 87 | 70 | - | - | - | - | - | PP3 | | INT14 | | | | | | | PU/PD | YES | N/A | SMT | YES | Hi-z | Hi-z |
| 86 | 88 | 71 | 57 | 47 | - | - | - | BSC | | | | | | | | | PD | N/A | N/A | SMT | N/A | - | - |
| 87 | 89 | 72 | 58 | - | - | - | - | DVDD5B | | | | | | | | | - | - | - | - | - | - | - |
| 88 | 90 | 73 | 59 | - | - | - | - | DVSSB | | | | | | | | | - | - | - | - | - | - | - |
| 89 | 91 | - | - | - | - | - | - | PF4 | ANA15 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 90 | 92 | - | - | - | - | - | - | PF3 | ANA14 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 91 | 93 | - | - | - | - | - | - | PF2 | ANA13 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 92 | 94 | - | - | - | - | - | - | PF1 | ANA12 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 93 | 95 | - | - | - | - | - | - | PF0 | ANA11 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 94 | 96 | 74 | - | - | - | - | - | PE6 | ANA10 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 95 | 97 | 75 | - | - | - | - | - | PE5 | ANA09 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 96 | 98 | 76 | 60 | 48 | 44 | 40 | - | PE4 | ANA08 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 97 | 99 | 77 | 61 | 49 | 45 | 41 | - | PE3 | ANA07 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 98 | 100 | 78 | 62 | 50 | 46 | 42 | - | PE2 | ANA06 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 99 | 1 | 79 | 63 | 51 | 47 | 43 | 31 | PE1 | ANA05 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |
| 100 | 2 | 80 | 64 | 52 | 48 | 44 | 32 | PE0 | ANA04 | | | | | | | | PU/PD | YES | N/A | SMT | N/A | Hi-z | Hi-z |

Note1: The UT1CTS_N/UT1RTS_N of PK3 is invalid in the M3H0.

Part Naming Conventions

TMP M3H 4 F W x UG

The identification of
Toshiba microcontrollers

Core

| Symbol | Core |
|--------|----------------------------------|
| M4 | Arm Cortex-M4 processor with FPU |
| M3 | Arm Cortex-M3 |
| M0 | Arm Cortex-M0 |

Product Group

| Family | Group | Application |
|--------|-------|---|
| TXZ | H | For General-purpose/Consumer electronic equipment |
| | K | For Motor/Inverter control industrial equipment(MCU+AMP/COMP) |
| | G | For OA/Digital equipment/industrial equipment |
| | E | For Precision instruments control |
| | P | For Healthcare/ Battery equipment |
| | J | For FA / Robotics |

Revision

Package

| Symbol | Package |
|----------------|--|
| QG | Plastic shrink quad outline non-leaded package; dry-packed |
| UG,DUG, FG,DFG | Plastic quad flat package; dry-packed |
| MG,DMG | Plastic small-outline package; dry-packed |
| XBG | Plastic ball grid array; dry-packed |

ROM Size

| Symbol | Size[KB] |
|--------|----------|
| M | 32 |
| P | 48 |
| S | 64 |
| U | 96 |
| W | 128 |
| Y | 256 |
| Z | 384 |
| D | 512 |
| E | 768 |
| 10 | 1,023 |
| 15 | 1,536 |
| 20 | 2,048 |
| 40 | 4,096 |
| 80 | 8,192 |

Pin Count

| Symbol | Pin Count | Symbol | Pin Count |
|--------|--------------------|--------|--------------------|
| 0 | G Under 32pin | 8 | Q 129pin to 144pin |
| 1 | H 33pin to 44pin | 9 | R 145pin to 176pin |
| 2 | J 45pin to 48pin | A | S 177pin to 200pin |
| 3 | K 49pin to 52pin | B | T 201pin to 224pin |
| 4 | L 53pin to 64pin | C | U 225pin to 250pin |
| 5 | M 65pin to 80pin | D | V 251pin to 300pin |
| 6 | N 81pin to 100pin | | |
| 7 | P 101pin to 128pin | | |

ROM Type

| Symbol | Type |
|--------|-------|
| F | Flash |
| C | Mask |

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