TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOS Ⅵ)

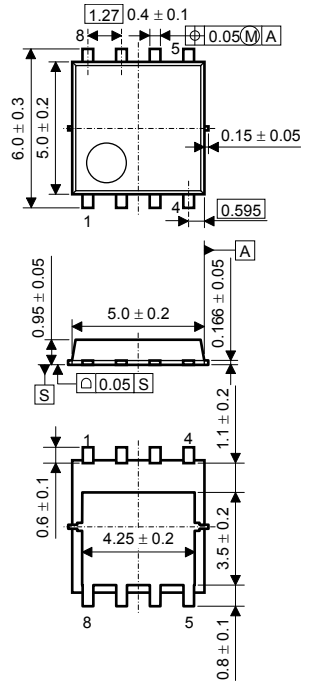
TPCA8128

Lithium Ion Battery Applications

Power Management Switch Applications

- Small footprint due to compact and slim package
- Low drain-source ON resistance : $R_{DS\ (ON)}$ = 3.7 mΩ (typ.)
- Low leakage current : I_{DSS} = −10 μA (max) (V_{DS} = −30 V)
- Enhancement mode
  : V_{th} = −0.8 to −2.0 V (V_{DS} = −10 V, I_D = −0.5 m A)

Unit: mm



1, 2, 3: Source 4: Gate
5, 6, 7, 8: Drain

JEDEC	―
JEITA	―
TOSHIBA	2-5Q1A

Weight: 0.076 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

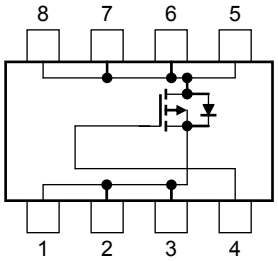
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−30	V
Gate-source voltage		V_{GSS}	−25/+20	V
Drain current	DC (Note 1)	I_D	−34	A
	Pulse (Note 1)	I_{DP}	−102	
Drain power dissipation (Tc = 25°C)		P_D	45	W
Drain power dissipation (t = 10 s) (Note 2a)		P_D	2.8	
Drain power dissipation (t = 10 s) (Note 2b)		P_D	1.6	
Single pulse avalanche energy (Note 3)		E_{AS}	150	mJ
Avalanche current		I_{AR}	−34	A
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: For (Note 1), (Note 2), (Note 3), refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with caution.

Circuit Configuration

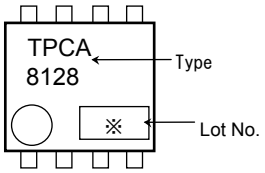


Start of commercial production
2009-12

Thermal Characteristics

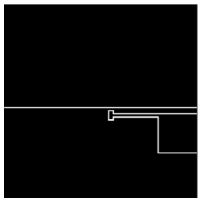
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case (Tc = 25 °C)	$R_{th\ (ch\text{-}c)}$	2.78	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th\ (ch\text{-}a)}$	44.6	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th\ (ch\text{-}a)}$	78.1	

Marking (Note 4)



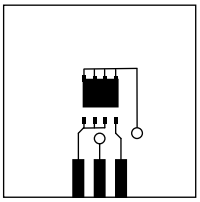
Note 1: The channel temperature should not exceed 150°C during use.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(a)

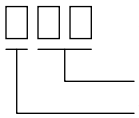


FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(b)

Note 3: V_{DD} = −24 V, T_{ch} = 25°C (initial), L = 100 μH, R_G = 25 Ω, I_{AR} = −34 A

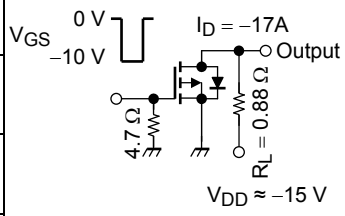
Note 4: ※ Weekly code: (Three digits)



Week of manufacture
(01 for first week of a year, continues up to 52 or 53)

Year of manufacture
(The last digit of the calendar year)

Electrical Characteristics (Ta = 25°C)

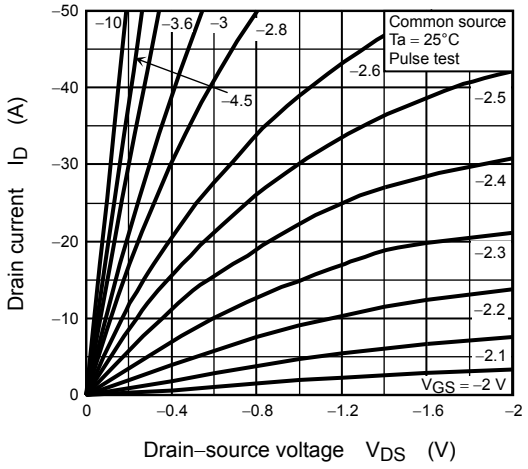
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cut-off current		I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−30	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 10 V (Note 5)	−21	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −0.5mA	−0.8	—	−2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −4.5 V, I_D = −17 A	—	5.1	6.7	mΩ
			V_{GS} = −10 V, I_D = −17 A	—	3.7	4.8	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	4800	—	pF
Reverse transfer capacitance		C_{rss}		—	800	—	
Output capacitance		C_{oss}		—	900	—	
Switching time	Rise time	t_r		—	11	—	ns
	Turn-on time	t_{on}		—	21	—	
	Fall time	t_f		—	135	—	
	Turn-off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	390	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ −24 V, V_{GS} = −10 V	—	115	—	nC
Gate-source charge 1		Q_{gs1}	I_D = −34 A	—	11	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	30	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

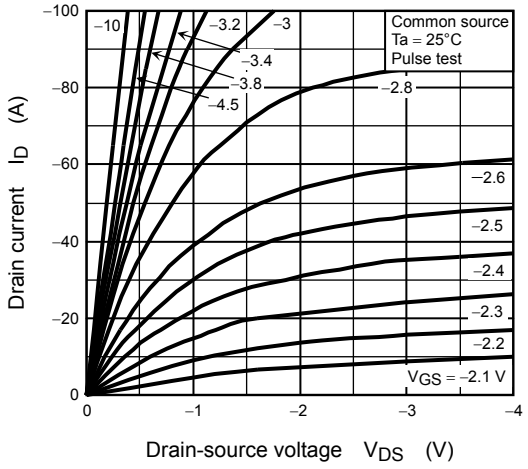
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−102	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −34 A, V_{GS} = 0 V	—	—	1.2	V

Note 5: V_{DSX} mode (the application of a plus voltage between gate and source) may cause decrease in maximum rating of drain-source voltage.

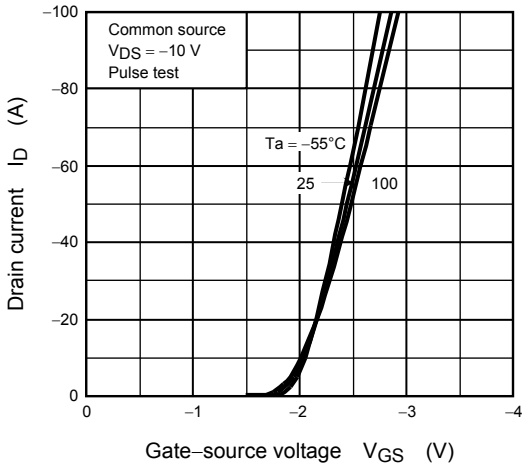
$I_D - V_{DS}$



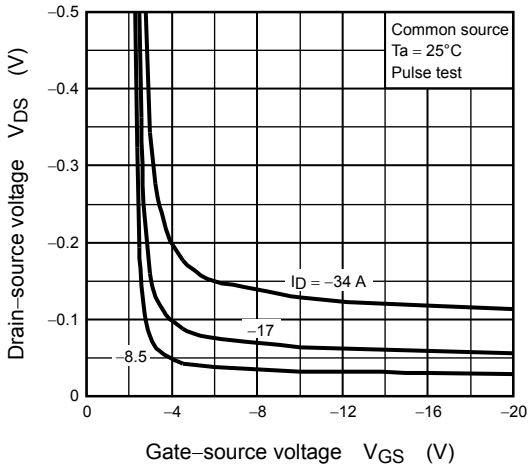
$I_D - V_{DS}$



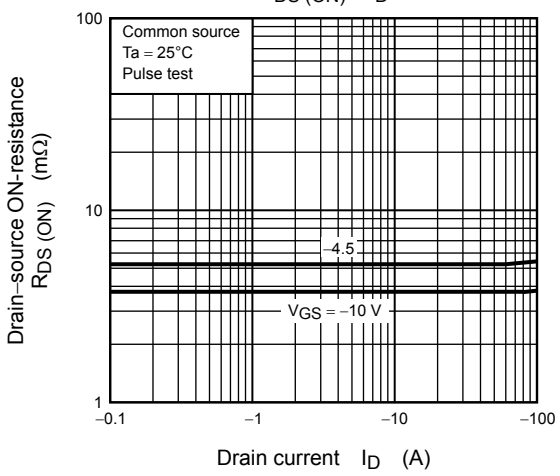
$I_D - V_{GS}$



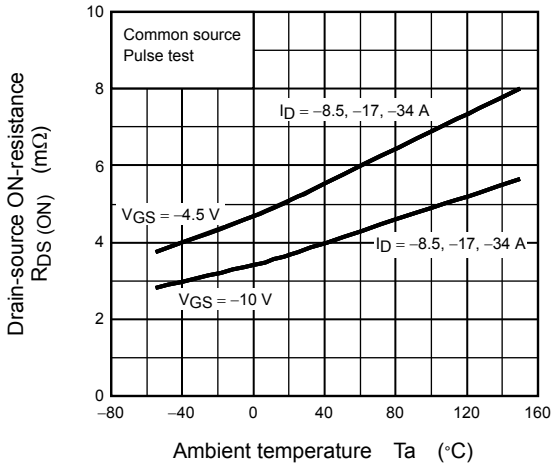
$V_{DS} - V_{GS}$



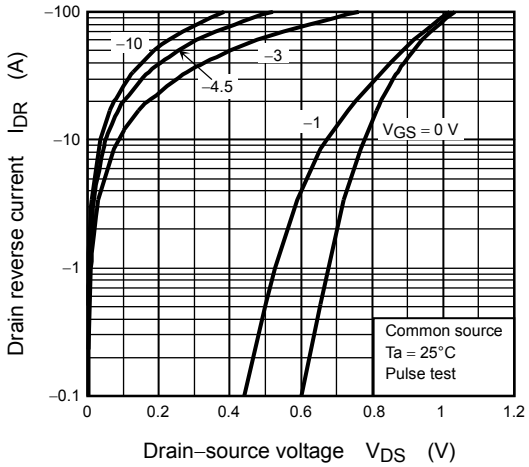
$R_{DS\ (ON)} - I_D$



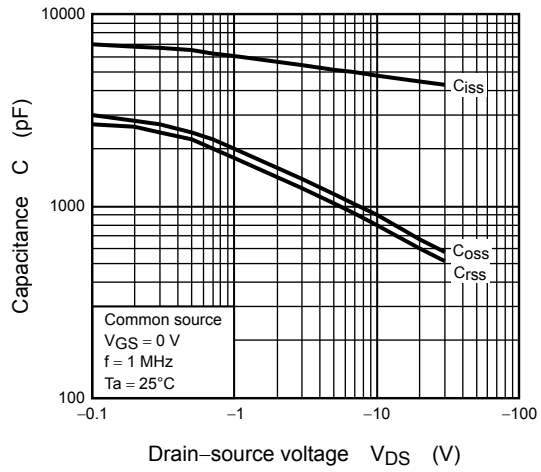
$R_{DS\ (ON)}$ – Ta



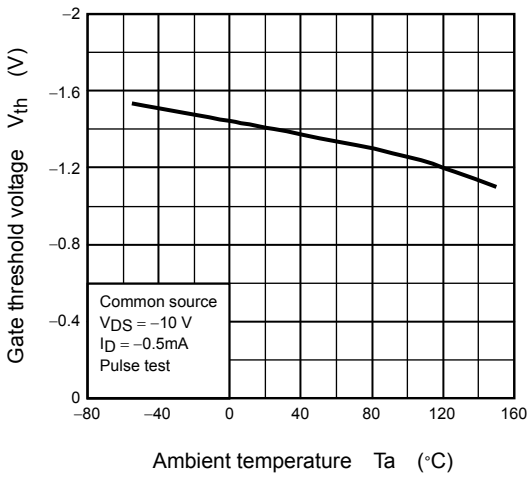
I_{DR} – V_{DS}



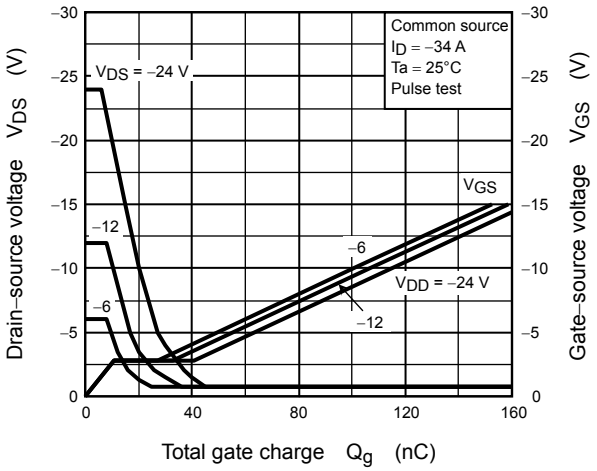
Capacitance – V_{DS}



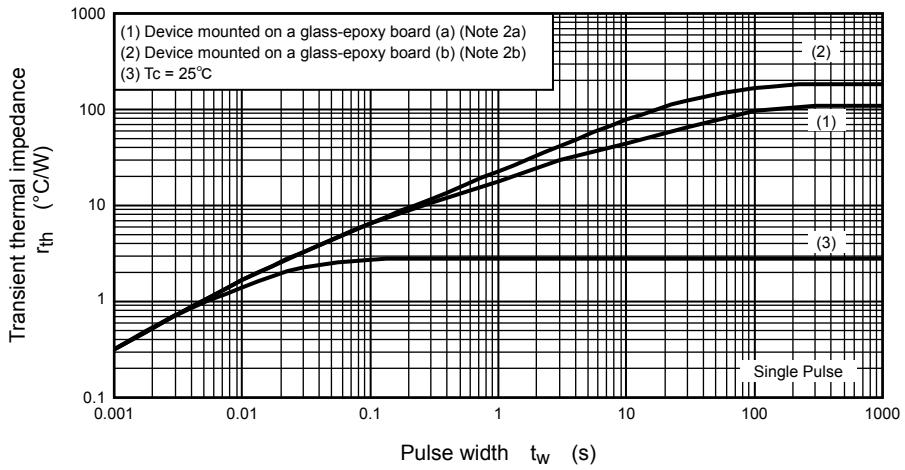
V_{th} – Ta



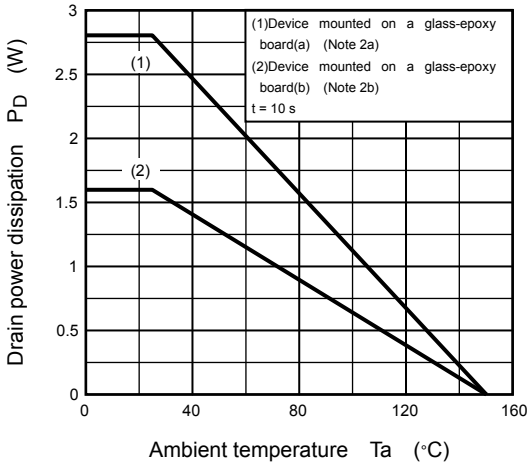
Dynamic input/output characteristics



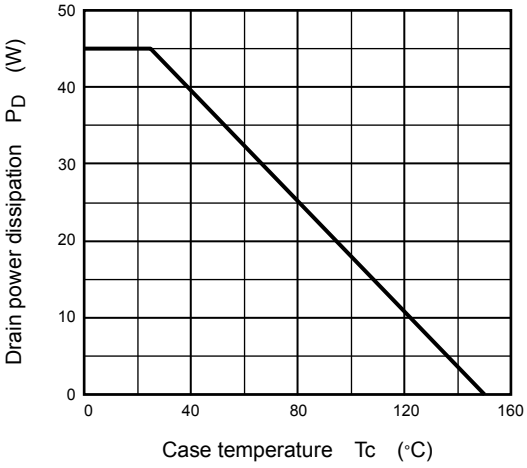
$r_{th} - t_w$



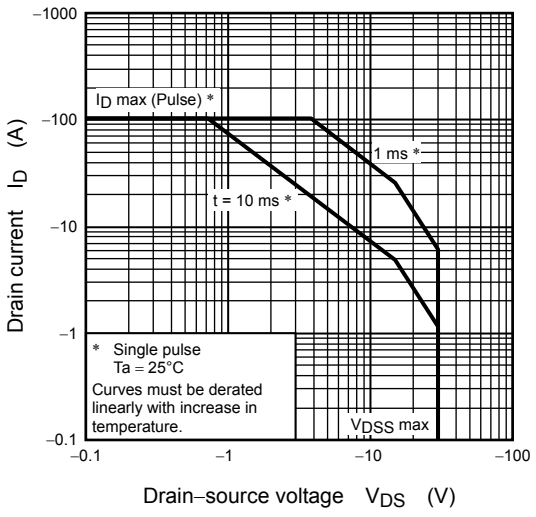
P_D – Ta



P_D – Tc



Safe operating area



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