

MOSFETs Silicon N-channel MOS (U-MOSIX-H)

TPH2R506PL

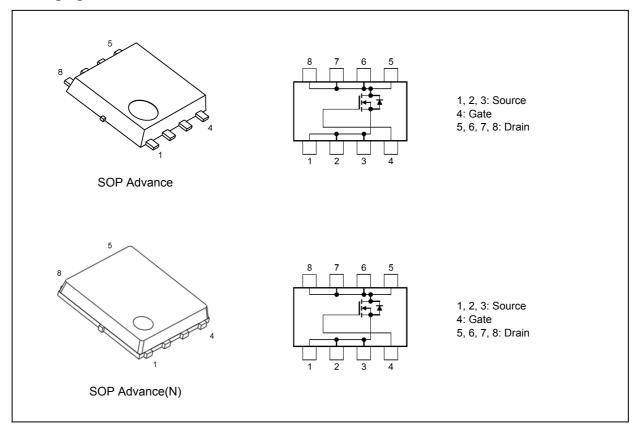
1. Applications

- · High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- · Motor Drivers

2. Features

- (1) High-speed switching
- (2) Small gate charge : $Q_{SW} = 19 \text{ nC (typ.)}$
- (3) Small output charge : $Q_{oss} = 51 \text{ nC}$ (typ.)
- (4) Low drain-source on-resistance : $R_{DS(ON)} = 1.9 \text{ m}\Omega \text{ (typ.)}(V_{GS} = 10 \text{ V})$
- (5) Low leakage current : $I_{DSS} = 10 \mu A (max)(V_{DS} = 60 V)$
- (6) Enhancement mode : V_{th} = 1.5 to 2.5 V (V_{DS} = 10 V, I_{D} = 0.5 mA)

3. Packaging and Internal Circuit



The package can be selected according to your preference. For details, please contact your TOSHIBA sales representative.

Start of commercial production



4. Absolute Maximum Ratings (Note) (Ta = 25 °C unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	60	V
Gate-source voltage			V_{GSS}	±20	
Drain current (DC)	(T _c = 25 °C)	(Note 1)	Ι _D	100	Α
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	I_D	160	
Drain current (pulsed)	(t = 100 μs)	(Note 1)	I _{DP}	500	
Power dissipation	(T _c = 25 °C)		P_{D}	132	W
Power dissipation		(Note 3)	P_{D}	3.0	
Power dissipation		(Note 4)	P_{D}	0.96	
Single-pulse avalanche energy		(Note 5)	E _{AS}	65	mJ
Single-pulse avalanche current		(Note 5)	I _{AS}	100	Α
Channel temperature			T _{ch}	175	°C
Storage temperature			T _{stg}	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit		
Channel-to-case thermal resistance	$(T_c = 25 °C)$		R _{th(ch-c)}	1.13	°C/W
Channel-to-ambient thermal resistance	(T _a = 25 °C)	(Note 3)	R _{th(ch-a)}	50	
Channel-to-ambient thermal resistance	(T _a = 25 °C)	(Note 4)	R _{th(ch-a)}	156	

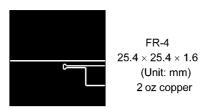
Note 1: Ensure that the channel temperature does not exceed 175 °C.

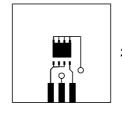
Note 2: Limited by silicon chip capability.

Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: V_{DD} = 48 V, T_{ch} = 25 °C (initial), L = 5 μ H, I_{AS} = 100 A





FR-4 $25.4 \times 25.4 \times 1.6$ (Unit: mm) 2 oz copper

Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±0.1	μА
Drain cut-off current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	
Drain-source breakdown voltage	V _{(BR)DSS}	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	60			>
Drain-source breakdown voltage (Note 6)	V _{(BR)DSX}	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	45	_	_	
Gate threshold voltage	V_{th}	$V_{DS} = 10 \text{ V}, I_{D} = 0.5 \text{ mA}$	1.5	_	2.5	
Drain-source on-resistance	R _{DS(ON)}	$V_{GS} = 4.5 \text{ V}, I_D = 30 \text{ A}$	_	2.8	4.4	mΩ
		V _{GS} = 10 V, I _D = 50 A	_	1.9	2.5	

Note 6: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V,	_	4180	5435	pF
Reverse transfer capacitance	C _{rss}	f = 1 MHz	_	60	115	
Output capacitance	C _{oss}		_	770	_	
Gate resistance	r _g	_	_	0.6	1.1	Ω
Switching time (rise time)	t _r	See Figure 6.2.1		7.1	_	ns
Switching time (turn-on time)	t _{on}		_	16	_	
Switching time (fall time)	t _f		_	13	_	
Switching time (turn-off time)	t _{off}		_	39		

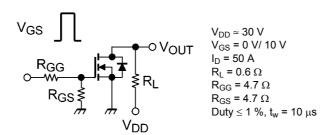


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$		60	1	nC
		$V_{DD} \approx 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 50 \text{ A}$		32		
Gate-source charge 1	Q _{gs1}	$V_{DD} \approx 30 \text{ V}, V_{GS} = 10 \text{ V},$	_	17	_	
Gate-drain charge	Q_{gd}	I _D = 50 A	_	11	_	
Gate switch charge	Q _{SW}		_	19	_	
Output charge	Q _{oss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz	_	51		



6.4. Source-Drain Characteristics ($T_a = 25$ °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (pulsed) (Note 7)	I _{DRP}	(t = 100 μs)	_	_	500	Α
Diode forward voltage	V _{DSF}	I _{DR} = 100 A, V _{GS} = 0 V		_	-1.2	V
Reverse recovery time	t _{rr}	I _{DR} = 25 A, V _{GS} = 0 V,		49		ns
Reverse recovery charge	Q_{rr}	-dI _{DR} /dt = 100 A/μs		57		nC

Note 7: Ensure that the channel temperature does not exceed 175 $^{\circ}\text{C}$.

7. Marking

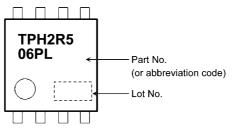


Fig. 7.1 Marking



8. Characteristics Curves (Note)

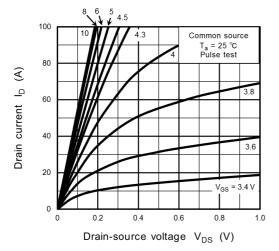


Fig. 8.1 I_D - V_{DS}

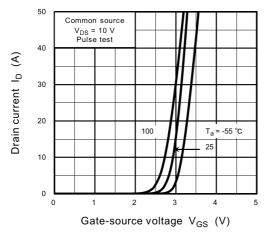


Fig. 8.3 I_D - V_{GS}

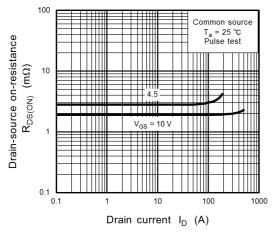


Fig. 8.5 R_{DS(ON)} - I_D

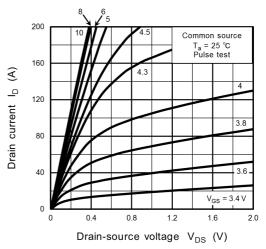


Fig. 8.2 I_D - V_{DS}

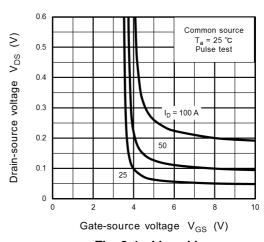


Fig. 8.4 V_{DS} - V_{GS}

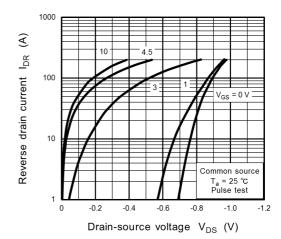


Fig. 8.6 IDR - VDS



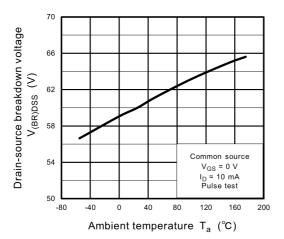


Fig. 8.7 V_{(BR)DSS} - T_a

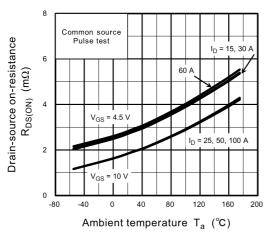


Fig. 8.9 R_{DS(ON)} - T_a

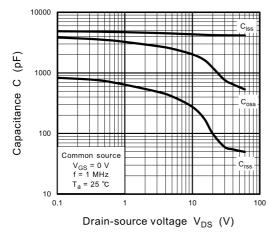


Fig. 8.11 Capacitance - V_{DS}

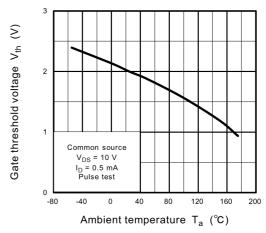


Fig. 8.8 V_{th} - T_a

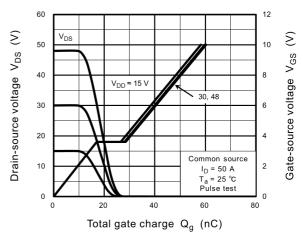


Fig. 8.10 Dynamic Input/Output Characteristics

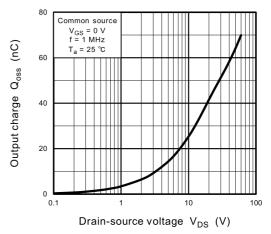


Fig. 8.12 Qoss - VDS



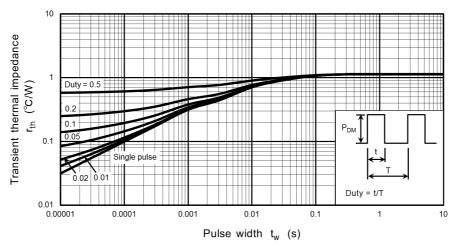


Fig. 8.13 r_{th} - t_w (Guaranteed Maximum)

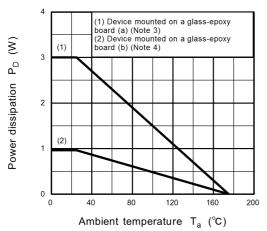


Fig. 8.14 P_D - T_a (Guaranteed Maximum)

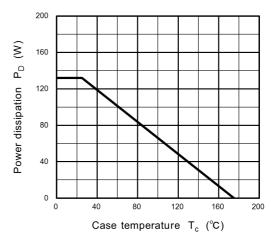


Fig. 8.15 P_D - T_c (Guaranteed Maximum)

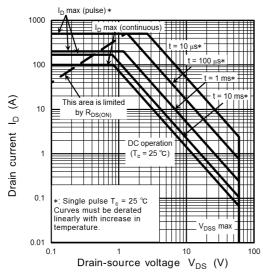


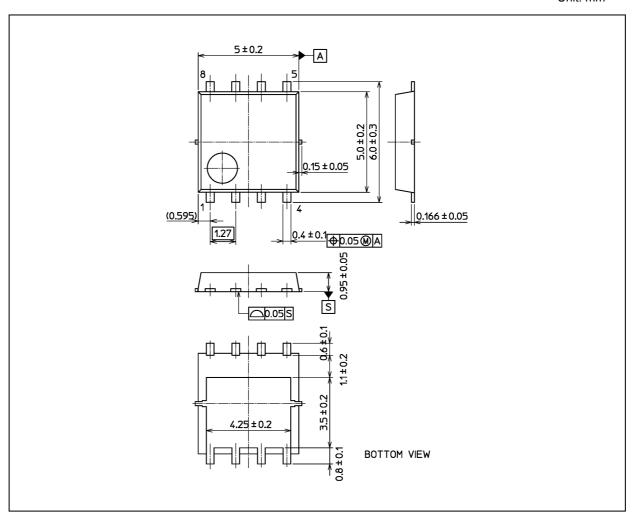
Fig. 8.16 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



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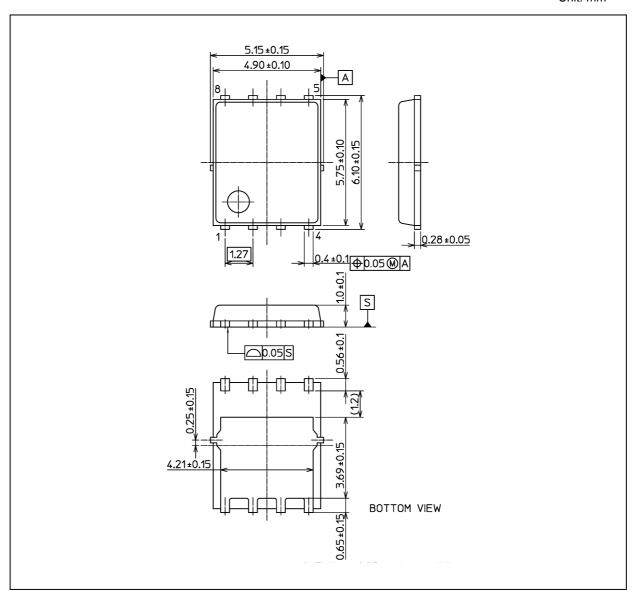
Weight: 0.079 g (typ.)

F	Package Name(s)
TOSHIBA: 2-5Q1S	
Nickname: SOP Advance	



Package Dimensions

Unit: mm



The package can be selected according to your preference. For details, please contact your TOSHIBA sales representative.

Weight: 0.105 g (typ.)

Package Name(s)
TOSHIBA: 2-5W1A
Nickname: SOP Advance(N)



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