

MOSFETs Silicon N-channel MOS (U-MOSVIII-H)

TPH6400ENH

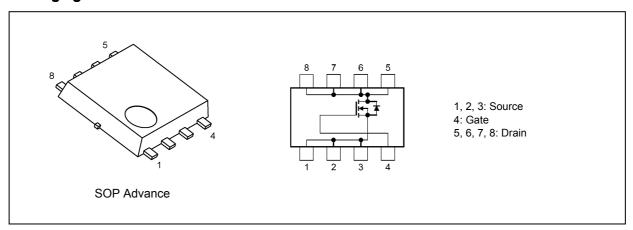
1. Applications

- · High-Efficiency DC-DC Converters
- Switching Voltage Regulators

2. Features

- (1) High-speed switching
- (2) Small gate charge: $Q_{SW} = 4.4 \text{ nC (typ.)}$
- (3) Low drain-source on-resistance: $R_{DS(ON)} = 54 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (4) Low leakage current: $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 200 \text{ V)}$
- (5) Enhancement mode: $V_{th} = 2.0 \text{ to } 4.0 \text{ V (V}_{DS} = 10 \text{ V, I}_{D} = 0.3 \text{ mA)}$

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25 °C unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	200	V
Gate-source voltage			V _{GSS}	±20	
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	I _D	21	Α
Drain current (DC)	(Continuous)	(Note 1)	I _D	13	
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I _{DP}	42	
Power dissipation	(T _c = 25 °C)		P_{D}	57	W
Power dissipation	(t = 10 s)	(Note 3)	P _D	2.8	
Power dissipation	(t = 10 s)	(Note 4)	P_{D}	1.6	
Single-pulse avalanche energy		(Note 5)	E _{AS}	56	mJ
Avalanche current			I _{AR}	13	Α
Channel temperature			T _{ch}	150	°C
Storage temperature			T _{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production



5. Thermal Characteristics

Characteristics			Symbol	Max	Unit
Channel-to-case thermal resistance	(T _c = 25 °C)		R _{th(ch-c)}	2.19	°C/W
Channel-to-ambient thermal resistance	(t = 10 s)	(Note 3)	R _{th(ch-a)}	44.6	
Channel-to-ambient thermal resistance	(t = 10 s)	(Note 4)	R _{th(ch-a)}	78.1	

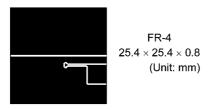
Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Limited by silicon chip capability.

Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: V_{DD} = 60 V, T_{ch} = 25 °C (initial), L = 510 μH , I_{AR} = 13 A



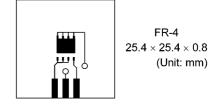


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

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6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±0.1	μА
Drain cut-off current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V	_	_	10	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	200	_	_	V
	V _{(BR)DSX}	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	140	_	_	
Gate threshold voltage	V_{th}	$V_{DS} = 10 \text{ V}, I_{D} = 0.3 \text{ mA}$	2.0	_	4.0	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 6.5 A		54	64	mΩ

6.2. Dynamic Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	_	810	1100	pF
Reverse transfer capacitance	C_{rss}		_	3	50	
Output capacitance	C _{oss}		_	90		
Gate resistance	r _g	_	_	2.8	4.2	Ω
Switching time (rise time)	t _r	See Fig. 6.2.1	_	5.4		ns
Switching time (turn-on time)	t _{on}		_	14.6	_	
Switching time (fall time)	t _f		_	5.2	_	
Switching time (turn-off time)	t _{off}		-	19		

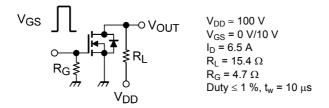


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} \approx 100 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 13 \text{ A}$	_	11.2		nC
Gate-source charge 1	Q _{gs1}			3.9		nC
Gate-drain charge	Q_{gd}		_	3.0		
Gate switch charge	Q_{SW}			4.4		

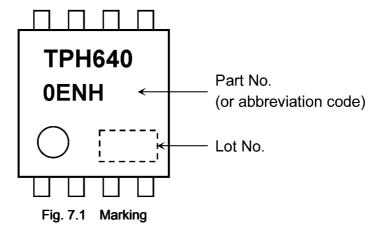
6.4. Source-Drain Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (pulsed)	(Note 6)	I _{DRP}	_	_	_	42	Α
Diode forward voltage		V_{DSF}	I _{DR} = 13 A, V _{GS} = 0 V			-1.2	V

Note 6: Ensure that the channel temperature does not exceed 150 °C.



7. Marking



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8. Characteristics Curves (Note)

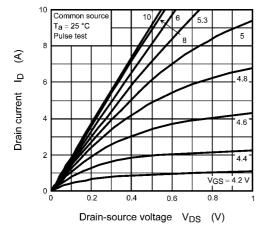
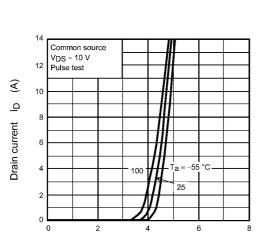


Fig. 8.1 I_D - V_{DS}



 $\label{eq:Gate-source} \mbox{Gate-source voltage} \quad \mbox{V}_{GS} \quad \mbox{(V)} \\ \mbox{Fig. 8.3} \quad \mbox{I}_{D} - \mbox{V}_{GS} \\ \mbox{}$

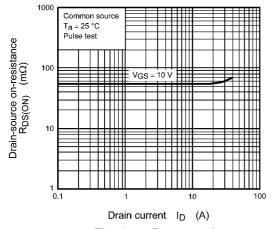


Fig. 8.5 R_{DS(ON)} - I_D

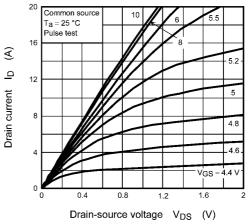


Fig. 8.2 I_D - V_{DS}

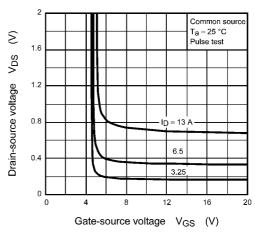


Fig. 8.4 V_{DS} - V_{GS}

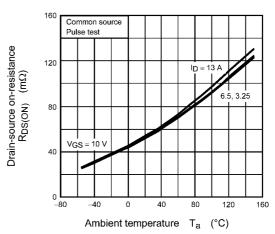


Fig. 8.6 R_{DS(ON)} - T_a

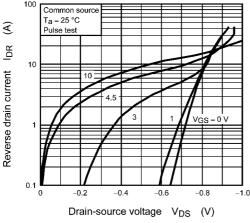


Fig. 8.7 IDR - VDS

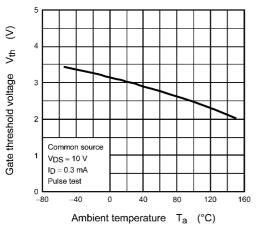


Fig. 8.9 V_{th} - T_a

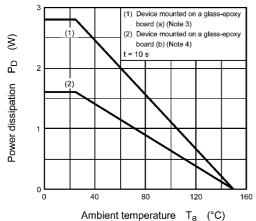


Fig. 8.11 P_D - T_a (Guaranteed Maximum)

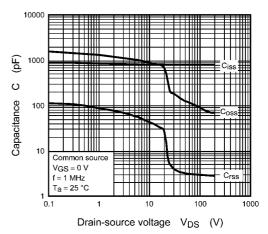


Fig. 8.8 Capacitance - V_{DS}

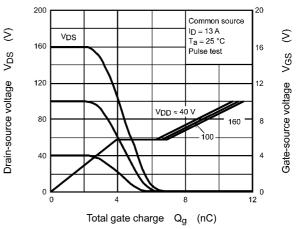


Fig. 8.10 Dynamic Input/Output Characteristics

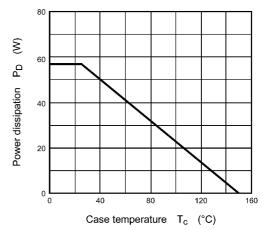


Fig. 8.12 P_D - T_c (Guaranteed Maximum)

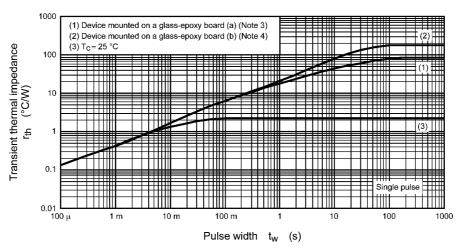


Fig. 8.13 r_{th} - t_w (Guaranteed Maximum)

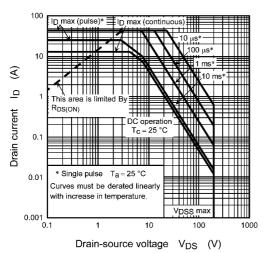


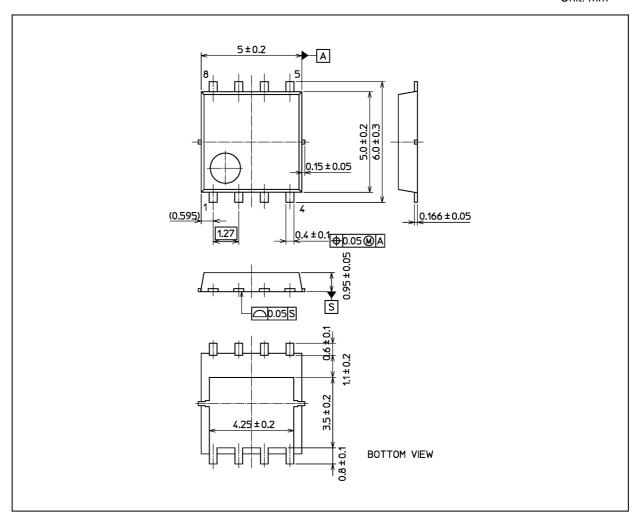
Fig. 8.14 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 0.069 g (typ.)

	Package Name(s)
TOSHIBA: 2-5Q1S	
Nickname: SOP Advance	

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