transphorm **User Guide**

TDTTP4000W066B: 4kW Bridgeless Totem-pole PFC Evaluation Board

Overview

This user guide describes the TDTTP4000W066B_0v1 4kW bridgeless totem-pole power factor correction (PFC) evaluation board. Very high efficiency single-phase AC-DC conversion is achieved with the TP65H035WS, a diode-free Gallium Nitride (GaN) FET bridge with low reverse-recovery charge. Using GaN FETs in the fast-switching leg of the circuit and low-resistance MOSFETs in the slow-switching leg of the circuit results in improved performance and efficiency. For more information and complete design files, please visit transphormusa.com/tp4kit. **The TDTTP4000W066B_0v1-KIT is for evaluation purposes only.**

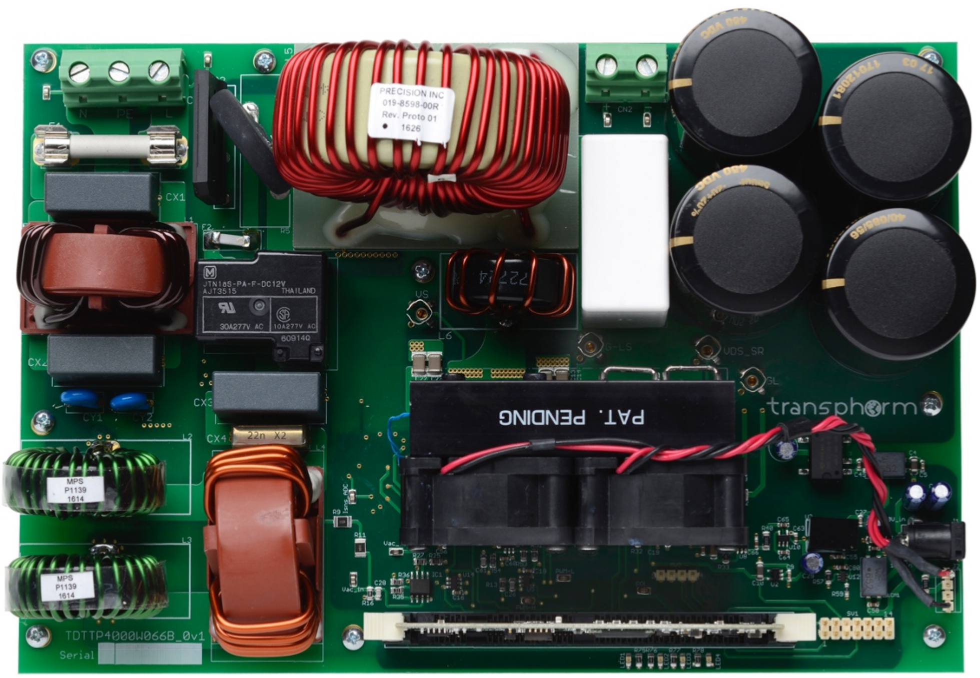

Figure 1. TDTTP4000W066B_0v1 4kW totem-pole PFC evaluation board

Warning

This evaluation board is intended to demonstrate GaN FET technology and is for demonstration purposes only and no guarantees are made for standards compliance.

There are areas of this evaluation board that have exposed access to hazardous high voltage levels. Exercise caution to avoid contact with those voltages. Also note that the evaluation board may retain high voltage temporarily after input power has been removed. Exercise caution when handling.

When testing converters on an evaluation board, ensure adequate cooling. Apply cooling air with a fan blowing across the converter or across a heatsink attached to the converter. Monitor the converter temperature to ensure it does not exceed the maximum rated per the datasheet specification.

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TDTTP4000W066B input/output specifications

- Input voltage: 85V_{AC} to 265V_{AC}, 47Hz to 63Hz
- Input current: 18Arms; 2000W at 115V_{AC}, 4000W at 230V_{AC})
- 10% overload short time: 19.8Arms; 2200W at 115V_{AC}, 4400W at 230V_{AC})
- Ambient temperature: <50°C
- Output voltage: 387V_{DC} ± 5V_{DC}
- PWM frequency: 66kHz
- Auxiliary supply: 12V_{DC} for bias voltage
- Power dissipation in the GaN FET: Limited by the maximum junction temperature; refer to the TP65H035WS datasheet

Figure 2 shows the input and output connections. To reduce EMI noise, adding a ferrite core at both the input and output is recommended.

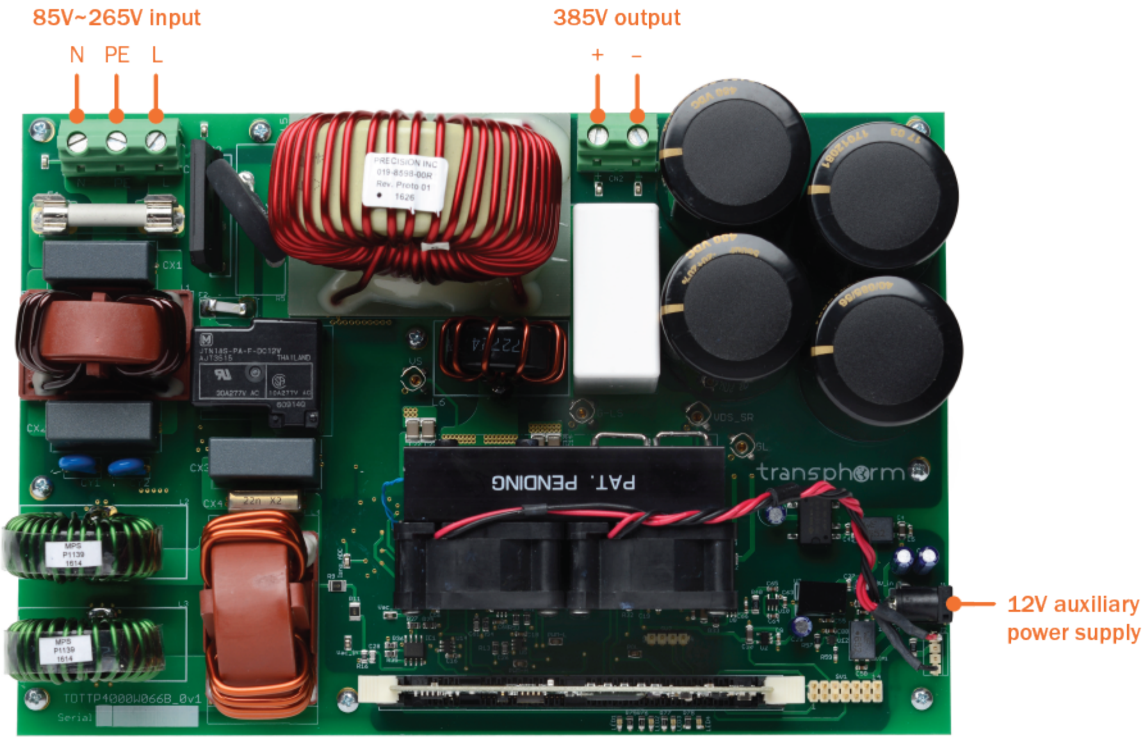


Figure 2. Input and output cable connections

Circuit description

The bridgeless totem-pole PFC topology is shown in Figure 3. Two GaN FETs and two low-resistance silicon (Si) MOSFETs are used to eliminate diode drops and improve efficiency. Further information and discussion on the performance and the characteristics of the bridgeless PFC circuit is provided in [1].

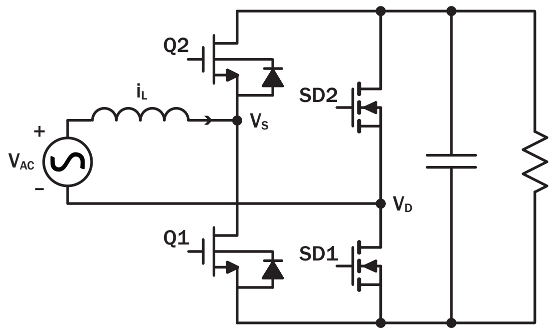


Figure 3. Bridgeless totem-pole PFC boost converter based on low-resistance MOSFETs for line rectification

Figure 4(a) is a simplified schematic of a totem-pole PFC in continuous conduction mode (CCM) mode, focused on minimizing conduction losses. It comprises two fast-switching GaN FETs (Q1 and Q2) operating at a high pulse-width-modulation (PWM) frequency and two very low-resistance MOSFETs (S1 and S2) operating at a much slower line frequency (50Hz/60Hz). The primary current path includes one fast switch and one slow switch only, with no diode drop. The function of S1 and S2 is that of a synchronized rectifier as illustrated in Figures 4(b) and 4(c). During the positive AC cycle, S1 is on and S2 is off, forcing the AC neutral line tied to the negative terminal to the DC output. The opposite applies for the negative cycle.

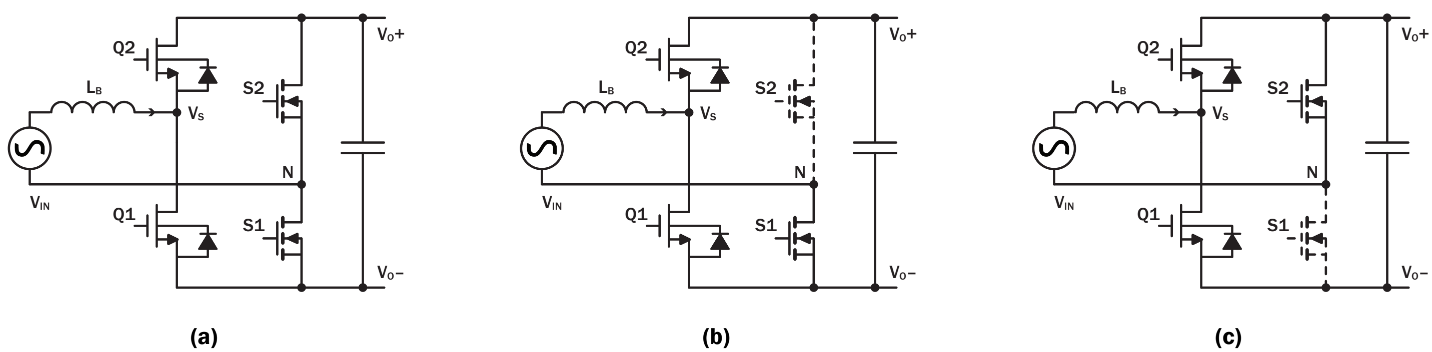
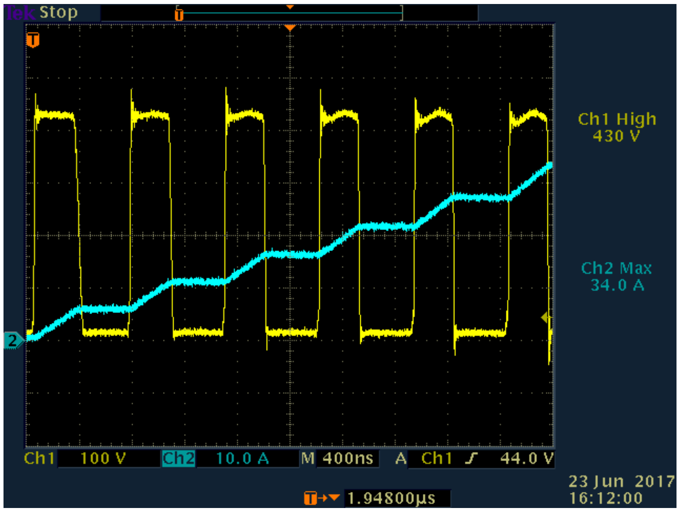


Figure 4. Totem-pole PFC with GaN FETs (a) simplified schematic, (b) during positive AC cycle and (c) during negative AC cycle

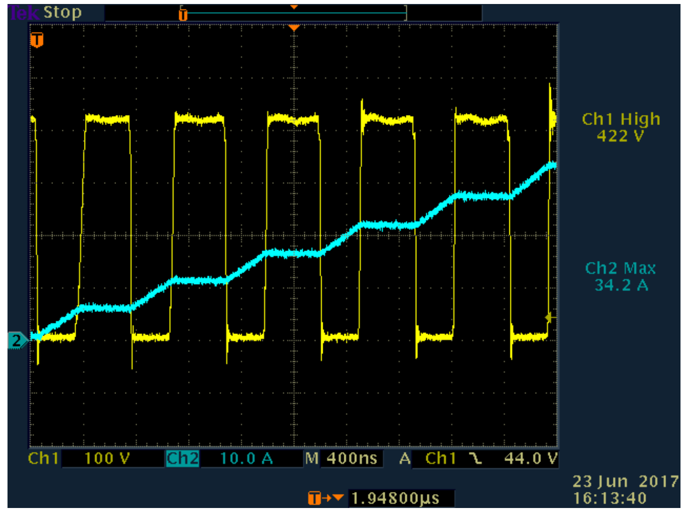
In either AC polarity, the two GaN FETs form a synchronized boost converter with one transistor acting as a master switch to allow energy intake by the boost inductor (LB), and another transistor as a slave switch to release energy to the DC output. The roles of the two GaN devices interchange when the polarity of the AC input changes; therefore, each transistor must be able to perform both master and slave functions. To avoid shoot-through a dead time is built in between two switching events, during which both transistors are momentarily off. To allow CCM operation, the body diode of the slave transistor must function as a flyback diode for the inductor current to flow during dead time. The diode current; however, must quickly reduce to zero and transition to the reverse blocking state once the master switch turns on.

This is the critical process for a totem-pole PFC which, with the high Q_{rr} of the body diode of high-voltage Si MOSFETs, results in abnormal spikes, instability, and associated high switching losses. The low Q_{rr} of the GaN switches allows designers to overcome this barrier.

As seen in Figure 5, inductive tests at 430V bus show healthy voltage waveforms up to inductor current exceeding 35A using either a high-side (Figure 5(a)) or low-side (Figure 5(b)) GaN transistor as a master switch. With a design goal of 4.4kW output power in CCM mode at 230V_{AC} input, the required inductor current is 20A. This test confirms a successful totem-pole power block with enough current overhead.



(a) High side



(b) Low side

Figure 5. Waveforms of two hard-switched GaN FETs when setting (a) high-side as a master and (b) low-side as a master

One issue inherent in the bridgeless totem-pole PFC is the operation mode transition at AC voltage zero-crossing. For instance, when the circuit operation mode changes from positive half-line to negative half-line at the zero-crossing, the duty ratio of the high-side GaN switch changes abruptly from almost 100% to 0% and the duty ratio of low-side GaN switch changes from 0% to 100%. Due to the slow reverse recovery of diodes (or body diode of a MOSFET), the voltage V_D cannot jump from ground to V_{DC} instantly; a current spike will be induced. To avoid the problem, a soft-start at every zero-crossing is implemented to gently reverse duty ratio (a soft-start time of a few switching cycles is enough). The TDTTP4000W066B evaluation board is designed to run in CCM and the larger inductance alleviates the current spike issue at zero-crossing.

Dead time control

The required form of the gate-drive signals is shown in Figure 5. The times marked A are the dead times when neither transistor is driven on. The dead time must be greater than zero to avoid shoot-through currents. The Si8230 gate drive chip ensures a minimum dead time based on the value of resistor R24, connected to the DT input. The dead time in ns is equal to the resistance in kΩ x 10, so the default value of 12k corresponds to 120ns. This will add to any dead time already present in the input signals. The on-board pulse generator circuit; for example, creates dead times of about 60ns (see Figure 6). The resulting dead time at the gate pins of Q1 and Q2 is about 120ns. Either shorting or removing R7 will reduce the dead time to 60ns.

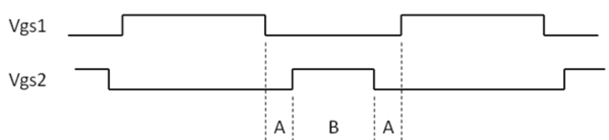


Figure 6. Non-overlapping gate pulses

While a typical Si MOSFET has a maximum dV/dt rating of 50V/ns, the TP65H035WS GaN FET will switch at dV/dt of 100V/ns or higher to achieve the lowest possible switching loss. At this level of operation, even the layout becomes a significant contributor to performance. As shown in Figure 8, the recommended layout keeps a minimum gate drive loop and keeps the traces between the switching nodes very short--with the shortest practical return trace to the power bus and ground. The power ground plane provides a large cross-sectional area to achieve an even ground potential throughout the circuit. The layout carefully separates the power ground and the IC (small signal) ground, only joining them at the source pin of the FET to avoid any possible ground loop.

Note that the Transphorm GaN FETs in TO-247 packages have pinout configuration of G-S-D, instead of the traditional G-D-S of a MOSFET. The G-S-D configuration is designed with thorough consideration to minimize the gate source driving loop, reducing parasitic inductance and to separate the driving loop (gate source) and power loop (drain source) to minimize noise. All PCB layers of the TDTTP4000W066B_0V1 design are shown Figure 8(a-c) and available in the design files.

Design details

A detailed circuit schematic is shown in Figures 7 and 8, the PCB layers in Figure 9, and the parts list in Table 1 (also included in the design files).

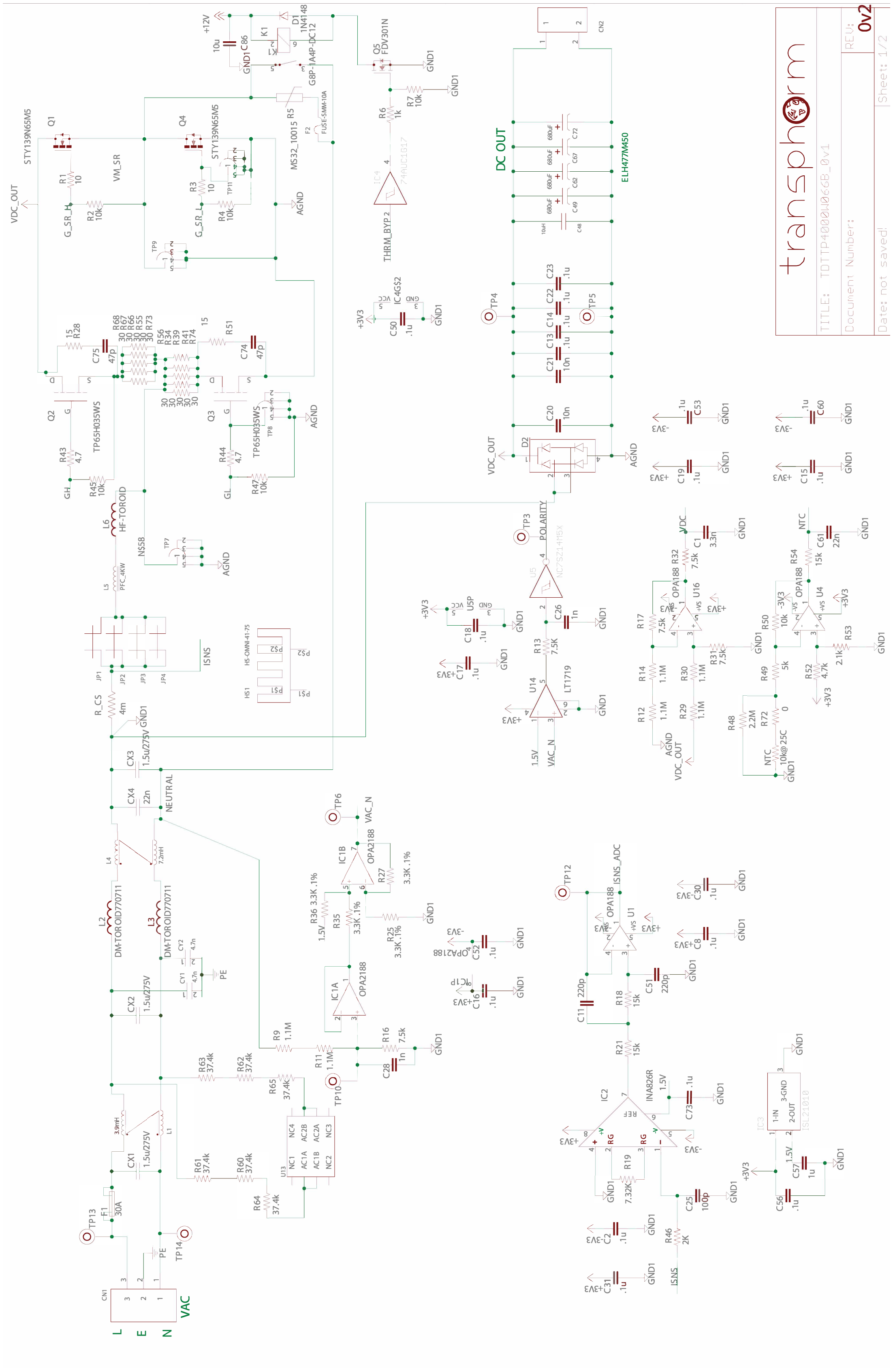


Figure 7. Detailed circuit schematic (1 of 2)

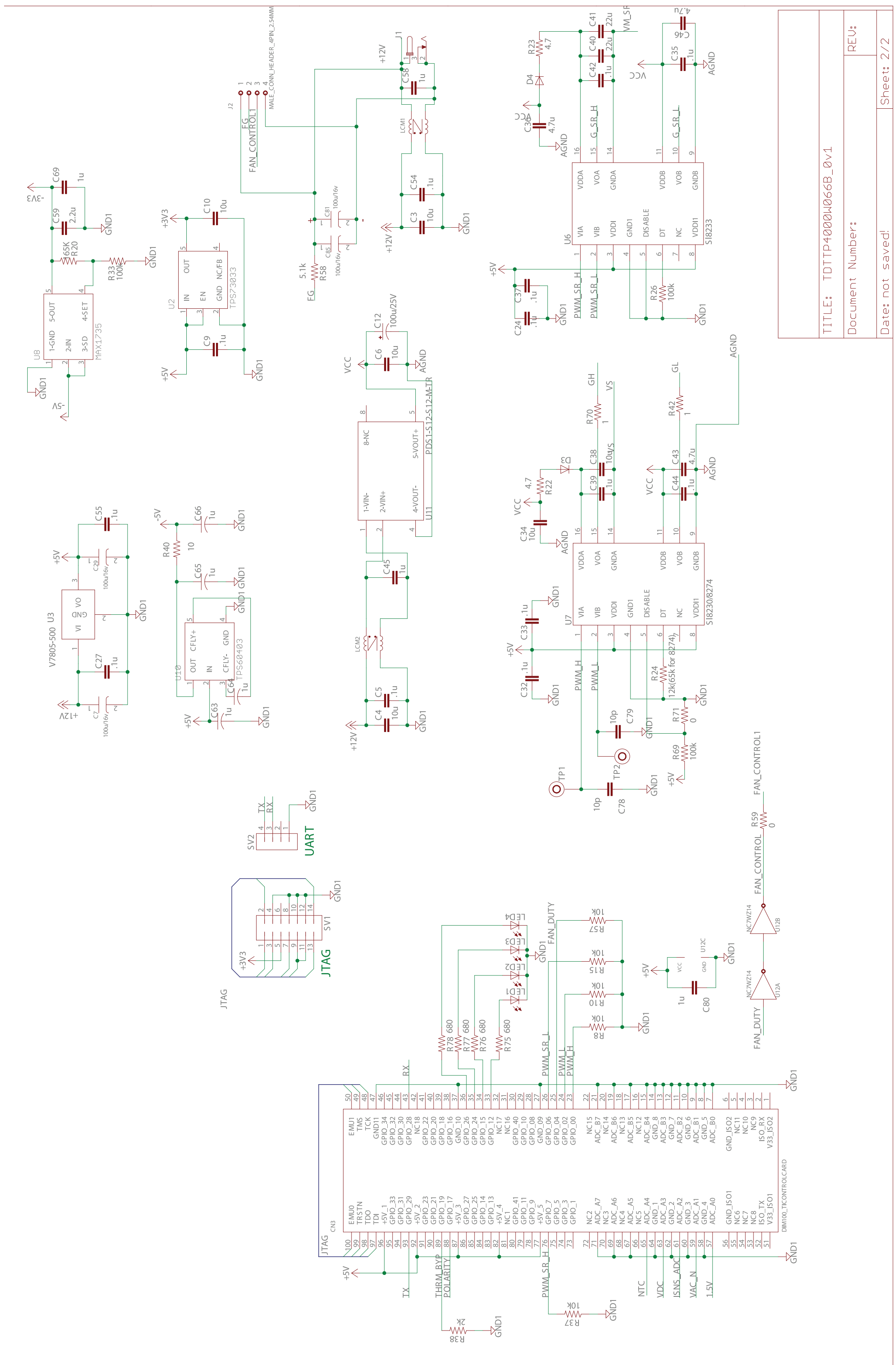


Figure 8. Detailed circuit schematic (2 of 2)

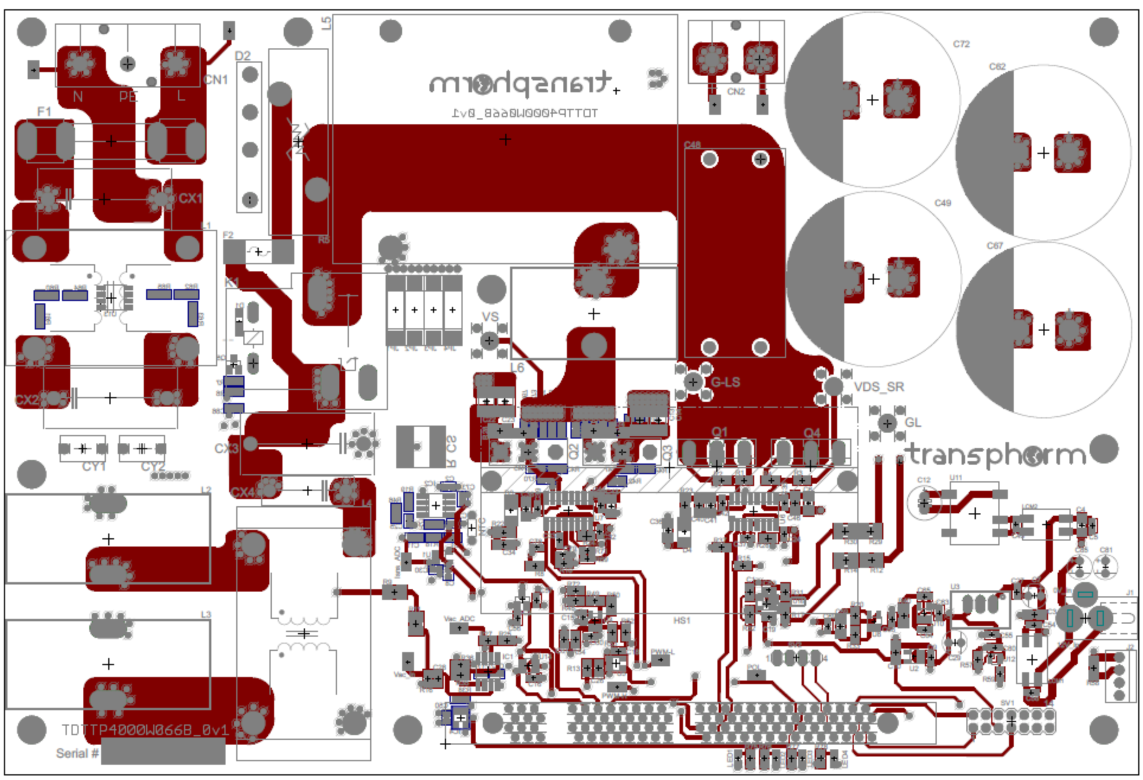
Table 1. TDTTP4000W066B evaluation board bill of materials (BOM)

Designator	Qty	Value	Descriptor/Package	Manufacturer Part Number	Manufacturer
D3, D4	2		DO-214AC, SMA	ES1J	Micro Commercial
D2	1		4-SIP, GBJ	GBJ2506-BP	Micro Commercial
LED1, LED2, LED3, LED4	4		0805 (2012 metric)	SML-211UTT86	ROHM Semiconductor
SV2	1		MA04-1	961104-6404-AR	3M
SV1	1		MA07-2	67996-114HLF	FCI
J1	1			PJ-002AH	CUI
TP7, TP8, TP9, TP11	4		Probe connector	131-4353-00	Tektronix
TP1, TP2, TP3, TP4, TP5, TP6, TP10, TP12, TP13, TP14	10			5015	Keystone
C2, C5, C8, C9, C15, C16, C17, C18, C19, C24, C27, C30, C31, C32, C33, C35, C37, C39, C42, C44, C50, C52, C53, C54, C55, C56, C60, C73	28	0.1μF	C0603	C0603C104J3RACTU	Kemet
C13, C14, C22, C23	4	0.1μF	C1812	C1812V104KDRACTU	Kemet
R59, R71	2	0	R0603	RCS06030000Z0EA	Vishay
R72	1	0	R0805	RC0805JR-070RL	Yageo
R42, R70	2	1Ω	R0805	RMCF0805FT1R00	Stackpole
R9, R11, R12, R14, R29, R30	6	1.1MΩ	R1210	KTR25JZPF1104	ROHM Semiconductor
CX1, CX2, CX3	3	1.5μF/275V	Radial	155MKP275KG	Illinois Capacitor
R1, R3	2	10Ω	R0805	ERJ-6GEYJ100V	Panasonic
R40	1	10Ω	R1206	ERJ-8ENF10R0V	Panasonic
R26, R33	2	100kΩ	R0805	RJ-6ENF1003V	Panasonic
C25	1	100pF	C0603	06035A101FAT2A	AVX Corporation
C7, C29, C81, C85	4	100μF/16V	Radial, Can	UKL1C101KPDANA	Nichicon
C12	1	100μF/25V	Radial, Can	ESK107M025AC3AA	Kemet
R2, R4, R7, R8, R10, R15, R37, R45, R47, R50, R57	11	10kΩ	R0805	ERJ-6ENF1002V	Panasonic
NTC	1	10kΩ @25°C	Ring Lug	B57703M103G40	EPCOS (TDK)
C20, C21	2	10nF	C1206	SMK316B7103KF-T	Taiyo Yuden
C78, C79	2	10pF	C0603	C0603C100K3GACTU	Kemet
C86	1	10μF	C0805	GRM21BR61E106KA73L	Murata
C3, C4, C6, C10, C34, C38	6	10μF	C1206	12063D106KAT2A	AVX
C48	1	10μH	Radial - 4 Leads	C4ATGBW5100A3FJ	Kemet
R24	1	12kΩ (65k for 8274)	R0805	RC0805FR-0712KL	Yageo
R28, R51	2	15Ω	R1210	RMCF1210FT15R0	Stackpole
R18, R21, R54	3	15kΩ	R0805	05FR-0715KL	Yageo
R20	1	165kΩ	R0805	ERJ-6ENF1653V	Panasonic
D1	1		SOD-123	1N4148W-E3-18	Vishay
R6	1	1kΩ	R0805	ERJ-6ENF1001V	Panasonic
C26, C28	2	1nF	C0805	CC0805KRX7R9BB102	Yageo
C45, C57, C58, C69, C80, C63, C64, C65, C66	9	1μF	C0603	TMK107B7105KA-T	Taiyo Yuden
R53	1	2.1kΩ	R0805	RC0805FR-072K1L	Yageo
R48	1	2.2MΩ	R0805	RMCF0805JT2M20	Stackpole
C59	1	2.2μF	C1206	CL31B225KAHNNNE	Samsung Electro
C11, C51	2	220pF	C0805	CC0805KRX7R9BB221	Yageo
C61	1	22nF	C0805	C2012C0G1V223J060AC	TDK
CX4	1	22nF	ECQ-U2A224ML	PME271M522MR30	Kemet
C40, C41	2	22μF	C1206	CL31X226KAHN3NE	Samsung Electro

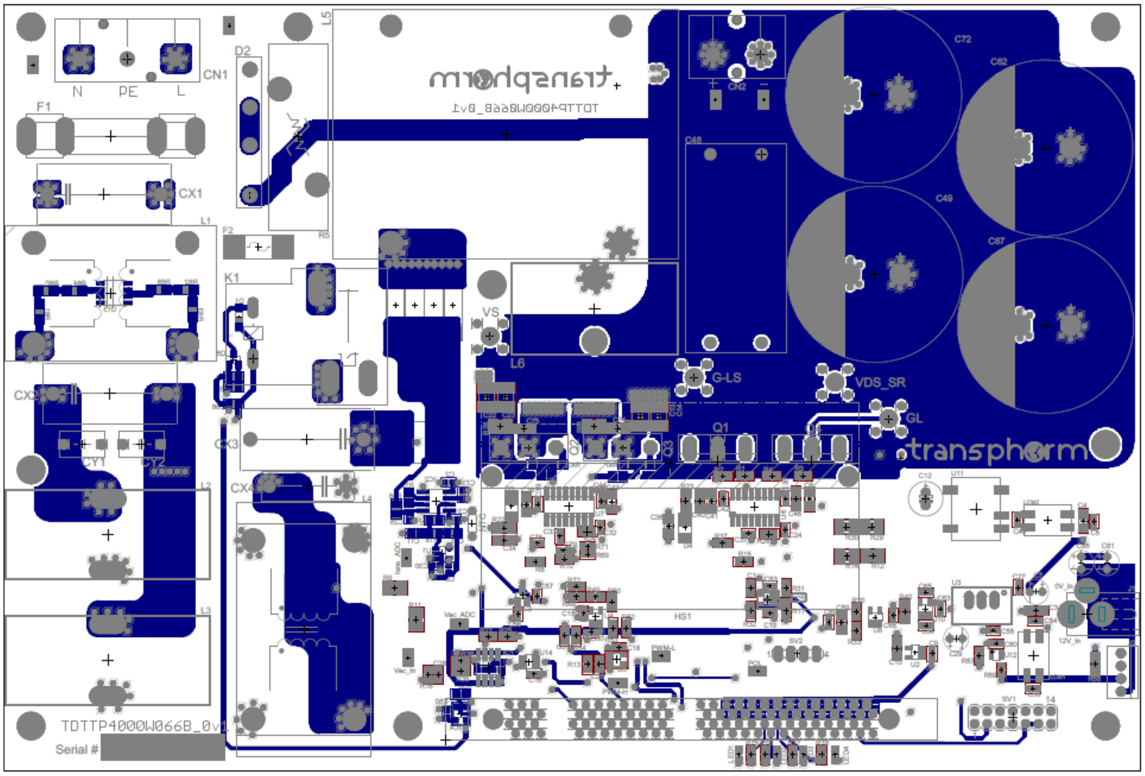
Designator	Qty	Value	Descriptor/Package	Manufacturer Part Number	Manufacturer
R38, R46	1	2kΩ	R0805	ERJ-6ENF2001V	Panasonic
CN2	1		2PIN_9.53MM	20020705-M021B01LF	FCI
R25, R27, R35, R36	4	3.3kΩ 0.1%	R0805	ERA-6AEB332V	Panasonic
C1	1	3.3nF	C0805	C0805C332K5RACTU	Kemet
L1	1	3.9mH	CMC_42X27MM_SM	T60405-R6128-X225	Vacuumschmelze
R34, R39, R41, R55, R56, R66, R67, R68, R73, R74	10	30Ω	R0805	BLM21SN300SH1D	Murata
F1	1	30A	SH32	01020078H	Littelfuse
R60, R61, R62, R63, R64, R65	6	37.4kΩ	R1206	RC1206FR-0737K4L	Yageo
CN1	1		3PIN 9.53MM	20020316-H031B01LF	FCI
R43, R44	2	4.7Ω	R0805	RNCP0805FTD4R70	Stackpole
R22, R23	2	4.7Ω	R1206	CRM1206-JW-4R7ELF	Bourns
R52	1	4.7kΩ	R0805	RC0805FR-074K7L	Yageo
CY1, CY2	2	4.7nF	VY2_CAP_SAFETY	B32021A3472M	EPCOS (TDK)
C36, C43, C46	3	4.7µF	C1206	CL31B475KBHNNNE	Samsung Electro
C74, C75	2	47pF	C1206	CC1206JKNPOZBN470	Yageo
R_CS	1	4mΩ	Wide 2827	CSSH2728FT4L00	Stackpole
R58	1	5.1kΩ	R1206	RC1206FR-075K1L	Yageo
R49	1	5kΩ	R0805	RC0805FR-075K1L	Yageo
R75, R76, R77, R78	4	680Ω	R0805	RC0805FR-07680RL	Yageo
C49, C62, C67, C72	4	560µF	ELE_CAP_D35MM_P10	ALC10A561DF450	Kemet
L4	1	7.2mH	CMC_42X27MM	T60405-R6128-X230	Vacuumschmelze
R19	1	7.32kΩ	R0805	RC0805FR-077K32L	Yageo
R13	1	7.5kΩ	R0805	ERJ-6ENF7501V	Panasonic
R16, R17, R31, R32	4	7.5kΩ	R0805	RN73C2A7K5BTDF	Panasonic
IC4	1		SOT-23-5	SN74LVC1G17DBVR	Texas Instruments
LCM1, LCM2	2		CMC_WURTH_744229	744229	Wurth
CN3	1		DIM100	5390213-1	TE Connectivity
L2, L3	2		DM-77071B	CWS-1SN-12606	CWS
Q5	1		SOT-23	FDV301N	Fairchild/ON Semiconductor
F2	1	10A	SMM-FUSE	65800003109	Littelfuse
K1	1		G8P-1A4P	JTN1AS-PA-F-DC12V	Panasonic Electric Works
L6	1		DM-77894-AWG11	CWS-1SN-12554	CWS
HS1	1		HS-OMNI-41-75	OMNI-UNI-41-75	Wakefield-Vette
IC2	1		SO8	INA826AID	Texas Instruments
IC3	1		SOT-23-3	ISL21010CFH315Z-TK	Intersil
JP1, JP2, JP3, JP4	4		JUMPER-S1621-46R	S1621-46R	Harwin Inc
U14	1		TSOT-23	LT1719CS6#TRMPBF	Linear Technology
J2	1		MALE_CONN_HEADER_4PIN_2.54MM	961104-6404-AR	3M
U8	1		SOT-23-5	MAX1735EUK50+T	Maxim Integrated
R5	1		MS35_10018	MS32 10015-B	Ametherm
U5	1		SOT-23-5	NC7SZ14M5X	Fairchild/ON Semiconductor
U12	1		SC70	NC7WZ14P6X	Fairchild/ON Semiconductor
U13	1		SOIC-8	NCP4810DR2G	ON Semiconductor
U1, U4, U16	3		SOT-23-5	OPA188AIDBVT	Texas Instruments
IC1	1		SO8	OPA2188AIDR	Texas Instruments
U11	1		8-SMD Module, 5 Leads, Gull Wing	PDS1-S12-S12-M-TR	CUI
L5	1		PFC_4KW	019-8598-00R	Precision
U7	1		SOIC16N	SI8230BB-D-IS1	Silicon Labs
U6	1		SOIC16N	SI8233BB-D-IS1	Silicon Labs
Q1, Q4	2		TO-247AD-V	STY139N65M5	STMicroelectronics
Q2, Q3	2		TO-247	TP65H035WS	Transphorm

Designator	Qty	Value	Descriptor/Package	Manufacturer Part Number	Manufacturer
U10	1		SOT-23-5	TPS60403DBVR	Texas Instruments
U2	1		SOT-23-5	TPS73033DBVR	Texas Instruments
U3	1		3-SIP Module	V7805-500	CUI
	1		Control Card	TMS320F28335	Texas Instruments
	9		Standoff (nylon 1/2)	1902C	Keystone
	9		Machine Screw (ss 1/2)	9902	Keystone
	2		Thermal Pad for Q2, Q3	4169G	Avid Thermollogy
	2		6/32 Screws for FETs to HS (Q2, Q3)		

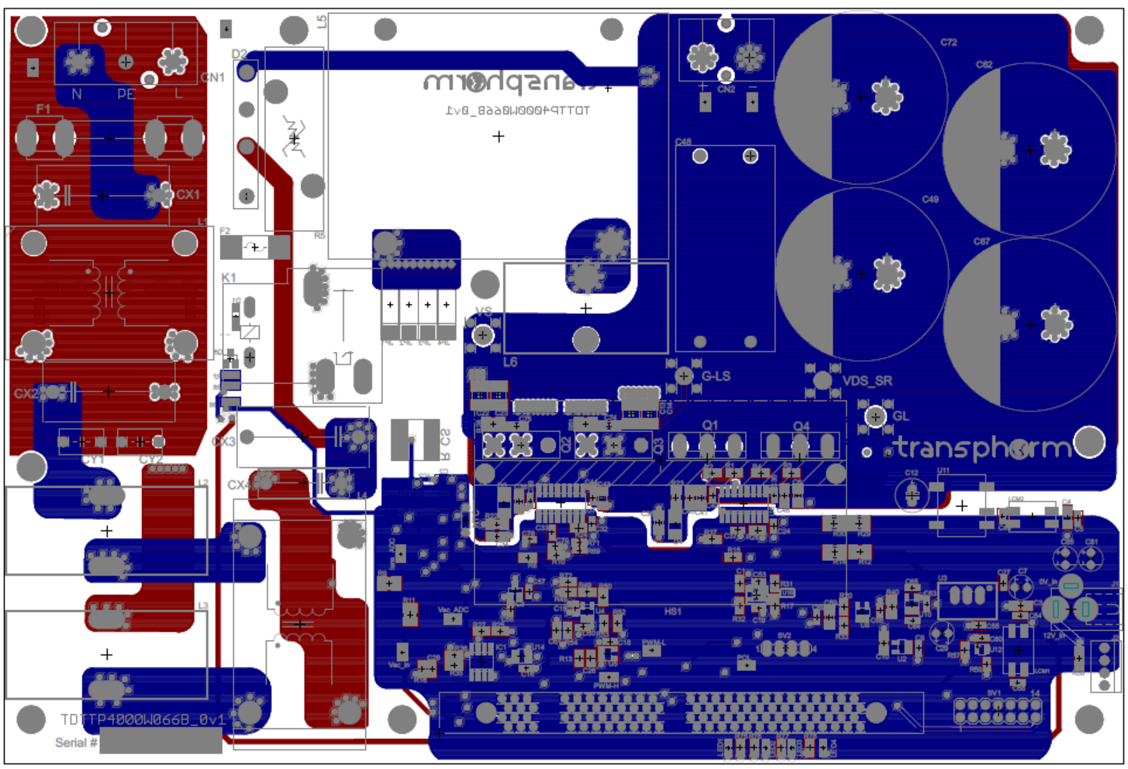
For TDTTP4000W066B evaluation board, the PFC circuit has been implemented on a 4-layer PCB. The GaN FET half-bridge is built with Transphorm's TP65H035WS (35mΩ) GaN FET. The slow Si switches are STY139N65M5 (17mΩ) superjunction MOSFETs. The inductor is made of a High Flux core with an inductance of 480µH and a DC resistance of 25mΩ and designed to operate at 66kHz. A simple 0.5A rated high/low side driver IC (Si8230) with 0/12V as on/off states directly drives each GaN FET. A 150MHz DSP (TMS320F28335) handles the control algorithm. The voltage and current loop controls are similar to a conventional boost PFC converter. The feedback signals are DC output voltage (V_O), AC input potentials (V_{ACP} and V_{ACN}) and inductor current (I_L). The input voltage polarity and RMS value are determined from V_{ACP} and V_{ACN}. The outer voltage loop output multiplied by $|V_{AC}|$ gives a sinusoidal current reference. The current loop gives the proper duty ratio for the boost circuit. The polarity determines how PWM signal is distributed to drive Q1 and Q2. A soft-start sequence with a duty ratio ramp is employed for a short period at each AC zero-crossing for better stability.



(a) PCB top layer



(b) PCB bottom layer



(c) PCB inner layer 2 (ground plane) + inner layer 3 (power plane)

Figure 9. PCB layers

Using the board

The TDTTP4000W066B board can be used for evaluating Transphorm GaN FETs in a bridgeless totem-pole PFC circuit and is building block but not a complete circuit.

Powering on the board

1. Insert the control card and verify LED1 is on
2. Connect an electronic/resistive load to the corresponding marking (CN2). The requirements for the resistive load are
   - At 115V_{AC} input: 0W and ≤2200W
   - At 230V_{AC} input: 0W and ≤4400W
3. Connect the 12V_{DC} auxiliary supply (included) to the evaluation board
4. Verify that both fans attached to the heatsink are running
5. With high-voltage power off, connect the high-voltage AC power input to the corresponding marking (CN1) on the PCB; N and L (PE: potential ground)
6. Turn on the AC power input (85V_{AC} to 265V_{AC}, 50kHz to 60kHz); minimum power load for turn-on sequence is 350W
7. Monitor CN2 output voltage with V_{DC} meter to verify that 385V ±5V is generated
8. Electronic/resistive load can be increased while AC supply is on and board is functional

Powering off the board

1. Switch off the high-voltage AC power input
2. Power off DC bias

Operational waveforms

Figure 10 shows the converter start-up procedure: DC input current (CH1), DC bus voltage waveform (CH2), and voltage waveform of the fast leg switching node (CH3). For the start up, there are three phases to charge the DC bus to a reference voltage.

1. In the beginning the relay K1 is open and DC bus capacitors are charged by input voltage through NTC and diode bridge
2. When the V_{DC} is over 100V, K1 is closed to bypass the NTC and the V_{DC} increases to the peak of the input voltage
3. After 100ms, the leg of the GaN FET is engaged in voltage closed-loop control and the DC bus voltage reference slowly increases to the rated voltage 385V

The NTC and diode bridge are applied in this circuit to avoid high inrush current flow through the GaN FETs.

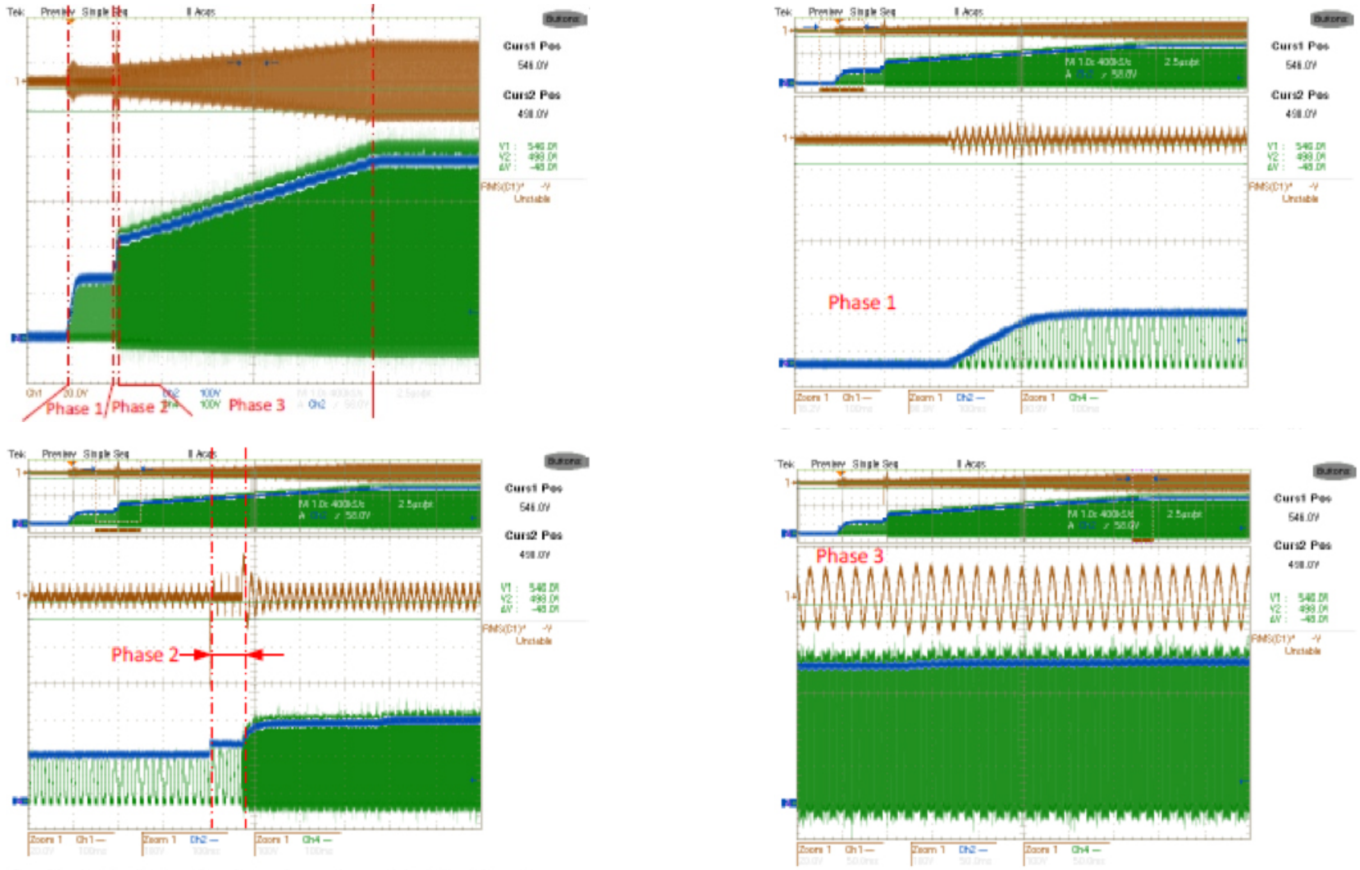
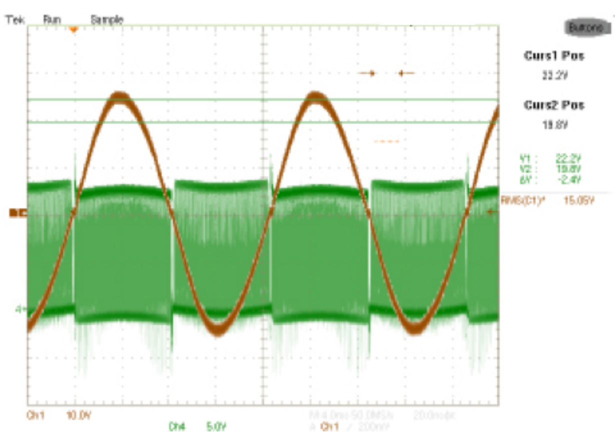
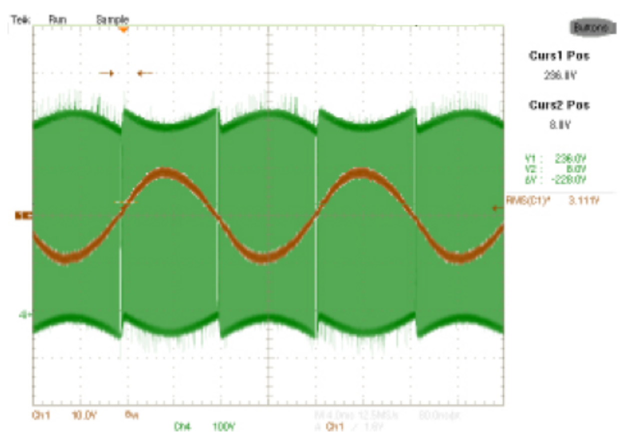


Figure 10. Start-up of the bridgeless totem-pole PFC with 1.2kW load
CH1: I_{IN}, CH2: V_O, CH3: V_{DS}



(a)



(b)

Figure 11. Active switch version of the bridgeless totem-pole PFC at low line, 3.5kW at high line
(a) CH1: i_{IN}=10A/div, CH4: V_{GS} of Q2=5V/div and (b) V_{DS} of Q2=100V/div

Figure 12 shows the turn-on and turn-off V_{GS} at I_L=23A. There is no voltage overshoot at turn-on and the turn-off voltage bump is caused by the R_G. A detailed description of the driver can be found in application note AN0004: Designing Hard-switched Bridges with GaN.

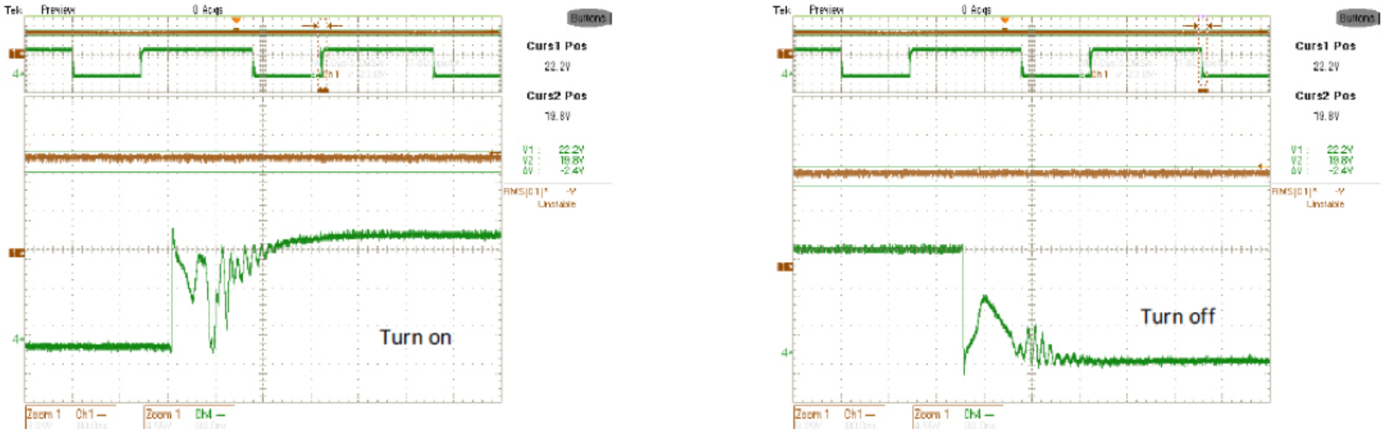


Figure 12. Waveforms of V_{GS} of Q2 at I_L=23A
CH1: I_{IN}=10A/div and CH4: V_{GS} of Q2=5V/div

Figure 13 shows the V_{DS} of Q2 at 3.5kW and a voltage spike of 56V at I_L=20A. In this circuit, the RC snubber and R_G help reduce voltage spikes.

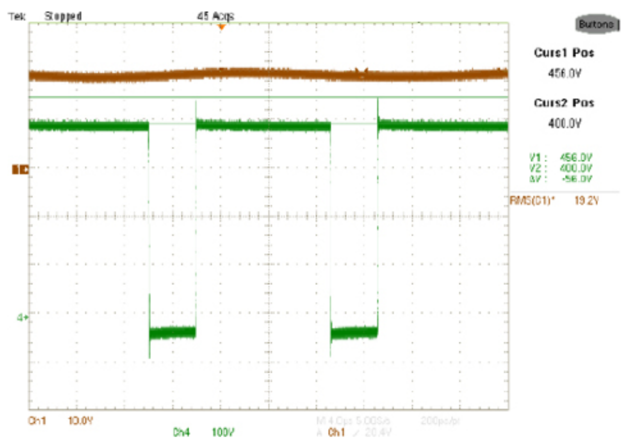
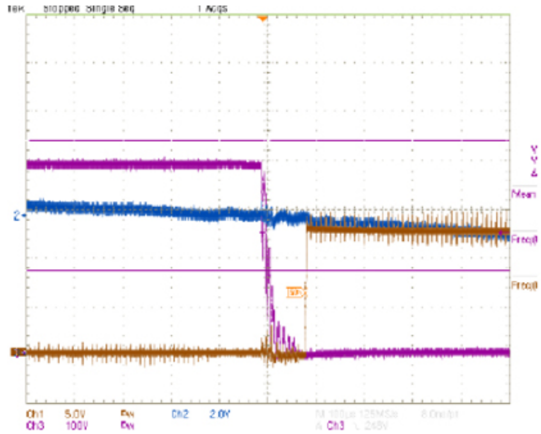
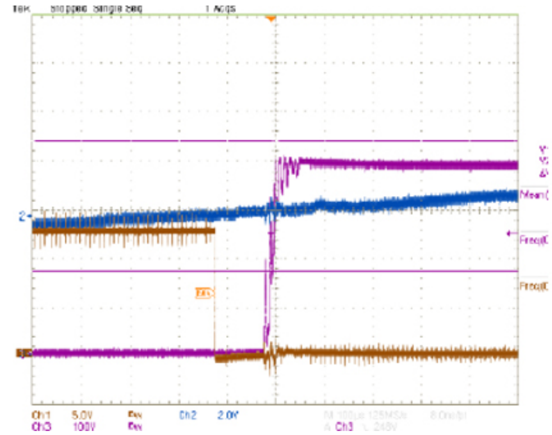


Figure 13. Waveforms of V_{DS} of Q2 at I_L=20A
CH1: I_{IN}=10A/div and CH4: V_{DS}=100V/div

Figure 14 shows the transition between two half-cycles. In Figure 13(a) the AC line enters the negative half and soft-start gradually increases voltage V_D from 0V to 385V, and in Figure13(b), V_D decreases from 385V to 0V.



(a)



(b)

Figure 14. Zero-crossing transitional waveforms (a) from negative to positive half-cycle and (b) from positive to negative half-cycle CH1: PW< gate signal for S_{D2}, CH2: I_L and CH3: V_D

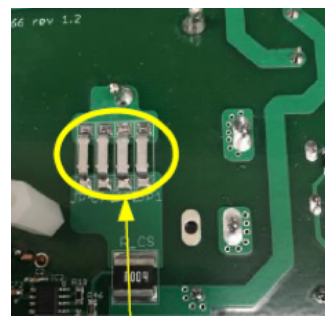
Probing

As shown in Figure 15, on the evaluation board there are four probing sockets for measuring V_{GS} and V_{DS} of low side GaN FET and MOSFET. By removing the jumpers and using a short wire to clamp the current prove, the PFC inductor can also be measured.

Probing tips: Low side GaN FET V_{GS} and V_{DS}

Probing tips: Low side MOSFET V_{GS} and V_{DS}

Passive voltage probes



Remove jumpers and add a cable for inductor current measurement

Figure 7. V_{GS} and V_{DS} of low side GaN FET and MOSFET measurement socket tips and current measuring position

Efficiency sweep and EMI

For the efficiency measurement, the input/output voltage and current will be measured for the input/output power calculation with a power analyzer. Efficiency has been measured at $120V_{AC}$ or $230V_{AC}$ input and $400V_{DC}$ output using the WT1800 precision power analyzer from Yokogawa. The efficiency and power loss results for the TDTTP4000W066B are shown in Figure 16. The extremely high efficiency of 99% at $230V_{AC}$ input, and >98% at 115V AC input is the highest among PFC designs with similar PWM frequency, enabling customers to reach peak system efficiency that meets or exceeds the 80 PLUS standard.

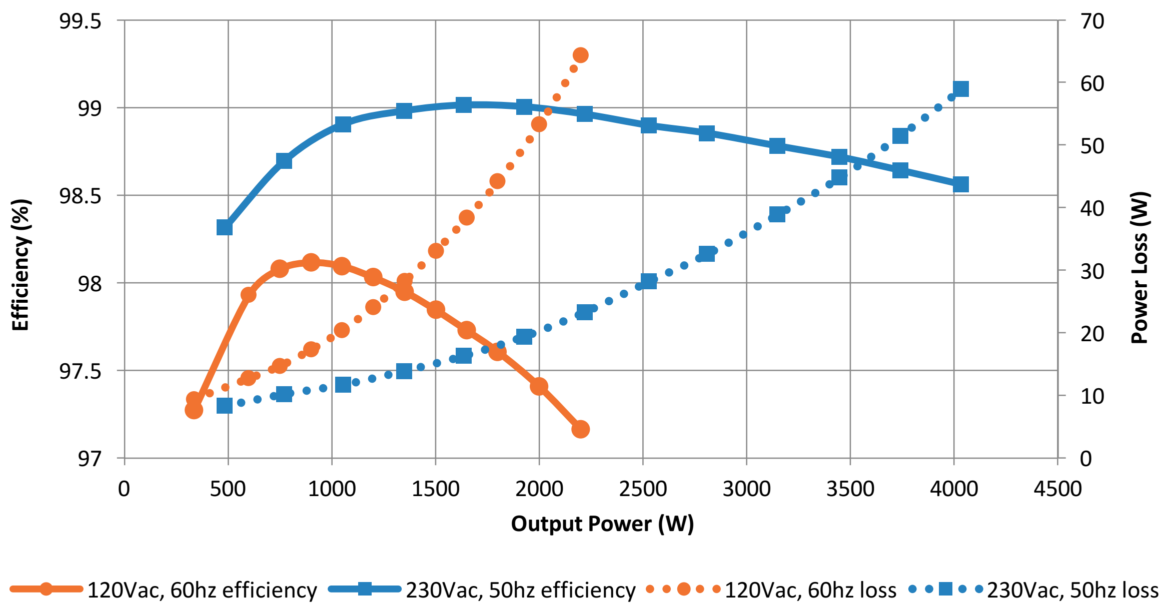


Figure 8. TDTTP4000W066B efficiency results

Conducted emissions have also been measured for this board using an LIN-115A LISN by Com-Power. The results compared to EN55022A limits are shown in Figure 17. **Note that the EMI test was done by using the lab-use power supply for an auxiliary 12V source. Do not use wall AC-DC adaptor for EMI test.**

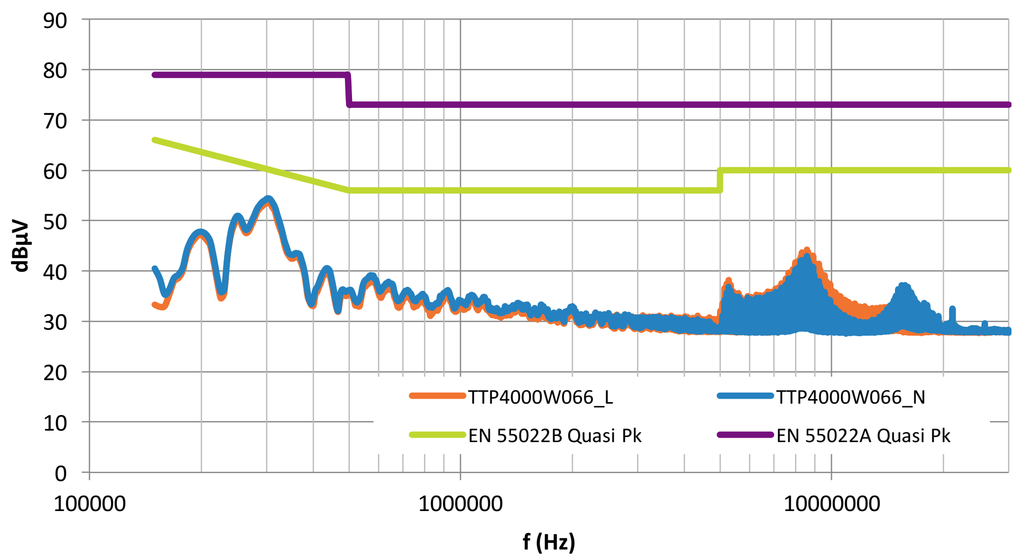


Figure 9. Conducted emissions @ 115V, 1150W

The THDi is measured using the WT1800 power analyzer at the condition of input THDv 3.8%, and as shown in Figure 18, it meets the standard of IEC61000-3-12.

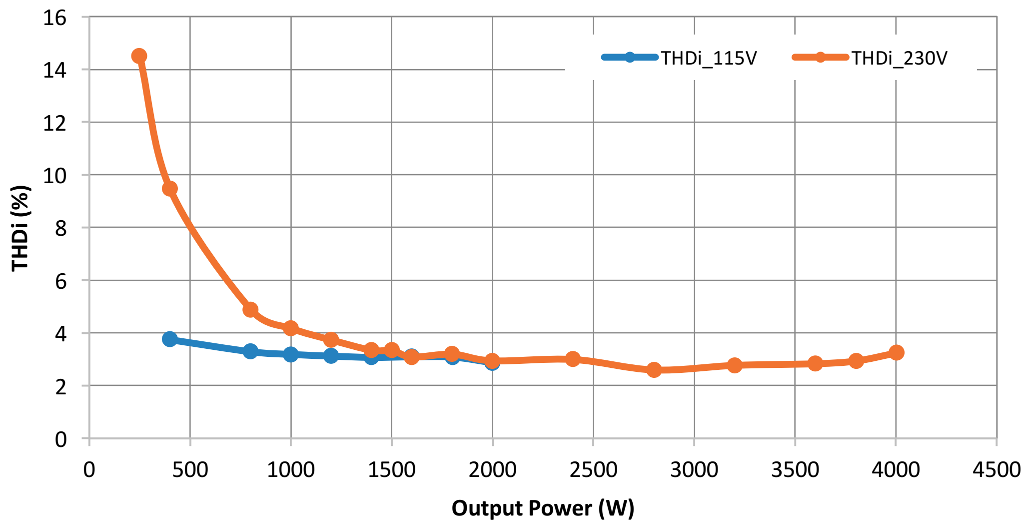


Figure 10. THDi measurements meet IEC61000-3-12 (>16A)

Maximum load limit

The TDTTP4000W066B evaluation board can run overload in a short time. The rated input current for <230V_{AC} input is 18A and the 10% overload current can be 19.8A. The input over-current protection (OCP) will be triggered when the current is over 21A.

Warnings

The TDTTP4000W066B is for evaluation purposes only and is not intended to be a finished product and does not include all protection features found in commercial power supplies. Additional warnings to keep in mind:

1. An isolated AC source should be used as input. An isolated lab bench-grade power supply or the included AUX DC supply should also be used for the 12V DC power supply. Float the oscilloscope by using an isolated oscilloscope or by disabling the PE (Protective Earth) pin in the power plug. Float the current probe power supply (if any) by disabling the PE pin in the power plug.
2. Use a resistive load only. The totem-pole PFC kit can work at zero load with burst mode and the output voltage will be swinging between 375V and 385V during burst mode.
3. The evaluation board is not fully-tested at large load steps. **DO NOT** apply a very large step in the load (>2000W) when it is running.
4. **DO NOT** manually probe the waveforms when the board is running. Set up probing before powering up the demo board.
5. The auxiliary V_{DC} supply must be 12V. The evaluation board will not work under 10V or over 15V V_{DC}, for example.
6. **DO NOT** touch any part of the evaluation board when it is running.
7. When plugging the control cards into the socket, make sure the control cards are fully pushed down with a clicking sound.
8. If the evaluation circuit goes into protection mode it will work as a diode bridge by shutting down all PWM functions. Recycle the bias power supply to reset the DSP and exit protection mode.
9. **DO NOT** use a passive probe to measure control circuit signals and power circuit signals at the same time. GND1 and AGND are not the same ground.
10. To get clean V_{GS} of the low side GaN FET, it is not recommended to measure the V_{DS} at the same time.
11. It is not recommended to use a passive voltage probe for V_{DS} and V_{GS} measurements while simultaneously using a differential voltage probe for V_{IN} measurements, unless the differential probe has very good dv/dt immunity.

References

[1] Z. Liang, U. Mishra and Y. Wu, "True Bridge-less Totem-pole PFC based on GaN FETs," in *PCIM*, Europe, pp. 1017-1022, May 2013.

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