



TE0701 TRM

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1 Table of Contents

| | | |
|-----|--|----|
| 1 | Table of Contents | 2 |
| 2 | Table of Figures | 4 |
| 3 | Table of Tables | 5 |
| 4 | Overview | 6 |
| 4.1 | Key Features | 6 |
| 4.2 | Block Diagram | 6 |
| 4.3 | Main Components | 8 |
| 4.4 | Initial Delivery State | 9 |
| 4.5 | Control Signals | 9 |
| 5 | Signals, Interfaces and Pins | 11 |
| 5.1 | FMC LPC Connector | 11 |
| 5.2 | ARM JTAG Connector | 12 |
| 5.3 | Mini-USB2 B Connector | 13 |
| 5.4 | Micro-USB2 Connector | 13 |
| 5.5 | MMC/SD-Card Socket | 14 |
| 5.6 | RJ45 - Ethernet | 15 |
| 5.7 | Mini CameraLink Connector | 16 |
| 5.8 | HDMI Connector | 16 |
| 5.9 | Pmod Connectors | 17 |
| 6 | On-board Peripherals | 21 |
| 6.1 | System Controller CPLD | 21 |
| 6.2 | FTDI FT2232H | 25 |
| 6.3 | SDIO Port Expander | 26 |
| 6.4 | HDMI Transmitter and Protection Circuit | 28 |
| 6.5 | Configuration DIP-switches | 29 |
| 6.6 | Push Buttons | 31 |
| 6.7 | On-board LEDs | 31 |
| 6.8 | Oscillators | 32 |
| 7 | Power and Power-On Sequence | 33 |
| 7.1 | Power Consumption | 33 |
| 7.2 | Power Distribution Dependencies | 33 |
| 7.3 | Power-On Sequence | 34 |
| 7.4 | Configuring mounted SoM's PL bank VCCO FMC_VADJ | 34 |
| 7.5 | Configuring 12V Power Supply Pin on the CameraLink Connector | 35 |
| 7.6 | Summary of VCCIO configuration via jumpers | 35 |

| | | |
|------|--|----|
| 7.7 | Power Rails | 38 |
| 8 | Board to Board Connectors | 42 |
| 8.1 | Connector Mating height | 42 |
| 8.2 | Connector Speed Ratings | 43 |
| 8.3 | Current Rating | 43 |
| 8.4 | Connector Mechanical Ratings | 43 |
| 9 | Technical Specifications | 44 |
| 9.1 | Absolute Maximum Ratings | 44 |
| 9.2 | Recommended Operating Conditions | 44 |
| 9.3 | Physical Dimensions | 45 |
| 10 | Variants Currently In Production | 46 |
| 11 | Revision History | 47 |
| 11.1 | Hardware Revision History | 47 |
| 11.2 | Document Change History | 48 |
| 12 | Disclaimer | 50 |
| 12.1 | Data Privacy | 50 |
| 12.2 | Document Warranty | 50 |
| 12.3 | Limitation of Liability | 50 |
| 12.4 | Copyright Notice | 50 |
| 12.5 | Technology Licenses | 50 |
| 12.6 | Environmental Protection | 50 |
| 12.7 | REACH, RoHS and WEEE | 50 |

2 Table of Figures

| | |
|---|----|
| Figure 1: TE0701-06 block diagram | 7 |
| Figure 2: TE0701-06 main components..... | 8 |
| Figure 3: JTAG/UART interface | 13 |
| Figure 4: TE0701 MicroUSB2 interface configuration..... | 14 |
| Figure 5: Power Distribution | 34 |
| Figure 6: Power Sequency..... | 35 |
| Figure 7: VCCIO jumper pin location (PCB-REV06), top view | 38 |
| Figure 8: Physical dimensions drawing..... | 46 |
| Figure 9: Hardware Revision Number | 48 |

3 Table of Tables

| | |
|---|----|
| Table 1: Initial delivery state of programmable devices on the board..... | 9 |
| Table 2: TE0701 Control Signals..... | 9 |
| Table 3: FMC connector J10 interface | 11 |
| Table 4: ARM JTAG connector signals and pins | 12 |
| Table 5: SD/MMC Card socket signals and pins | 14 |
| Table 6: RJ45 Ethernet MagJack signals and pins..... | 16 |
| Table 7: Mini CameraLink singals and pins..... | 17 |
| Table 8: HDMI connector signals and pins | 18 |
| Table 9: Pmod connectors pin description..... | 19 |
| Table 10: System Controller CPLD I/O pins..... | 21 |
| Table 11: FT2232H interface connections..... | 27 |
| Table 12: TI TXS02612 interface description..... | 28 |
| Table 13: HDMI transmitter signals and interface | 29 |
| Table 14: DIP-switches functionality description | 30 |
| Table 15: On-board Push Buttons | 32 |
| Table 16: On-board LEDs description | 31 |
| Table 17: On-board oscillators | 33 |
| Table 18: Configuring FMC_VADJ | 35 |
| Table 19: Baseboard supply-voltages VIOTA and VIOTB..... | 36 |
| Table 20: Configuration of baseboard supply-voltages via jumpers..... | 36 |
| Table 21: Power pin description of B2B Module Connector | 38 |
| Table 22: Power pin description of FMC connector..... | 39 |
| Table 23: Power pin description of Pmod connectors | 39 |
| Table 24: Power pin description of main power supply connectors | 39 |
| Table 25: Power pin description of peripherals' connectors..... | 39 |
| Table 26: Power Pin description of VCCIO selection jumpers..... | 40 |
| Table 27: Connectors. | 43 |
| Table 28: Speed rating. | 44 |
| Table 29: Module absolute maximum ratings | 45 |
| Table 30: Recommended Operating Conditions | 45 |
| Table 31: Trenz Electronic Shop Overview | 46 |
| Table 32: Hardware Revision History | 47 |
| Table 33: Document change history | 48 |

4 Overview

The Trenz Electronic TE0701 Carrier Board is a baseboard for 4 x 5 SoMs, which exposes the module's B2B connector pins to accessible connectors and provides a whole range of on-board components to test and evaluate TE 4 x 5 SoMs.

See page "[4 x 5 cm carriers](#)¹" to get information about the SoMs supported by the TE0701 carrier board.

Refer to <http://trenz.org/te0701-info> for the current online version of this manual and other available documentation.

4.1 Key Features

- Barrel jack for 12V power supply
- Overvoltage-, undervoltage- and reversed- supply-voltage-protection
- System Controller CPLD Lattice MachXO2 1200HC
- ARM JTAG interface connector
- Mini Camera Link
- RJ45 Gigabit Ethernet MagJack
- Low pin count FPGA Mezzanine Card (FMC LPC) connector
- USB JTAG and UART interface (FTDI FT2232HQ) with Mini-USB connector
- ADV7511 HDMI transmitter with HDMI connector
- 8 x red user LEDs
- 2 x user push-button
- 2 x 4-bit DIP switch for baseboard configuration
- Pmod connectors
- Micro SD card socket
- Micro-USB interface (device, host or OTG modes)
- Trenz Electronic 4 x 5 modules high-speed connector strips (3x Samtec LSHM series connectors)

4.2 Block Diagram

¹ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers>

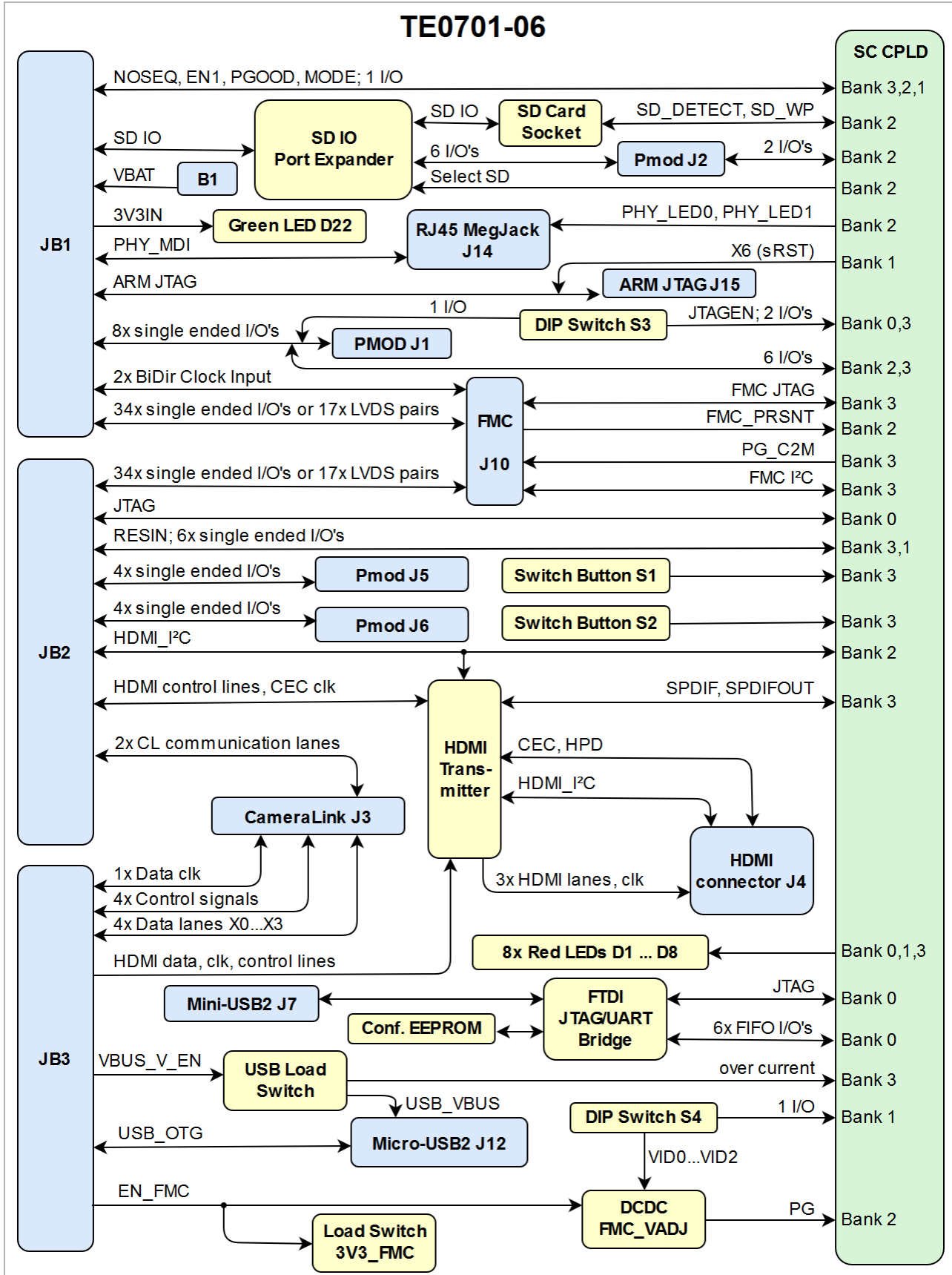


Figure 1: TE0701-06 block diagram

4.3 Main Components

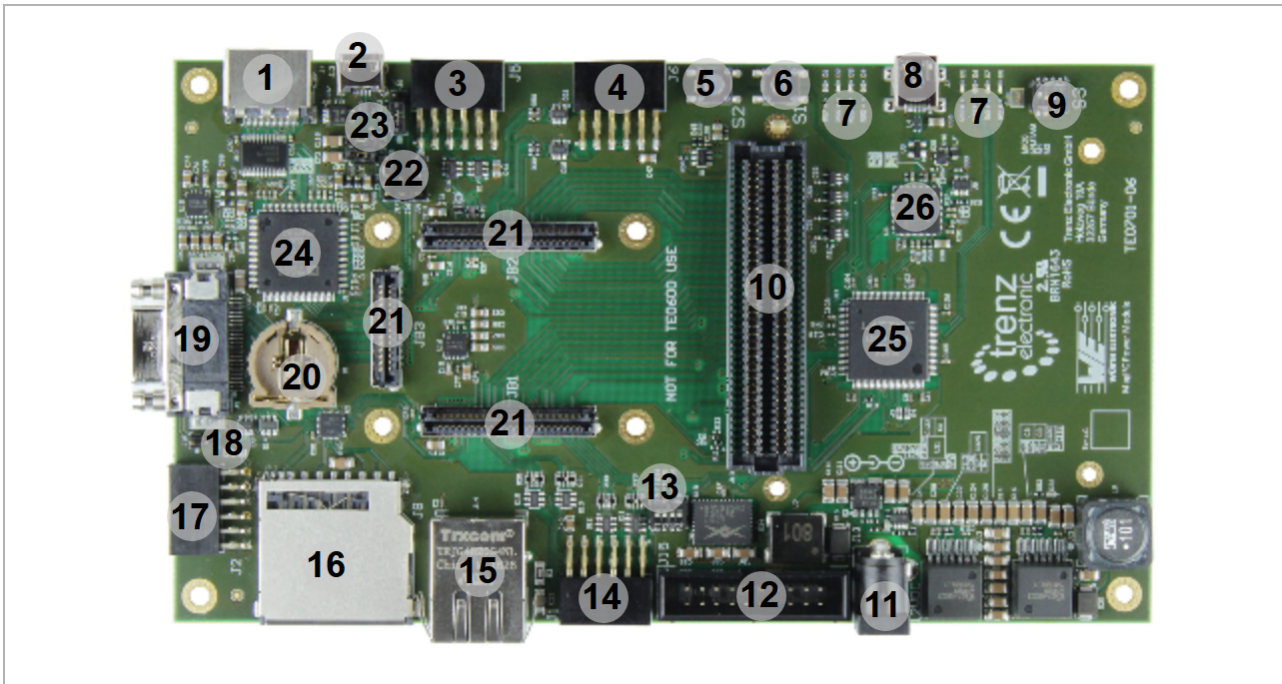


Figure 2: TE0701-06 main components

1. HDMI connector (1.4 HEAC support), J4
2. Micro-USB2 connector, J12
3. Pmod connector, J5
4. Pmod connector, J6
5. User push-button ("RESTART" button by default), S2
6. User push-button ("RESET" button by default), S1
7. 8x red user LEDs, D1 ... D8
8. Mini-USB2 connector, J7
9. User 4-bit DIP switch, S3
10. VITA 57.1 compliant LPC FMC connector, J10
11. Barrel jack for 12V power supply, J13
12. ARM JTAG connector (DS-5 D-Stream), J15, functionality depends on module
13. User 4-bit DIP switch, S4
14. Pmod connector, J1
15. RJ45 Gigabit Ethernet connector, J14
16. SD Card connector, J8
17. Pmod connector, J2
18. Jumper, J18
19. Mini CameraLink connector, J3
20. CR1220 Backup-Battery holder, B1
21. Trenez Electronic 4 x 5 modules B2B connectors, JB1 ... JB3
22. Jumper J16, J17, J21
23. Jumper J9, J19, J20
24. Analog Devices ADV7511 HDMI Transmitter, U1
25. Lattice Semiconductor MachXO2 1200 HC System Controller CPLD, U14
26. FTDI FT2232H USB2 to JTAG/UART Bridge, U3

4.4 Initial Delivery State

| Storage device name | Content | Notes |
|--|------------------|--|
| FTDI chip configuration EEPROM U9 (STM93C66) | Xilinx License | Do not overwrite, see warning in related section |
| System Controller CPLD U14 | SC CPLD Firmware | - |

Table 1: Initial delivery state of programmable devices on the board

4.5 Control Signals

To get started with TE0701 board, some basic control signals are essential and are described in the following table:

| Control signal | Switch / Button / LED / Pin | Signal Schematic Names | Connecte d to | Functionality | Notes |
|---------------------|-----------------------------|------------------------|---------------------|--|--|
| SC CPLD JTAG Enable | DIP switch S3-3 | JTAGEN | SC CPLD U14, pin 82 | ON: SC CPLD JTAG enabled, OFF: FPGA JTAG enabled | - |
| BOOT MODE | SC CPLD U14, pin 27 | MODE | B2B JB1, pin 31 | Boot Mode for attached module (Flash or SD) | - |
| Module Reset | SC CPLD U14, pin 13 | RESIN | B2B JB2, pin 17 | Module Reset | - |
| Global Reset input | Push Button S2 | S2 | SC CPLD U14, pin 2 | Manual reset from user | - |
| SD Card detection | SD Slot J8, pin 10 | SD_DETECT | SC CPLD U14, pin 40 | Detection Signal for inserted SD Card | Boot mode is set to SD Boot, when SD Card is detected. |

| Control signal | Switch / Button / LED / Pin | Signal Schematic Names | Connected to | Functionality | Notes |
|---|-------------------------------|------------------------|--|--|---|
| Board status indicators | Red LEDs D1 ... D8 | ULED1 ... ULED8 | SC CPLD U14, pins 78, 77, 76, 16, 69, 68, 65, 64 | indicating various board and module status / configuration | Refer to the firmware documentation of the SC CPLD² U14 and to the subsection 'LEDs' in section 'On-board Peripherals' for more details and current functionality. |
| Board 3.3V power indicator | Green LED D22 | 3V3IN | B2B JB1, pin 14, 16 | ON: 3.3V on-board voltage available | - |
| FMC_VADJ voltage selection | DIP switches S4-1, S4-2, S4-3 | VID0 ... VID2 | SC CPLD U14, pins 34, 35, 38 | sets adjustable voltage for FMC connector | - |
| I ² C control / FMC_VADJ voltage selection | DIP switches S3-2, S3-1 | CM0, CM1 | SC CPLD U14, pins 99, 1 | enabling / disabling I ² C control of board functionalities, sets FMC_VADJ voltage (only 3 steps), available to user if FMC_VADJ set by DIP-switch S4 | Refer to the firmware documentation of the SC CPLD³ U14 and to the subsection 'DIP switches' in section 'On-board Peripherals' for current functionality and more details. |

Table 2: TE0701 Control Signals

² <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

³ <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

5 Signals, Interfaces and Pins

5.1 FMC LPC Connector

I/O signals and interfaces connected to the FPGA SoCs I/O bank and FMC connector J10:

| FMC Connector J2 Pins and Interfaces | I/O Signal Count | LVDS-pairs count | Connecte d to | VCCIO voltage | Notes |
|--------------------------------------|------------------|------------------|--|---------------------|---|
| I/O | 34 | 17 | B2B JB1 connector | FMC_VAD J / 3V3_FMC | pins usable as single ended I/O's and LVDS pairs |
| | 34 | 17 | B2B JB2 connector | FMC_VAD J / 3V3_FMC | |
| I ² C | 2 | - | SC CPLD U14, pin 8, 10 | - | FMC I ² C Geographical Address pins GA0 and GA1 set to GND. |
| JTAG | 4 | - | SC CPLD U14, pin 4, 7, 9, 12 | 3.3V | - |
| Clock Input | - | 2 | B2B JB1 connector | - | 2x bidirectional reference clock inputs |
| Control Signals | 2 | - | SC CPLD U14, pin 20, 28 | - | 'PG_C2M', 'FMC_PRSENT' |
| Reference voltage (FMC_VREF) | 1 | - | B2B JB1 connector, pin 85, 97 B2B JB2 connector, pin 37, 93 | - | FMC sets thresholds of attached module's reference voltage (VREF pins). |

Table 3: FMC connector J10 interface

5.2 ARM JTAG Connector

The TE0701 baseboard offers the ARM JTAG 20-pin connector (2.54mm pitch). It can be used in standard JTAG or Serial Wire Debug (SWD) mode.

The following table contains the ARM JTAG connector pinout:

| Connector J15 pin | Schematic Name | Connected to | Notes |
|-------------------|----------------|-----------------|------------------------------|
| 1, VTREF | FMC_VADJ | DCDC U18 | Voltage Target Reference |
| 2, not connected | - | - | - |
| 3, NTRST | X0 | B2B JB1, pin 32 | active low Test Reset |
| 4, GND | - | - | - |
| 5, TDI | X1 | B2B JB1, pin 34 | Test Data In |
| 6, GND | - | - | - |
| 7, TMS / SWDIO | X2 | B2B JB1, pin 36 | Test Mode Select |
| 8, GND | - | - | - |
| 9, TCK / SWCLK | X3 | B2B JB1, pin 38 | Test Clock |
| 10, GND | - | - | - |
| 11, RTCK | X4 | B2B JB1, pin 42 | Return Test Clock |
| 12, GND | - | - | - |
| 13, TDO / SWO | X5 | B2B JB1, pin 44 | Test Data Out |
| 14, not connected | - | - | - |
| 15, sRST | X6 | B2B JB1, pin 99 | active low System Test Reset |
| 16, not connected | - | - | - |
| 17, not connected | - | - | - |
| 18, GND | - | - | - |

| Connector J15 pin | Schematic Name | Connected to | Notes |
|-------------------|----------------|--------------|-------|
| 19, not connected | - | - | - |
| 20, GND | - | - | - |

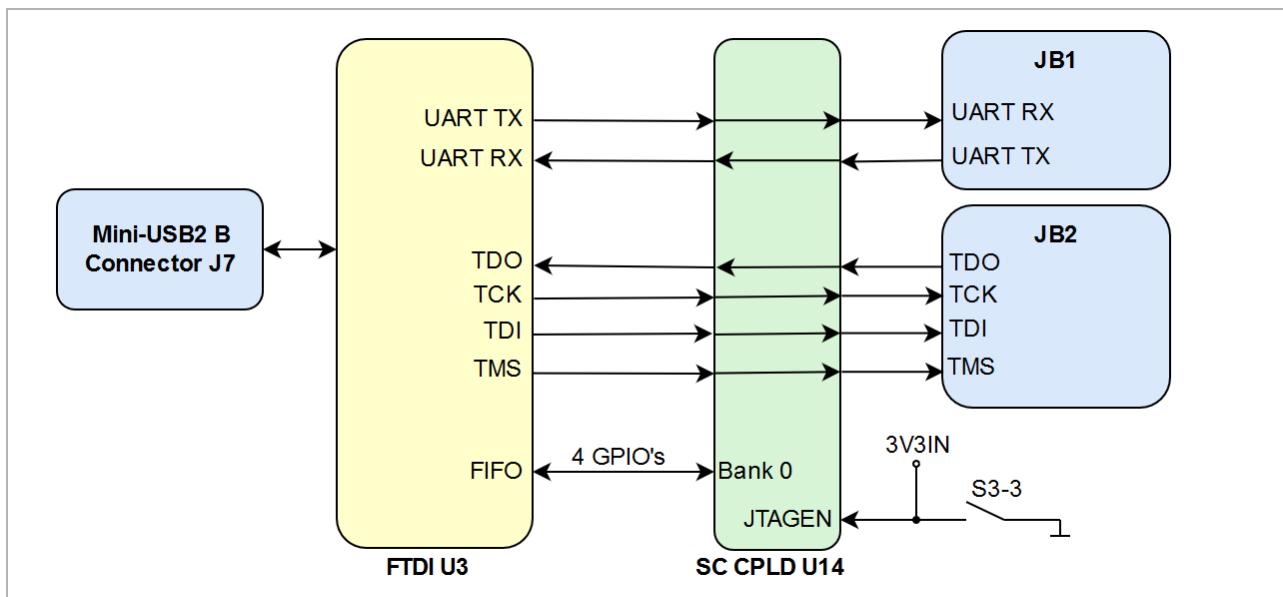
Table 4: ARM JTAG connector signals and pins

5.3 Mini-USB2 B Connector

Mini-USB2 interface provides access to UART and JTAG functions via FTDI FT2232 chip. The signals are forwarded to the B2B connectors via SC CPLD U14. 4 additional I/O's connected to the SC CPLD are available to the user.

JTAG access to the System Controller CPLD and attached module is provided via mini-USB JTAG interface J7 (FTDI FT2232H) and controlled by DIP switch S3-3.

The JTAG port of the System Controller CPLD is enabled by setting switch S3-3 JTAGEN to the OFF position.


Figure 3: JTAG/UART interface

5.4 Micro-USB2 Connector

The TE0701 carrier board can be configured as a USB host. Hence, it must provide from 5.25V to 4.75V to the board side of the downstream connection (micro-USB port on J12). To provide sufficient power, a TPS2051 power distribution switch is located on the carrier board in between the 5V power supply and the VBUS signal of the USB downstream port interface. If the output load exceeds the current-limit threshold, the TPS2051 limits the output current and pulls the over-current logic output (OC_n) low, which is routed to the on-board CPLD. The TPS2051 is put into operation by setting J19 CLOSED. J20 provides an extra 200µF decoupling capacitor (in addition to 10µF) to further stabilize the output signal. Moreover, a series terminating resistor of either 10K (J9: **1-2**, 3) or 1K (J9: 1, **2-3**) is selectable on the "USB-VBUS" signal. Both signals, USB-VBUS and VBUS_V_EN (that enables the TPS2051 on "high") are routed (as well as the corresponding D+/- data lines) via the on-board connector directly to the USB 2.0 high-speed transceiver PHY of the mounted SoM. In summary, the default jumper settings are the following: J9: **1-2**, 3 (10K series terminating resistor); J19: CLOSED (TPS2051 in operation); J20: CLOSED (200 µF added).

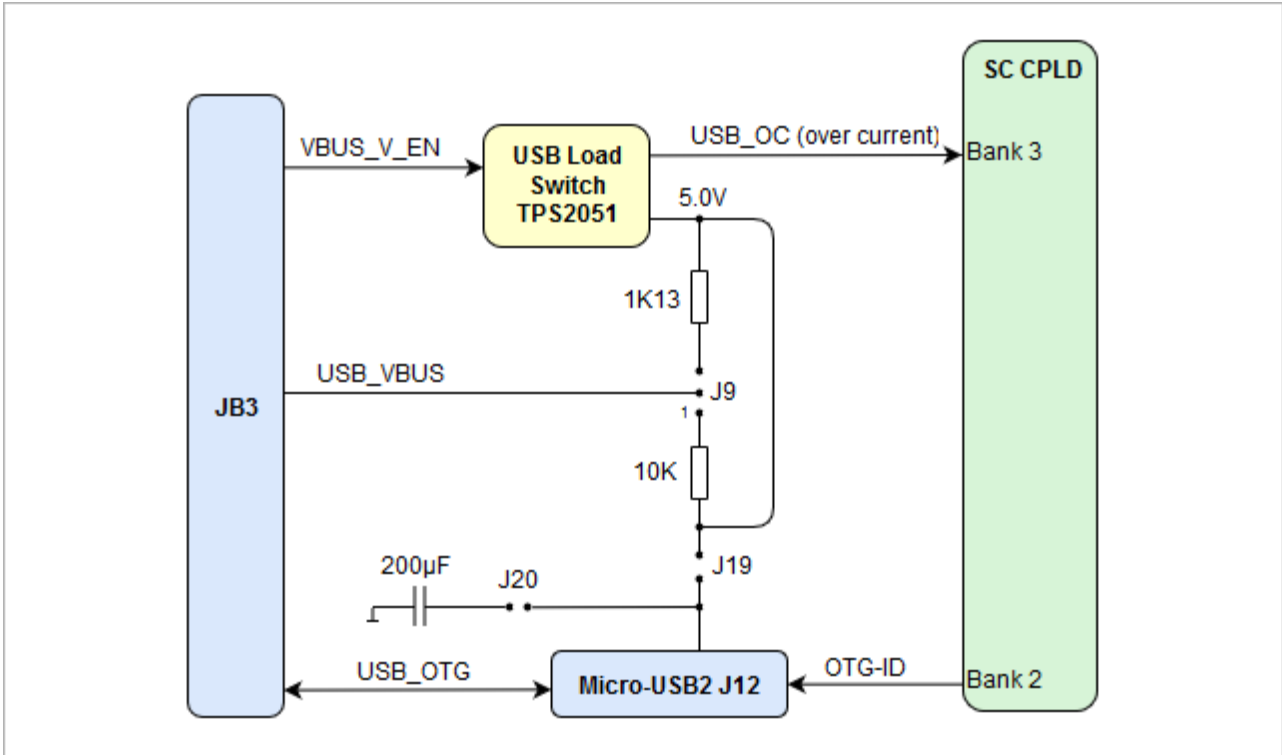


Figure 4: TE0701 MicroUSB2 interface configuration

5.5 MMC/SD-Card Socket

MMC/SD-Card socket is not directly wired to the B2B connector pins, but through a Texas Instruments TXS02612 SDIO Port Expander, which is needed for voltage translation due to different voltage levels of the Micro SD Card and MIO-bank of the Xilinx Zynq module. The Micro SD Card has 3.3V signal voltage level, but the MIO-bank on the Xilinx Zynq module has VCCIO of 1.8V.

With SD_SEL signal connected to the Texas Instruments TXS02612 SDIO Port Expander user can choose which port is accessible. Port B0 of SDIO Port Expander is connected to the Micro SD Card connector and B1 is connected to the Pmod J2 connector. SEL_SD signal can be controlled by the System Controller CPLD firmware.

| Connector J8 pin | Signal Schematic Name | Muxed to signal on Port Expander | Connected to | Notes |
|------------------|-----------------------|----------------------------------|-----------------|-------|
| 1, DAT3 | DAT3/CS | SD_DAT3 | B2B JB1, pin 18 | - |
| 2, CMD | CMD/MOSI | SD_CMD | B2B JB1, pin 26 | - |
| 5, CLK | S_CLK | SD_CLK | B2B JB1, pin 28 | - |
| 7, DAT0 | DAT0/MISO | SD_DAT0 | B2B JB1, pin 24 | - |

| Connector J8 pin | Signal Schematic Name | Muxed to signal on Port Expander | Connected to | Notes |
|------------------|-----------------------|----------------------------------|---------------------|---------------|
| 8, DAT1 | DAT1 | SD_DAT1 | B2B JB1, pin 22 | - |
| 9, DAT2 | DAT2 | SD_DAT2 | B2B JB1, pin 20 | - |
| 10, CD | SD_DETECT | - | SC CPLD U14, pin 40 | Card Detect |
| 11, WP | SD_WP | - | SC CPLD U14, pin 41 | Write Protect |

Table 5: SD/MMC Card socket signals and pins

5.6 RJ45 - Ethernet

The TE0701 Carrier Board has a RJ45 Gigabit Ethernet MagJack (J14) with two LEDs. On-board Ethernet MagJack J14 pins are routed to B2B connector JB1 via MDI. The center tap of the magnetics is not connected to module's B2B connector. PHY LEDs are not connected directly to the module's B2B connectors as the 4 x 5 module have no dedicated PHY LED pins assigned. PHY LEDs are connected to the TE0701 System Controller CPLD and can be routed to some of the module's I/O pins with firmware.

See documentation of the [TE0701 System Controller CPLD⁴](#) to get information of the function of the PHY LEDs.

| RJ45 MagJack J14 pin | Signal Schematic Name | Connected to | Notes |
|----------------------|-----------------------|---------------------|--------|
| LED1 | PHY_LED1 | SC CPLD U14, pin 42 | Yellow |
| LED2 | PHY_LED2 | SC CPLD U14, pin 43 | Green |
| PHY_MDI | PHY_MDI0_P | B2B JB1, pin 3 | - |
| | PHY_MDI0_N | B2B JB1, pin 5 | - |
| | PHY_MDI1_P | B2B JB1, pin 9 | - |
| | PHY_MDI1_N | B2B JB1, pin 11 | - |
| | PHY_MDI2_P | B2B JB1, pin 15 | - |
| | PHY_MDI2_N | B2B JB1, pin 17 | - |
| | PHY_MDI3_P | B2B JB1, pin 21 | - |

⁴ <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

| RJ45 MagJack J14 pin | Signal Schematic Name | Connected to | Notes |
|----------------------|-----------------------|-----------------|-------|
| | PHY_MDI3_N | B2B JB1, pin 23 | - |

Table 6: RJ45 Ethernet MagJack signals and pins

5.7 Mini CameraLink Connector

The TE0701 board provides the high speed CameraLink interface for visual input. The CameraLink is connected with 11 LVDS-pairs to the B2B connectors JB2 and JB3 which create data receive and control lanes.

| CameraLink J3 pin | Signal Schematic Name | Connected to | Notes |
|-------------------|-----------------------|--------------------------------|---------------------------------------|
| Pin 20, 7 | CL_TC_P / CL_TC_N | B2B JB2, Pin 12, 14 | Communication lanes |
| Pin 6, 19 | CL_TFG_P / CL_TFG_N | B2B JB2, Pin 16, 18 | |
| Pin 9, 22 | CL_CLK_P / CL_CLK_N | B2B JB3, Pin 31, 33 | Data clock |
| Pin 18, 5 | CL_CC1_P / CL_CC1_N | B2B JB3, Pin 26, 28 | Control lanes |
| Pin 17, 4 | CL_CC2_P / CL_CC2_N | B2B JB3, Pin 20, 22 | |
| Pin 16, 3 | CL_CC3_P / CL_CC3_N | B2B JB3, Pin 14, 16 | |
| Pin 15, 2 | CL_CC4_P / CL_CC4_N | B2B JB3, Pin 8, 10 | |
| Pin 12, 25 | CL_X0_P / CL_X0_N | B2B JB3, Pin 25, 27 | Data lanes |
| Pin 11, 24 | CL_X1_P / CL_X1_N | B2B JB3, Pin 19, 21 | |
| Pin 10, 23 | CL_X2_P / CL_X2_N | B2B JB3, Pin 13, 15 | |
| Pin 8, 21 | CL_X3_P / CL_X3_N | B2B JB3, Pin 7, 9 | |
| Pin 1, 23 | 12V0_CL | 12V Main Power supply (12V_LC) | filtered and protected supply voltage |

Table 7: Mini CameraLink signals and pins

5.8 HDMI Connector

The TE0701 board provides a HDMI interface routed to the B2B connectors of the the Zynq module. The HDMI interface is created by the HDMI transmitter ADV7511 provided by Analog Devices. The HDMI transmitter is incorporated in conjunction with the HDMI protection circuit TI TPD12S016 for more signal robustness.

| HDMI connector J4 pin | Signal Schematic Name | Connected to | Notes |
|-----------------------|----------------------------|---------------------------------|---|
| Pin 1, 3 | HDMI_TX2_P / HDMI_TX2_N | HDMI transmitter, Pin 43, 42 | also connected to HDMI protection circuit |
| Pin 4, 6 | HDMI_TX1_P / HDMI_TX1_N | HDMI transmitter, Pin 40, 29 | also connected to HDMI protection circuit |
| Pin 7, 9 | HDMI_TX0_P / HDMI_TX0_N | HDMI transmitter, Pin 36, 35 | also connected to HDMI protection circuit |
| Pin 10, 12 | HDMI_TXC_P / HDMI_TXC_N | HDMI transmitter, Pin 33, 32 | also connected to HDMI protection circuit |
| Pin 13 | CEC_B | HDMI transmitter, Pin 48 | HDMI CEC, wired through HDMI protection circuit |
| Pin 15 | SCL_B | HDMI transmitter, Pin 53 | HDMI I ² C clock line, wired through HDMI protection circuit |
| Pin 16 | SDA_B | HDMI transmitter, Pin 54 | HDMI I ² C data line, wired through HDMI protection circuit |
| Pin 19 | HPD_B | HDMI transmitter, Pin 30 | Hot Plug Detect, wired through HDMI protection circuit |
| Pin 18 | 5V_HDMI | HDMI protection circuit, Pin 13 | 5V supply voltage, wired through HDMI protection circuit |

Table 8: HDMI connector signals and pins

5.9 Pmod Connectors

The TE0701 board offers 4 Pmod (2x6 pins, SMT, right angle) connectors which provides as a standard modular interface I/O pins and MGT lanes for use with extension modules.

The connectors support single ended and differential signaling as the I/O's are routed from the B2B connectors of the attached module as LVDS-pairs to the Pmod connectors.

Following table gives an overview of the Pmod connectors and the signals routed to the attached module and to the System Controller CPLD U14:

| Pmod connector J1 pin | Signal Schematic Name | Connected to | Notes |
|------------------------------|------------------------------|---|---|
| 1 | MIO0 | B2B connector JB1, pin 88; DIP switch S3-4 | - |
| 2 | MIO9 | B2B connector JB1, pin 92 | - |
| 3 | MIO14 | B2B connector JB1, pin 91; SC CPLD U14, pin 37 | - |
| 4 | MIO15 | B2B connector JB1, pin 86; SC CPLD U14, pin 18 | - |
| 7 | MIO13 | B2B connector JB1, pin 98; SC CPLD U14, pin 30 | - |
| 8 | MIO10 | B2B connector JB1, pin 96; SC CPLD U14, pin 29 | - |
| 9 | MIO11 | B2B connector JB1, pin 94; SC CPLD U14, pin 19 | - |
| 10 | MIO12 | B2B connector JB1, pin 100; SC CPLD U14, pin 36 | - |
| Pmod connector J2 pin | Signal Schematic Name | Connected to | Notes |
| 1 | PX3 | SDIO Port Expander U2, pin 10 | muxed to signal 'SD_DAT3' (B2B JB1, pin 18) |
| 2 | PX4 | SDIO Port Expander U2, pin 12 | muxed to signal 'SD_CMD' (B2B JB1, pin 26) |
| 3 | PX0 | SDIO Port Expander U2, pin 14 | muxed to signal 'SD_DAT0' (B2B JB1, pin 24) |
| 4 | PX5 | SDIO Port Expander U2, pin 13 | muxed to signal 'SD_CLK' (B2B JB1, pin 28) |

| 7 | PX1 | SDIO Port Expander U2, pin 15 | muxed to signal 'SD_DAT1' (B2B JB1, pin 22) |
|------------------------------|------------------------------|-------------------------------|---|
| 8 | PX2 | SDIO Port Expander U2, pin 8 | muxed to signal 'SD_DAT2' (B2B JB1, pin 20) |
| 9 | PX6 | SC CPLD U14, pin 49 | - |
| 10 | PX7 | SC CPLD U14, pin 48 | - |
| Pmod connector J5 pin | Signal Schematic Name | Connected to | Notes |
| 1 | PA1_P | B2B connector JB2, pin 27 | usable as LVDS pair |
| 2 | PA1_N | B2B connector JB2, pin 25 | |
| 3 | PA2_P | B2B connector JB2, pin 26 | usable as LVDS pair |
| 4 | PA2_N | B2B connector JB2, pin 28 | |
| 7 | PA0_P | B2B connector JB2, pin 23 | usable as LVDS pair |
| 8 | PA0_N | B2B connector JB2, pin 21 | |
| 9 | PA3_P | B2B connector JB2, pin 22 | usable as LVDS pair |
| 10 | PA3_N | B2B connector JB2, pin 24 | |
| Pmod connector J6 pin | Signal Schematic Name | Connected to | Notes |
| 1 | PB2_N | B2B connector JB2, pin 51 | usable as LVDS pair |
| 2 | PB2_P | B2B connector JB2, pin 53 | |
| 3 | PB0_N | B2B connector JB2, pin 33 | usable as LVDS pair |
| 4 | PB0_P | B2B connector JB2, pin 31 | |
| 7 | PB3_N | B2B connector JB2, pin 47 | usable as LVDS pair |
| 8 | PB3_P | B2B connector JB2, pin 45 | |

| | | | |
|----|-------|---------------------------|---------------------|
| 9 | PB1_N | B2B connector JB2, pin 43 | usable as LVDS pair |
| 10 | PB1_P | B2B connector JB2, pin 41 | |

Table 9: Pmod connectors pin description

i J5 and J6 are incompatible with dual PMODs, because they have different PMOD connector offset and variable (different) VCCIO voltage.

6 On-board Peripherals

6.1 System Controller CPLD

The System Controller CPLD (U14) is provided by Lattice Semiconductor LCMXO2-1200HC (MachXO2 Product Family). The SC-CPLD is the central system management unit where essential control signals are logically linked by the implemented logic in CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG / UART and I²C between the on-board peripherals and the attached module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and the programming state of the attached module.

For detailed information, refer to [the firmware documentation of the SC CPLD](#)⁵. Table below lists the SC CPLD I/O signals and pins:

| SC CPLD U14 Pins and Interfaces | Connected to | Function | Notes |
|---------------------------------|---------------------------|--|-------|
| FMC_TMS | FMC J10, pin D31 | FMC JTAG | - |
| FMC_TDI | FMC J10, pin D29 | | |
| FMC_TDO | FMC J10, pin D30 | | |
| FMC_TCK | FMC J10, pin D33 | | |
| FMC_SDA | FMC J10, pin C31 | FMC I ² C | - |
| FMC_SCL | FMC J10, pin C30 | | |
| PG_C2M | FMC J10, pin D1 | FMC control signals | - |
| FMC_PRSENT | FMC J10, pin H2 | | |
| EN_FMC | DC-DC U18, Load switch Q1 | FMC power control signals | - |
| POK_FMC | DC-DC U18 | | |
| S1 | Pushbutton S1 | available to user | - |
| S2 | Pushbutton S2 | Global Reset in standard configuration | - |

⁵ <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

| SC CPLD U14 Pins and Interfaces | Connected to | Function | Notes |
|---------------------------------|----------------------------|---|--|
| M_TDO | FTDI chip, pin 14 (ADBUS2) | SC CPLD JTAG interface activated if DIP switch S3-3 in OFF-position. Attached module JTAG interface activated if DIP switch S3-3 in ON-position. | - |
| M_TDI | FTDI chip, pin 13 (ADBUS1) | | |
| M_TCK | FTDI chip, pin 12 (ADBUS0) | | |
| M_TMS | FTDI chip, pin 15 (ADBUS3) | | |
| JTAGEN | DIP switch S3-3 | | |
| C_TMS | B2B JB2, pin 94 | Forwarded JTAG signals from FTDI chip, if DIP switch S3-3 in ON-position. | JTAG signals buffered with ICs U4, U6,U7, U8 |
| C_TCK | B2B JB2, pin 100 | | |
| C_TDO | B2B JB2, pin 98 | | |
| C_TDI | B2B JB2, pin 96 | | |
| ADBUS4 | FTDI chip, pin 17 | FIFO / GPIO's available to user | - |
| ADBUS7 | FTDI chip, pin 20 | | |
| ACBUS4 | FTDI chip, pin 26 | | |
| ACBUS5 | FTDI chip, pin 27 | | |
| BDBUS0 | FTDI chip, pin 32 | UART TX from FTDI (forwarded to MIO14) | UART signals connected to attached module |
| BDBUS1 | FTDI chip, pin 33 | UART RX to FTDI (forwarded from MIO15) | |
| EN1 | B2B JB1, pin 27 | SoM control signals, functionalities depend also on attached SoM's SC CPLD firmware. | - |
| NOSEQ | B2B JB1, pin 8 | | |
| PGOOD | B2B JB1, pin 29 | | |
| RESIN | B2B JB2, pin 17 | | |
| MODE | B2B JB1, pin 31 | | |

| SC CPLD U14 Pins and Interfaces | Connected to | Function | Notes |
|---------------------------------|---|--|-------|
| ULED1 | Red LED D1 | USER LEDs, refer to the current firmware documentation of the SC CPLD ⁶ . | - |
| ULED2 | Red LED D2 | | |
| ULED3 | Red LED D3 | | |
| ULED4 | Red LED D4 | | |
| ULED5 | Red LED D5 | | |
| ULED6 | Red LED D6 | | |
| ULED7 | Red LED D7 | | |
| ULED8 | Red LED D8 | | |
| Y0 | B2B JB2, pin 42 | User I/O's between SC CPLD U14 and attached module | - |
| Y1 | B2B JB2, pin 44 | | |
| Y2 | B2B JB2, pin 90 | | |
| Y3 | B2B JB2, pin 91 | | |
| Y4 | B2B JB2, pin 99 | | |
| Y5 | B2B JB2, pin 35 | | |
| Y6 | B2B JB1, pin 87 | | |
| X6 | B2B JB1, pin 99; ARM JTAG J15, pin 15 | ARM JTAG sRST (active low System Test Reset) | - |
| PHY_LED1 | RJ45 connector J14 | Current indicating function depends on SC CPLD firmware. | - |
| PHY_LED2 | | | |
| SEL_SD | SDIO port expander U2 | Control signal to select Port B0 or B1. | - |
| SD_DETECT | SD/MMC Card socket J8, pin 10 | Card Detect signal | - |

⁶ <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

| SC CPLD U14 Pins and Interfaces | Connected to | Function | Notes |
|---------------------------------|------------------------------------|---|--|
| SD_WP | SD/MMC Card socket J8, pin 11 | Write Protect signal | |
| HDMI_SCL | HDMI Transmitter U1, pin 55 | HDMI transmitter 2-wire serial bus | - |
| HDMI_SDA | HDMI Transmitter U1, pin 56 | | |
| HDMI_SPDIFOUT | HDMI Transmitter U1, pin 46 | Unidirectional HDMI S/PDIF lines | - |
| HDMI_SPDIF | HDMI Transmitter U1, pin 10 | | |
| CM0 | DIP switch S3-2 | Set FMC_VADJ "S3-1 S3-2: FMC_VADJ": OFF OFF : 1.8V OFF ON : 2.5V ON OFF : 2.2V ON ON : I2C control enabled | DIP switch S4-1, S4-2 and S4-3 have to be set to OFF if use DIP switches S3-1 and S3-2. |
| CM1 | DIP switch S3-1 | | |
| CM2 | DIP switch S4-4 | depends on current SC CPLD firmware | - |
| VID0 | DC-DC U18, pin 34; DIP switch S4-1 | set bit pattern as "VID2 VID1 VID0: FMC_VADJ": 0 0 0 : 3.3V 0 0 1 : 2.5V 0 1 0 : 1.8V 0 1 1 : 1.5V 1 0 0 : 1.25V 1 0 1 : 1.2V 1 1 0 : 0.8V (not supported as VCCIO standard) 1 1 1 : Reserved | SC CPLD settings will be overridden by DIP switch S4, if one of them is set to one (OFF-position). |
| VID1 | DC-DC U18, pin 33; DIP switch S4-2 | | |
| VID2 | DC-DC U18, pin 32; DIP switch S4-3 | | |
| USB_OC | USB-VBUS Load Switch U11, pin 5 | | |

| SC CPLD U14 Pins and Interfaces | Connected to | Function | Notes |
|---------------------------------|--------------------------------------|--|---|
| MIO10 | B2B JB1, pin 96; Pmod J1, pin 8 | User I/O's between SC CPLD U14, attached module and Pmod connector J1. | - |
| MIO11 | B2B JB1, pin 94; Pmod J1, pin 9 | | |
| MIO12 | B2B JB1, pin 100; Pmod J1, pin 10 | | |
| MIO13 | B2B JB1, pin 98; Pmod J1, pin 7 | | |
| MIO14 | B2B JB1, pin 91; Pmod J1, pin 3 | UART interface in standard SC CPLD firmware, else user I/O's. | |
| MIO15 | B2B JB1, pin 86; Pmod J1, pin 4 | | |
| PX6 | Pmod J2, pin 9 | User I/O's of SC CPLD U14 | - |
| PX7 | Pmod J2, pin 10 | | |
| VCCIO0 | 3V3IN | VCCIO SC CPLD bank 0 | - |
| VCCIO1 | VIOTB | VCCIO SC CPLD bank 1 | adjustable voltage, see section 'Power' |
| VCCIO2 | 3V3IN | VCCIO SC CPLD bank 2 | - |
| VCCIO3 | 3V3IN | VCCIO SC CPLD bank 3 | - |

Table 10: System Controller CPLD I/O pins

6.2 FTDI FT2232H

The TE0701 board is equipped with the FTDI FT2232H USB2 to JTAG/UART adapter controller connected to the Mini-USB2 B connector J7 to provide JTAG and UART access to the attached module or to the SC CPLD U14 (switchable over DIP switch S3-3).

There is also a 256-byte configuration EEPROM U9 (93AA56BT) wired to the FT2232H chip via Microwire bus which holds pre-programmed license code to support Xilinx programming tools. Refer to the FTDI datasheet to get information about the capacity of the FT2232H chip.

⚠ Do not access the FT2232H EEPROM using FTDI programming tools, doing so will erase normally invisible user EEPROM content and invalidate stored Xilinx JTAG license. Without this license the on-board JTAG will not be accessible any more with any Xilinx tools. Software tools from FTDI website do not warn or ask for confirmation before erasing user EEPROM content.

Channel A of the FTDI chip is configured as JTAG interface (MPSSE) connected to the SC CPLD U14, the JTAG signals are forwarded to the JTAG interface of the attached module if DIP switch S3-3 is in OFF-position.

Channel B can be used as UART interface routed to the SC CPLD U14 and is available for other user-specific purposes.

| FT2232H U3 Pin | Signal Schematic Name | Connected to | Notes |
|----------------|-----------------------|--------------------------------------|-----------------------------------|
| Pin 12, ADBUS0 | M_TCK | SC CPLD U14, pin 91 | JTAG interface |
| Pin 13, ADBUS1 | M_TDI | SC CPLD U14, pin 94 | |
| Pin 14, ADBUS2 | M_TDO | SC CPLD U14, pin 95 | |
| Pin 15, ADBUS3 | M_TMS | SC CPLD U14, pin 90 | |
| Pin 20, ADBUS7 | ADBUS7 | SC CPLD U14, pin 97 | UART and user configurable GPIO's |
| Pin 26, ACBUS4 | ACBUS4 | SC CPLD U14, pin 96 | |
| Pin 27, ACBUS5 | ACBUS5 | SC CPLD U14, pin 88 | |
| Pin 32, BDBUS0 | BDBUS0 | SC CPLD U14, pin 87 | |
| Pin 33, BDBUS1 | BDBUS1 | SC CPLD U14, pin 86 | |
| Pin 40, BDBUS7 | JTAGEN | DIP switch S3-3; SC CPLD U14, pin 82 | Control line |

Table 11: FT2232H interface connections

6.3 SDIO Port Expander

The TE0701 carrier board is equipped with the Texas Instruments TXS02612 SDIO Port Expander, which connected the SDIO port of the attached module either to the SD/MMC Card socket J8 or Pmod J1.

The SD IO port expander fullfills also a voltage translation between the ports A with bank voltage VCCO 'VIOB' and the ports B0 and B1 with VCCIO '3.3VOUT'.

| TI TXS02612 U2 Port A Pins and Signals | Connected to | TI TXS02612 U2 Port B0 and B1 Pins and Signals | Connected to | Notes |
|--|-----------------|--|-------------------------|--|
| Pin 6, 'SD_DAT0' | B2B JB1, pin 24 | Pin 18, 'DAT0/MISO', Port B0 | SD/MMC Socket J8, pin 7 | The SD IO port expander connects the signals of Port A to Port B0 or B1 depending on the state of the control line 'SEL_SD' (pin 24), connected to SC CPLD U14, pin 39. When 'SEL_SD' is low, port B0 is selected, when 'SEL_SD' is high, port B1 is selected. |
| | | Pin 14, 'PX0', Port B1 | Pmod J2, pin 3 | |
| Pin 7, 'SD_DAT1' | B2B JB1, pin 22 | Pin 16, 'DAT1', Port B0 | SD/MMC Socket J8, pin 8 | |
| | | Pin 15, 'PX1', Port B1 | Pmod J2, pin 7 | |
| Pin 1, 'SD_DAT2' | B2B JB1, pin 20 | Pin 23, 'DAT2', Port B0 | SD/MMC Socket J8, pin 9 | |
| | | Pin 8, 'PX2', Port B1 | Pmod J2, pin 8 | |
| Pin 3, 'SD_DAT3' | B2B JB1, pin 18 | Pin 22, 'DAT3/CS', Port B0 | SD/MMC Socket J8, pin 1 | |
| | | Pin 10, 'PX3', Port B1 | Pmod J2, pin 1 | |
| Pin 4, 'SD_CMD' | B2B JB1, pin 26 | Pin 20, 'CMD/MOSI', Port B0 | SD/MMC Socket J8, pin 2 | |
| | | Pin 12, 'PX4', Port B1 | Pmod J2, pin 2 | |
| Pin 9, 'SD_CLK' | B2B JB1, pin 28 | Pin 19, 'SCLK', Port B0 | SD/MMC Socket J8, pin 5 | |
| | | Pin 13, 'PX5', Port B1 | Pmod J2, pin 4 | |

Table 12: TI TXS02612 interface description

6.4 HDMI Transmitter and Protection Circuit

The TE0701 board is equipped with the HDMI transmitter chip ADV7511KSTZ U1 provided by Analog Devices. The HDMI transmitter chip is incorporated in conjunction with the HDMI protection circuit TPD12S016 by Texas Instruments.

Attached Zynq modules can output a HDMI video signal to the on-board HDMI connector J4 with CEC, S/PDIF, HPD and 2-wire serial bus functionalities.

Following pins and signals are assigned between the HDMI transmitter chip U1, the B2B connectors and the SC CPLD U14:

| AD ADV7511KSTZ U1 Pins and Signals | Connected to | Protection Circuit U10 | Notes |
|---|---------------------|------------------------|--------------------------------------|
| 'HDMI_D0' ... 'HDMI_D11', Pin 85 ... 96 | B2B JB3 | - | - |
| 'HDMI_TXC_N, HDMI_TXC_P, Pin 32, 33 | HDMI J4, pin 12, 10 | ESD protection | - |
| 'HDMI_TX0_N, HDMI_TX0_P, Pin 35, 36 | HDMI J4, pin 9, 7 | ESD protection | - |
| 'HDMI_TX1_N, HDMI_TX1_P, Pin 39, 40 | HDMI J4, pin 6, 4 | ESD protection | - |
| 'HDMI_TX2_N, HDMI_TX2_P, Pin 42, 43 | HDMI J4, pin 3, 1 | ESD protection | - |
| 'HDMI_VS', Pin 2 | B2B JB3, pin 60 | - | - |
| 'HDMI_HS', Pin 98 | B2B JB3, pin 58 | - | - |
| 'HDMI_CLK', Pin 79 | B2B JB3, pin 59 | - | - |
| 'HDMI_DE', Pin 97 | B2B JB3, pin 57 | - | - |
| 'HPD_A', Pin 30 | HDMI J4, pin 19 | signal pass-thru | level shifted signal ('HPD_B') to 5V |
| 'CEC_A', Pin 48 | HDMI J4, pin 13 | signal pass-thru | level shifted signal ('CEC_B') to 5V |
| 'CEC_CLK', Pin 50 | B2B JB2, pin 38 | - | - |

| | | | |
|--------------------------------------|--------------------------------------|------------------------------------|--|
| 'SCL_A', Pin 53 | HDMI J4, pin 15 | signal pass-thru | level shifted signal ('SCL_B') to 5V |
| 'SDA_A', Pin 54 | HDMI J4, pin 16 | signal pass-thru | level shifted signal ('SDA_B') to 5V |
| 'HDMI_SCL', Pin 55 | B2B JB2, pin 13, SC CPLD U14, pin 47 | - | I ² C bus lines also used for I2C control (if activated) of SC CPLD U14 functions |
| 'HDMI_SDA', Pin 56 | B2B JB2, pin 15; SC CPLD U14, pin 45 | - | |
| 'HDMI_INT', Pin 45 | B2B JB2, pin 32 | - | - |
| 'HDMI_SPDIF', Pin 10 | SC CPLD U14, pin 15 | - | - |
| 'HDMI_SPDIFOUT', Pin 46 | SC CPLD U14, pin 14 | - | - |
| TPD12S016 U10 Control Signals | Connected to | Functionality | Notes |
| LS_OE | B2B JB2, pin 36 | enable Level Shifter (1.8V ↔ 5.0V) | Both signals must be HIGH level for full functionality of HDMI Protection Circuit U10. |
| CT_HPDP | B2B JB2, pin 34 | enable Load Switch for HPD | |

Table 13: HDMI transmitter signals and interface

6.5 Configuration DIP-switches

There are two 4-bit DIP-switches S3 and S4 present on the TE0701 board to configure options and set parameters. The following table describes the functionalities of the particular switches.

| DIP-switch S3 | Signal Schematic Name | Connected to | Functionality | Notes |
|---------------|-----------------------|--------------|---------------|-------|
|---------------|-----------------------|--------------|---------------|-------|

| | | | | |
|-------------------------------|--------------------------------------|---------------------------------------|---|---|
| S3-1 | CM1 | SC CPLD U14, pin 1 | Set FMC_VADJ "S3-1 S3-2: FMC_VADJ": | DIP switch S4-1, S4-2 and S4-3 have to be set to OFF if use DIP switches S3-1 and S3-2. |
| S3-2 | CM0 | SC CPLD U14, pin 99 | OFF OFF : 1.8V OFF ON : 2.5V ON OFF : 2.2V ON ON : I2C control enable | |
| S3-3 | JTAGEN | SC CPLD U14, pin 82 | Positions: ON: enables JTAG interface of module OFF: enables JTAG interface of SC CPLD U14 | JTAG interface accessible through FTDI chip with Mini-USB2 B connector J7 |
| S3-4 | MIO0 | Pmod J1, pin 1; B2B JB1, pin 88 | depends on attached module | - |
| DIP- switch S4 | Signal Schematic Name | Connected to | Functionality | Notes |
| S4-1 | VID0 | SC CPLD U14, pin 34 | set 3bit code to adjust FMC_VADJ voltage | The FMC_VADJ voltage is provided by DCDC U8 EN5335QI, Set DIP-switches as bit pattern "S4-3 S4-2 S4-1: FMC_VADJ": ON ON ON : 3.3V ON ON OFF : 2.5V ON OFF ON : 1.8V ON OFF OFF : 1.5V OFF ON ON : 1.25V OFF ON OFF : 1.2V OFF OFF ON : 0.8V (not supported as VCCIO standard) OFF OFF OFF : activate I2C control of some SC CPLD functions |
| S4-2 | VID1 | SC CPLD U14, pin 35 | | |
| S4-3 | VID2 | SC CPLD U14, pin 38 | | |

| | | | | |
|------|-----|---------------------|-------------------------------------|---|
| S4-4 | CM2 | SC CPLD U14, pin 51 | depends on current SC CPLD firmware | - |
|------|-----|---------------------|-------------------------------------|---|

Table 14: DIP-switches functionality description

6.6 Push Buttons

There are two push buttons available to the user connected to the SC CPLD U14:

| Button | Connected to | Function | Notes |
|--------|--------------------|--|-------|
| S1 | SC CPLD U14, pin 3 | User button, function depends on SC CPLD firmware. | - |
| S2 | SC CPLD U14, pin 2 | Global Reset of attached module | - |

Table 15: On-board Push Buttons

Note: Functionality depends also on CPLD Firmware: [TE0701 CPLD](#)⁷

6.7 On-board LEDs

The TE0701 board is equipped with several LEDs to indicate states and activities.

| LED | Color | Connected to | Description and Notes |
|-----|-------|---------------------|--|
| D22 | green | 3.3VIN | indicates available 3.3V voltage level of attached module |
| D1 | red | SC CPLD U14, pin 78 | functionality depends on the current firmware of the SC CPLD, refer to the documentation. ⁸ |
| D2 | red | SC CPLD U14, pin 77 | |
| D3 | red | SC CPLD U14, pin 76 | |
| D4 | red | SC CPLD U14, pin 16 | |
| D5 | red | SC CPLD U14, pin 69 | |
| D6 | red | SC CPLD U14, pin 68 | |
| D7 | red | SC CPLD U14, pin 65 | |
| D8 | red | SC CPLD U14, pin 64 | |

Table 16: On-board LEDs description

⁷ <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

⁸ <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

6.8 Oscillators

The TE0701 board is equipped with one oscillator which provide reference clock signal to the FTDI chip:

| Clock Source | Signal Schematic Name | Frequency | Clock Input Destination |
|----------------------------------|------------------------------|------------------|-------------------------------------|
| SiTime SiT8008AI oscillator, U20 | OSCI | 12.000000 MHz | USB2 to JTAG/UART adapter U3, pin 3 |

Table 17: On-board oscillators

7 Power and Power-On Sequence

7.1 Power Consumption

Power supply with minimum current capability of 3A at 12V for system startup is recommended.

7.2 Power Distribution Dependencies

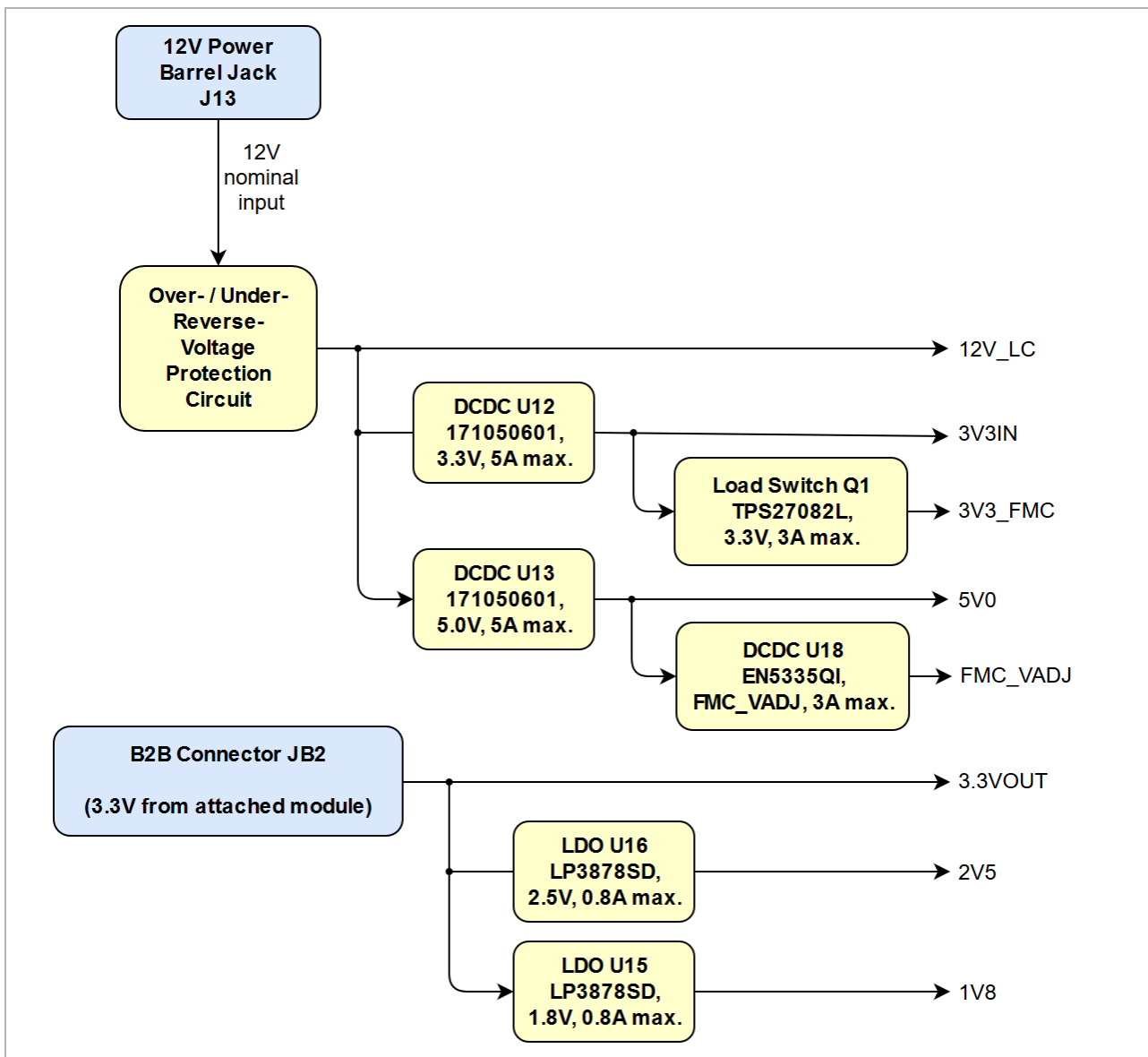


Figure 5: Power Distribution

7.3 Power-On Sequence

The on-board voltages 3.3V and 5.0V of the carrier board will be powered up simultaneously when 12V power supply is connected to the barrel jack J10.

The on-board voltages 1.8V and 2.5V will be enabled when module's 3.3V voltage level has become stable and 3.3VOUT is available on the B2B connector JB2 pins 9 and 11.

The PL IO-bank supply voltage FMC_VADJ will be available after the output of the 5.0V DC-DC converter is active and the pin EN_FMC of the System Controller CPLD U14 is asserted.

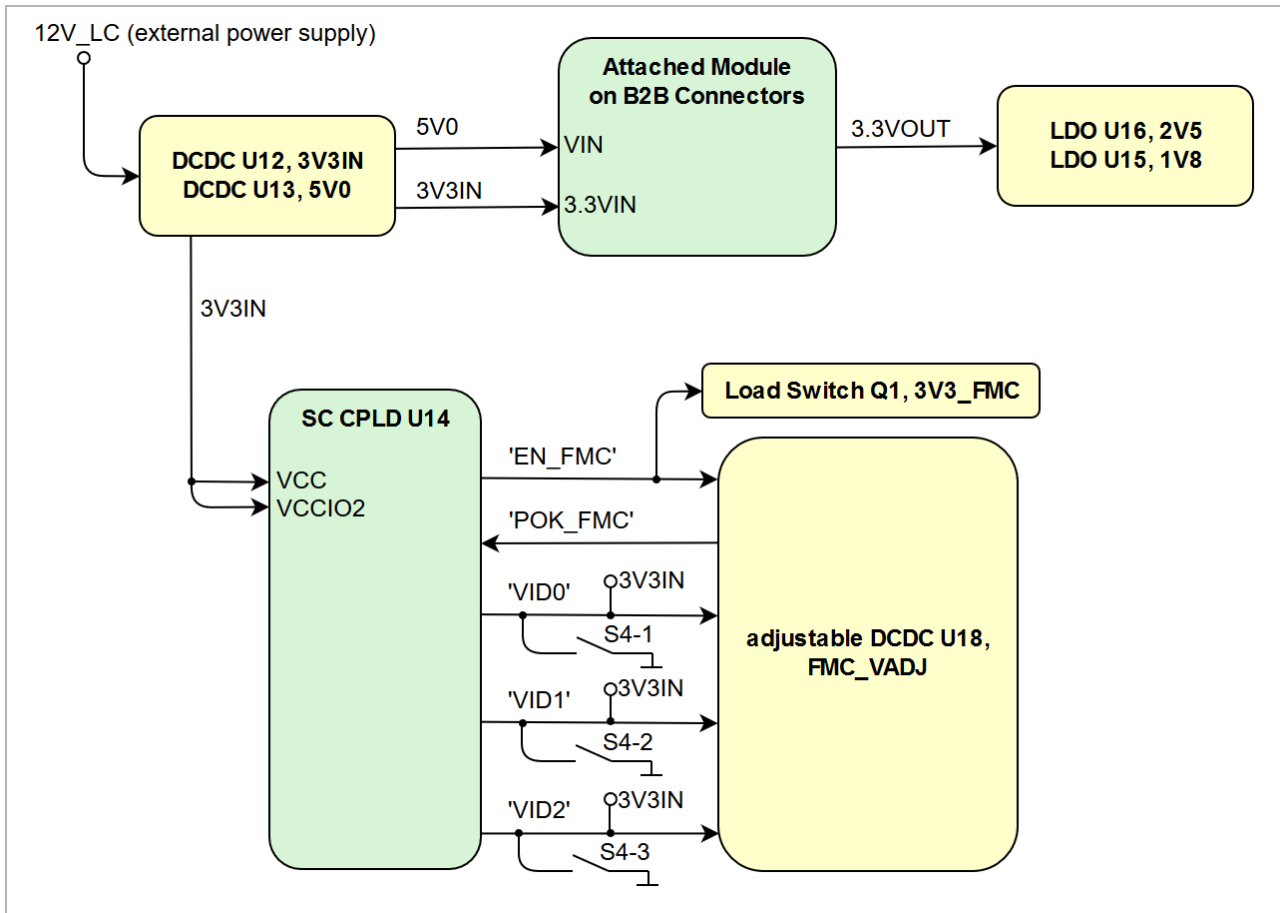


Figure 6: Power Sequence

7.4 Configuring mounted SoM's PL bank VCCO FMC_VADJ

On the TE0701 carrier board different VCCIO configurations can be chosen by 7 jumpers and one dedicated 4-bit DIP-switch S4. Settings of the jumpers and the DIP-switch S4 are explained below.

The baseboard supply voltages for the PL IO-banks VCCO of the SoM are selectable by the jumpers J16, J17 and J21. The DIP-switch S4 sets the adjustable baseboard supply-voltage FMC_VADJ.

Following table below describes switch S4 settings for different FMC_VADJ voltages.

| S4-1 | S4-2 | S4-3 | FMC_VADJ Value |
|------|------|------|---|
| ON | ON | ON | 3.3V |
| OFF | ON | ON | 2.5V |
| ON | OFF | ON | 1.8V |
| OFF | OFF | ON | 1.5V |
| ON | ON | OFF | 1.25V |
| OFF | OFF | OFF | Attention: Set VADJ to S3-M1 and S3-M2 control, read TE0701 System Controller CPLD⁹ description, before this mode is used! |

Table 18: Configuring FMC_VADJ

i There is also option to select fixed voltage of FMC_VADJ with the configuration of the 8-bit control register of the I²C-to-GPIO-module of the System Controller CPLD U14.

Switch S4 is also routed to the System Controller CPLD, hence the VCCIO configuration can be registered by the SC CPLD. Switch S4-4 is not dedicated for FMC_VADJ setting, the function of this switch depends on the System Controller CPLD firmware.

The supply-voltage FMC_VADJ is user programmable via I²C. Configuration of the adjustable voltage FMC_VADJ is done over dedicated I²C bus (lines HDMI_SCL and HDMI_SDA). A control byte has to be sent to the 8-bit control register of the I²C-to-GPIO module of the System Controller CPLD. This module's I²C address is 0x22. To enable FMC_VADJ on TE0701, bit 7 of the control register should be set to 1. Note that the I²C bus is shared with the I²C interface of the HDMI Controller.

For detailed information how to set the voltage FMC_VADJ via I²C, please refer to the documentation of the [TE0701 System Controller CPLD¹⁰](#).

7.5 Configuring 12V Power Supply Pin on the CameraLink Connector

12V power supply can be connected to pin 26 of the CameraLink by closing J18. However, this option is disabled by default (J18: OPEN).

7.6 Summary of VCCIO configuration via jumpers

There are two baseboard supply voltages VIOTA and VIOTB connected to the 4 x 5 SoM's PL IO-bank. The supply voltages have following pin assignments on B2B-connectors:

⁹ <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

¹⁰ <https://wiki.trenz-electronic.de/display/PD/TE0701+CPLD>

| Baseboard supply voltages | TE0701 B2B connector-pins | Standard 4 x 5 SoM's VCCO pins on B2B connectors | Connected with (Pull-up, VCCIO) |
|---------------------------|-------------------------------|--|--|
| VIOTA | JB2-2, JB2-4, JB2-6 | VCCIOB (JM2-1, JM2-3) / VCCIOC (JM2-5) | HDMI_SCL, HDMI_SDA, HDMI_INT, J5 VCCIO |
| VIOTB | JB1-10, JB1-12, JB2-8, JB2-10 | VCCIOA (JM1-9, JM1-11) / VCCIOD (JM2-7, JM2-9) | VCCIO1 (System Controller CPLD pin 55, 73) |

Table 19: Baseboard supply-voltages VIOTA and VIOTB

Note: The corresponding PL IO-voltage supply voltages of the 4 x 5 SoM to the selectable baseboard voltages VIOTA and VIOTB are depending on the mounted 4 x 5 SoM and varying in order of the used model.

Refer to SoM's schematics for more information about the specific pin assignment on module's B2B-connectors regarding PL IO-bank supply voltages and to the [4 x 5 Module integration Guide](#)¹¹ for VCCIO voltage options.

Following table shows baseboard supply voltages versus the available voltage levels, which can be configured via jumpers.

Notation: 'Jx: **1-2**, 3' means pins 1 and 2 are closed, pin 3 is open. 'Jx: 1, **2-3**' means pins 2 and 3 are closed, pin 1 is open.

| Voltage Levels | VIOTA | VIOTB | USB-VBUS | 12V0_CL |
|----------------|---------------------------------|---|----------|---------|
| 3V3 | J17: 1-2 , 3 & J16: open | J17: 1-2 , 3 & J16: open & J21: 1-2 , 3 | - | - |
| 2V5 | J17: 1, 2-3 & J16: open | J17: 1, 2-3 & J16: open & J21: 1-2 , 3 | - | - |
| FMC_VADJ | J17: open & J16: 1-2 | J21: 1, 2-3 | - | - |

¹¹ <https://wiki.trenz-electronic.de/display/PD/4x5+Module+Integration+Guide>

| Voltage Levels | VIOTA | VIOTB | USB-VBUS | 12V0_CL |
|----------------|-------|-------|--|-----------------|
| 5V0 intern | - | - | J9: 1-2 , 3 & J19: 1-2 (J20: 1-2 : additional decoupling-capacitor 200 µF) | - |
| VBUS extern | - | - | J9: 1, 2-3 & J19: open | - |
| 12V_LC | - | - | - | J18: 1-2 |

Table 20: Configuration of baseboard supply-voltages via jumpers

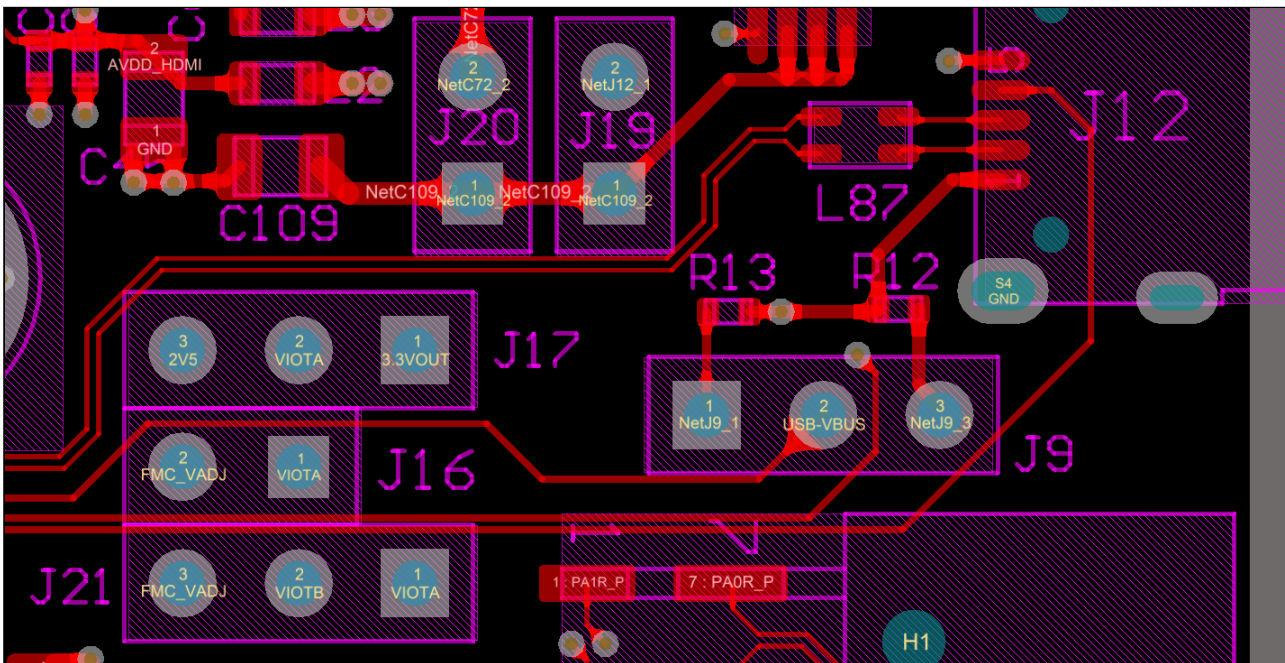


Figure 7: VCCIO jumper pin location (PCB-REV06), top view

⚠ Take care of the VCCO voltage ranges of the particular PL IO-banks (HR, HP) of the mounted SoM, otherwise damages may occur to the FPGA. Therefore, refer to the TRM of the mounted SoM to get the specific information of the voltage ranges.

It is recommended to set and measure the PL IO-bank supply-voltages before mounting of TE 4 x 5 module to avoid failures and damages to the functionality of the mounted SoM.

7.7 Power Rails

| Module Connector (B2B) Designator | VCC / VCCIO | Direction | Pins | Notes |
|-----------------------------------|-------------|-----------|------------|-----------------------------|
| JB1 | 5V0 | Out | 2, 4, 6 | 5.0V module supply voltage |
| | 3.3VIN | Out | 14, 16 | 3.3V module supply voltage |
| | VIOTB | Out | 10, 12 | PL IO-bank VCCO |
| | VIQB | In | 40 | 1.8V module output voltage |
| JB2 | 3.3VOUT | In | 9, 11 | 3.3V module output voltage |
| | 5V0 | Out | 1, 3, 5, 7 | 5.0V module supply voltage |
| | VIOTA | Out | 2, 4, 6 | PL IO-bank VCCO |
| | VIOTB | Out | 8, 10 | PL IO-bank VCCO |
| | VCCJTAG | In | 92 | 3.3V JTAG reference voltage |
| JB3 | USB-VBUS | Out | 56 | USB Host supply voltage |

Table 21: Power pin description of B2B Module Connector

| FMC Designator | VCC / VCCIO | Direction | Pins | Notes |
|----------------|-------------|-----------|------------------------|----------------------|
| J10 | 12V_LC | In | Pin C35, C37 | - |
| | 3V3_FMC | In | Pin D36, D38, D40, C39 | - |
| | 3.3VOUT | In | Pin D32 | - |
| | FMC_VADJ | Out | Pin G39, H40 | adjustable FMC VCCIO |

Table 22: Power pin description of FMC connector

| PMOD Designator | VCC / VCCIO | Direction | Pins | Notes |
|-----------------|-------------|-----------|-----------|-------|
| J1 | 3.3VOUT | Out | Pin 6, 12 | - |
| J2 | 3.3VOUT | Out | Pin 6, 12 | - |
| J5 | VIOTA | Out | Pin 6, 12 | - |
| J6 | FMC_VADJ | Out | Pin 6, 12 | - |

Table 23: Power pin description of Pmod connectors

| Main Power Jack Designator | VCC / VCCIO | Direction | Pins | Notes |
|----------------------------|-------------|-----------|------|------------------------------|
| J13 | 12VIN | In | 1 | - |
| B1 | VBAT | In | + | CR1220 Battery Holder (3.0V) |

Table 24: Power pin description of main power supply connectors

| Peripheral Socket Designator | VCC / VCCIO | Direction | Pins | Notes |
|------------------------------|-------------|-----------|------|----------------------------------|
| J15 | FMC_VADJ | In | 1 | ARM JTAG reference voltage VTREF |

| Peripheral Socket Designator | VCC / VCCIO | Direction | Pins | Notes |
|------------------------------|-------------|-----------|-------|---|
| J3 | 12V0_CL | In | 1, 26 | 12V CameraLink power supply voltage |
| J7 | VBUS | In | 1 | USB2.0 device mode USB VBUS |
| J4 | 5V_HDMI | Out | 18 | 5V HDMI supply voltage from HDMI Protection Circuit U10 |
| J8 | 3.3VOUT | Out | 4 | MicroSD Card Socket |
| J12 | USB-VBUS | In / Out | 1 | Direction depends on USB2 mode (OTG, Host, Device mode) |

Table 25: Power pin description of peripherals' connectors

| Jumper / Header Designator | VCC / VCCIO | Direction | Pins | Notes |
|----------------------------|-------------|-----------|---------|-------|
| J17 | VIOTA | In | 2 | - |
| | 3.3VOUT | Out | 1 | - |
| | 2V5 | Out | 3 | - |
| J21 | VIOTA | In | 1 | - |
| | VIOTB | In | 2 | - |
| | FMC_VADJ | Out | 3 | - |
| J16 | FMC_VADJ | Out | 2 | - |
| | VIOTA | In | 1 | - |
| J18 | 12V_LC | Out | 1 | - |
| | 12V0_CL | In | 2 | - |
| J6 | VCCIOC | In | 2, 4, 6 | - |
| | M1.8VOUT | Out | 1 | - |
| J9 | USB-VBUS | In | 2 | - |

| Jumper / Header Designator | VCC / VCCIO | Direction | Pins | Notes |
|----------------------------|-------------|-----------|------|---|
| | VBUS | Out | 3 | 1K13 serial resistor |
| | VBUS | Out | 1 | 10K serial resistor |
| J19 | 5.0V | Out | 1 | 5.0V from USB-VBUS load switch U11 |
| | VBUS | In | 2 | - |
| J20 | 5.0V | In | 1 | USB-VBUS voltage stabilization with additional 200 μ F capacitance. |
| | 5.0V | Out | 2 | |

Table 26: Power Pin description of VCCIO selection jumpers

8 Board to Board Connectors

⚠ These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three [Samtec Razor Beam LSHM connectors](#)¹² on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

8.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

| Order number | Connector on baseboard | compatible to | Mating height |
|--------------|-----------------------------|-----------------------------|---------------|
| 23836 | REF-189016-01 | LSHM-150-02.5-L-DV-A-S-K-TR | 6.5 mm |
| | LSHM-150-03.0-L-DV-A-S-K-TR | LSHM-150-03.0-L-DV-A-S-K-TR | 7.0 mm |
| 23838 | REF-189016-02 | LSHM-150-04.0-L-DV-A-S-K-TR | 8.0 mm |
| | LSHM-150-06.0-L-DV-A-S-K-TR | LSHM-150-06.0-L-DV-A-S-K-TR | 10.0mm |
| 26125 | REF-189017-01 | LSHM-130-02.5-L-DV-A-S-K-TR | 6.5 mm |
| | LSHM-130-03.0-L-DV-A-S-K-TR | LSHM-130-03.0-L-DV-A-S-K-TR | 7.0 mm |
| 24903 | REF-189017-02 | LSHM-130-04.0-L-DV-A-S-K-TR | 8.0 mm |
| | LSHM-130-06.0-L-DV-A-S-K-TR | LSHM-130-06.0-L-DV-A-S-K-TR | 10.0mm |

Table 27: Connectors.

The module can be manufactured using other connectors upon request.

¹² <https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=LSHM>

8.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

| Stacking height | Speed rating |
|---------------------|--------------------|
| 12 mm, Single-Ended | 7.5 GHz / 15 Gbps |
| 12 mm, Differential | 6.5 GHz / 13 Gbps |
| 5 mm, Single-Ended | 11.5 GHz / 23 Gbps |
| 5 mm, Differential | 7.0 GHz / 14 Gbps |

Table 28: Speed rating.

8.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

8.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

9 Technical Specifications

9.1 Absolute Maximum Ratings

| Parameter | Min | Max | Units | Notes |
|------------------------------------|------|------|-------|---|
| VIN supply voltage | 11.4 | 12.6 | V | ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) standard |
| I/O input voltage for SC CPLD U114 | -0.5 | 3.75 | V | Lattice MachXO2 Family datasheet |
| Voltage on TXS02612RTWR pins | -0.5 | 3.8 | V | TI TXS02612RTWR data sheet |
| Storage temperature | -40 | 100 | °C | LED's SML-P11MTT86 data sheet |

Table 29: Module absolute maximum ratings

9.2 Recommended Operating Conditions

| Parameter | Min | Max | Units | Notes |
|---|------|------|-------|----------------------------------|
| VIN supply voltage | 11.4 | 12.6 | V | - |
| I/O input voltage for SC CPLD U14 | -0.3 | 3.6 | V | Lattice MachXO2 Family datasheet |
| Voltage on TXS02612RTWR pins | 0 | 3.3 | V | TI TXS02612RTWR data sheet |
| Operating Temperature Range ^{1), 2), 3)} | 0 | 70 | °C | - |

Table 30: Recommended Operating Conditions

1) Temperature range may vary depending on assembly options

2) The operating temperature range of the onboard peripherals are a junction and also ambient operating temperature ranges

3) The relevant operating temperature range of the overall system is also determined by the operating temperature range of the attached module.

9.3 Physical Dimensions

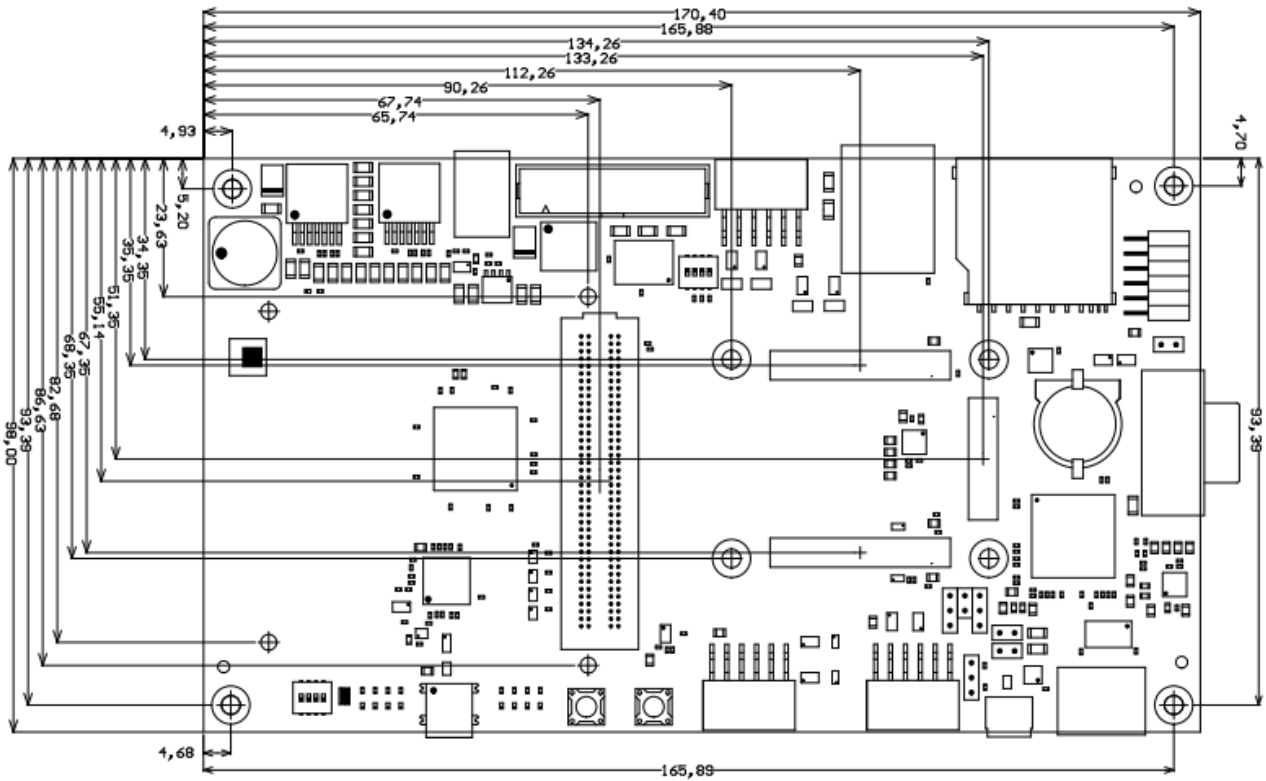


Figure 8: Physical dimensions drawing

10 Variants Currently In Production

| Trenz shop TE0701 overview page | |
|---|--|
| English page¹³ | German page¹⁴ |

Table 31: Trenz Electronic Shop Overview

¹³ <https://shop.trenz-electronic.de/en/TE0701-06-Carrier-Board-for-Trenz-Electronic-7-Series>

¹⁴ <https://shop.trenz-electronic.de/de/TE0701-06-Carrier-Board-for-Trenz-Electronic-7-Series>

11 Revision History

11.1 Hardware Revision History

| Date | Revision | Notes | PCN | Documentation link |
|------|----------|---|--|---|
| - | 06 | Additional Jumper J16 and switch S4 for setting voltage FMC_VADJ. | PCN-20161128 ¹⁵ | TE0701-06 ¹⁶ |
| - | 05 | Improved manufacturing | - | TE0701-05 ¹⁷ |
| - | 04 | - | - | TE0701-04 ¹⁸ |
| - | 03 | Changed DC/DC converters | - | TE0701-03 ¹⁹ |
| - | 02 | Prototype | - | TE0701-02 ²⁰ |
| - | 01 | Prototype | - | TE0701-01 ²¹ |

Table 32: Hardware Revision History



Figure 9: Hardware Revision Number

Hardware revision number is printed on the PCB board next to the module model number separated by the dash.

15 <https://wiki.trenz-electronic.de/display/PD/PCN-20161128+TE0701-05+to+TE0701-06+Hardware+Revision+Change>
 16 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/4x5_Carriers/TE0701/REV06
 17 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/4x5_Carriers/TE0701/REV05
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 20 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/4x5_Carriers/TE0701/REV02
 21 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/4x5_Carriers/TE0701/REV01

11.2 Document Change History

| Date | Revision | Authors | Description |
|--|------------------|-----------------------------|--|
|  2020-08-19 | v.80(see page 6) | John Hartfiel ²² | <ul style="list-style-type: none"> • Corrected USB J9 description • Typos • update Button description • Note for J15 |
| 2019-01-11 | v. 73 | John Hartfiel | <ul style="list-style-type: none"> • correction temperature range |
| 2018-10-22 | v.72 | Ali Naseri | <ul style="list-style-type: none"> • General TRM revision and updated to new style |
| 2018-06-13 | v.66 | Ali Naseri | <ul style="list-style-type: none"> • updated Power-on sequence diagram |
| 2018-01-12 | v.62 | John Hartfiel | <ul style="list-style-type: none"> • Dual PMOD note |
| 2017-11-09 | v.60 | John Hartfiel | <ul style="list-style-type: none"> • add B2B connector section |
| 2017-08-15 | v.59 | John Hartfiel | <ul style="list-style-type: none"> • Add VCCIO Jumper Pin location. • Updated VADJ description. |
| 2017-08-14 | v.58 | John Hartfiel | <ul style="list-style-type: none"> • Description correction. |
| 2017-05-25 | v.56 | Jan Kumann | <ul style="list-style-type: none"> • New physical dimensions drawing of the board. |
| 2017-05-16 | v.51 | Jan Kumann | <ul style="list-style-type: none"> • A few overall improvements and corrections, new block diagram. |
| 2017-04-11 | | Ali Naseri | <ul style="list-style-type: none"> • added block diagram |
| 2017-02-15 | v.45 | Ali Naseri | <ul style="list-style-type: none"> • added warning concerning the use of FTDI tools |
| 2017-02-15 | v.40 | Ali Naseri | <ul style="list-style-type: none"> • added power-on sequence diagram |

²² <https://wiki.trenz-electronic.de/display/~j.hartfiel>

| Date | Revision | Authors | Description |
|------------|----------|----------------|--|
| 2017-01-19 | v.35 | Ali Naseri | <ul style="list-style-type: none"> • correction of table 3 (switch-positions to adjust FMC_VADJ) • inserted hint to set and measure the PL IO-bank supply-voltages |
| 2017-01-13 | v.20 | Ali Naseri | <ul style="list-style-type: none"> • added section for baseboard supply voltage configuration |
| 2016-11-29 | v.10 | Ali Naseri | <ul style="list-style-type: none"> • TRM update due to new revision 06 of the carrier board. |
| 2016-11-28 | v.4 | Ali Naseri | <ul style="list-style-type: none"> • TRM adjustment to the newest revision (05) of TE0701 Carrier Board. |
| 2014-02-18 | 0.2 | Sven-Ole Voigt | <ul style="list-style-type: none"> • TE0701-03 (REV3) updated |
| 2014-01-05 | 0.1 | Sven-Ole Voigt | <ul style="list-style-type: none"> • Initial release |

Table 33: Document change history

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 2019-06-07

²³ <http://guidance.echa.europa.eu/>

²⁴ <https://echa.europa.eu/candidate-list-table>

²⁵ <http://www.echa.europa.eu/>

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