

**TM0035N03DF**

**N-Channel Enhancement Mosfet**

**General Description**

- Low  $R_{DS(ON)}$
- RoHS and Halogen-Free Compliant

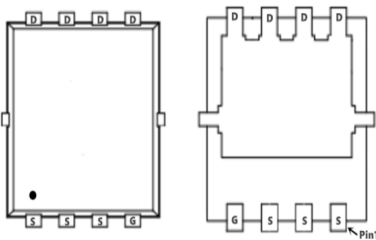
**Applications**

- Load switch
- PWM

**General Features**

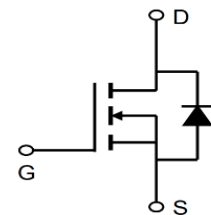
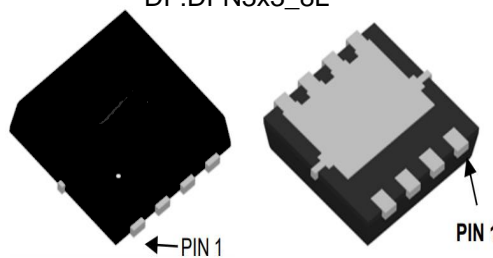
$V_{DS} = 30V$   $I_D = 100A$   
 $R_{DS(ON)} = 3.5 m\Omega (Typ.) @ V_{GS} = 10V$

- 100% UIS Tested
- 100%  $R_g$  Tested



Marking:100N03D

DF:DFN3x3\_8L



**Absolute Maximum Ratings** ( $T_A = 25^\circ C$  Unless Otherwise Noted)

Symbol	Parameter	Rating		Units
		10s	Steady State	
$V_{DS}$	Drain-Source Voltage	30		V
$V_{GS}$	Gate-Source Voltage	$\pm 20$		V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	100		A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	50		A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	30	19	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	25	16	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	162		A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	144.7		mJ
$I_{AS}$	Avalanche Current	53.8		A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation <sup>4</sup>	62.5		W
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>4</sup>	6	2.42	W
$T_{STG}$	Storage Temperature Range	-55 to 175		$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 175		$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup> ( $t \leq 10s$ )	---	25	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	2.4	$^\circ C/W$

**TM0035N03DF**
**N-Channel Enhancement Mosfet**
**Electrical Characteristics** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V,$	-	-	1.0	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>note3</small>	$V_{GS}=10V, I_D=30A$	-	3.5	5.4	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	5.5	10	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	2100	-	pF
$C_{oss}$	Output Capacitance		-	326	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	282	-	pF
$Q_g$	Total Gate Charge	$V_{DS}=15V, I_D=30A,$ $V_{GS}=10V$	-	45	-	nC
$Q_{gs}$	Gate-Source Charge		-	3	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	15	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=15V,$ $I_D=30A, R_{GEN}=3\Omega,$ $V_{GS}=10V$	-	21	-	ns
$t_r$	Turn-on Rise Time		-	32	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	59	-	ns
$t_f$	Turn-off Fall Time		-	34	-	ns
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	100	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=30A$	-	-	1.2	V
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=20A, di/dt=100A/\mu s$	-	15	-	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	4	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

 2. EAS condition:  $T_J=25^\circ\text{C}, V_G=10V, R_G=25\Omega, L=0.5\text{mH}, I_{AS}=18.4A$ 

 3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 0.5\%$

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Figure 1: Output Characteristics

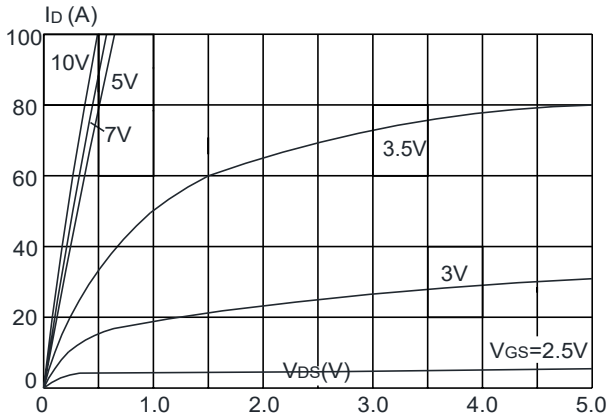


Figure 2: Typical Transfer Characteristics

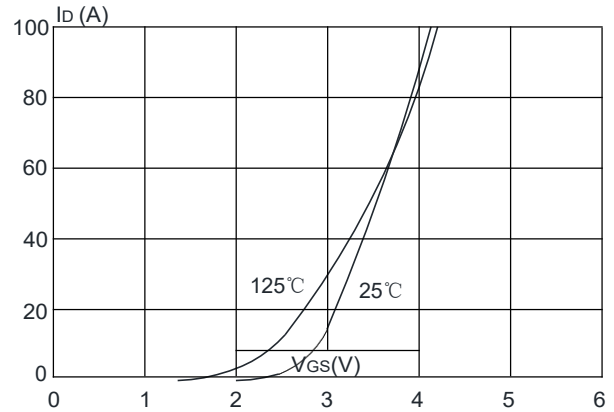


Figure 3: On-resistance vs. Drain Current

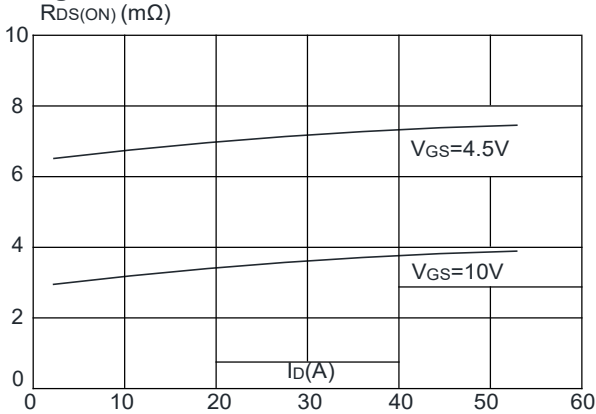


Figure 4: Body Diode Characteristics

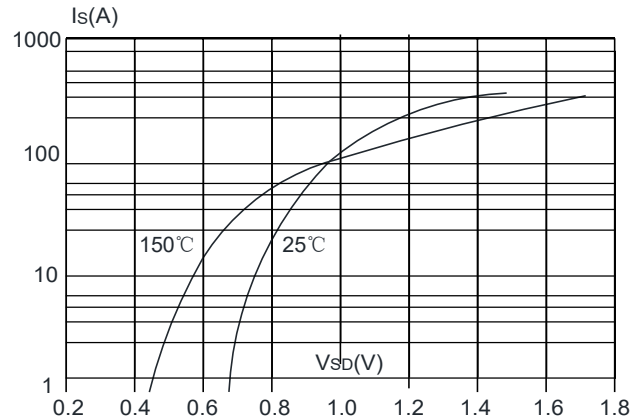


Figure 5: Gate Charge Characteristics

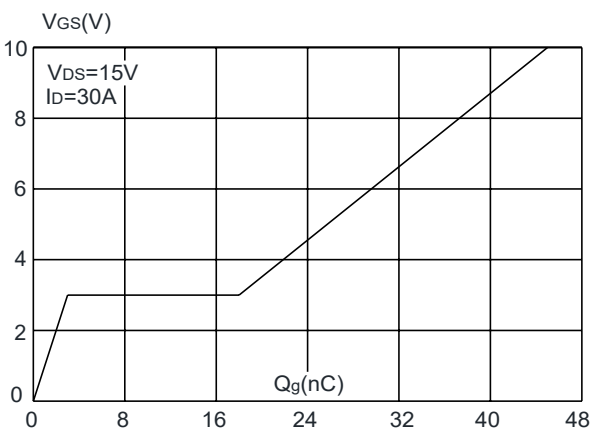
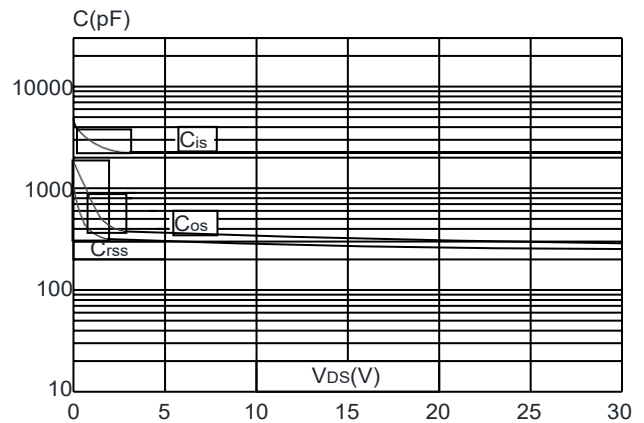


Figure 6: Capacitance Characteristics



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Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

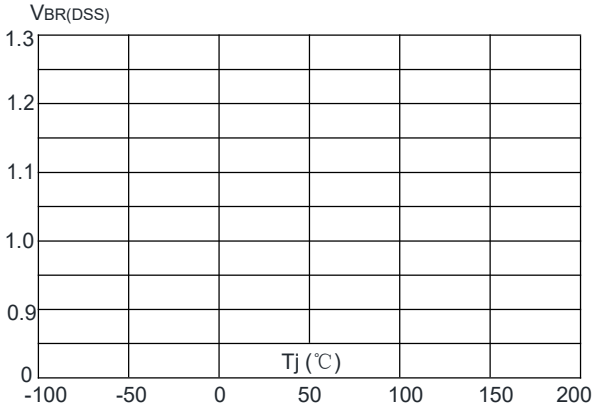


Figure 8: Normalized on Resistance vs. Junction Temperature

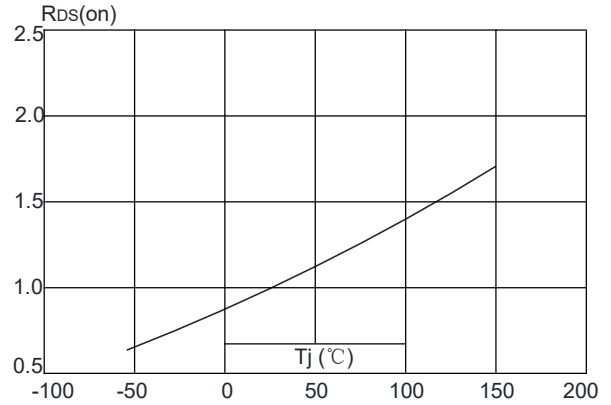


Figure 9: Maximum Safe Operating Area

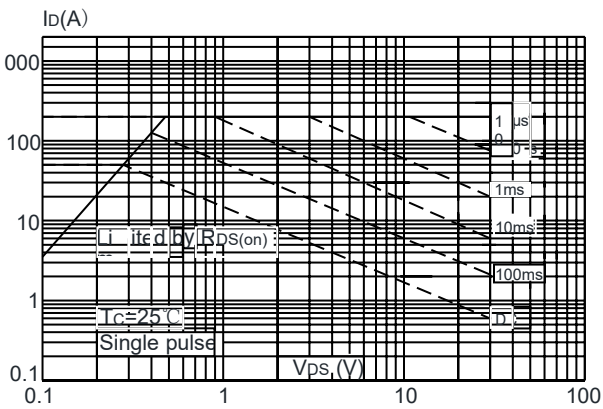


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

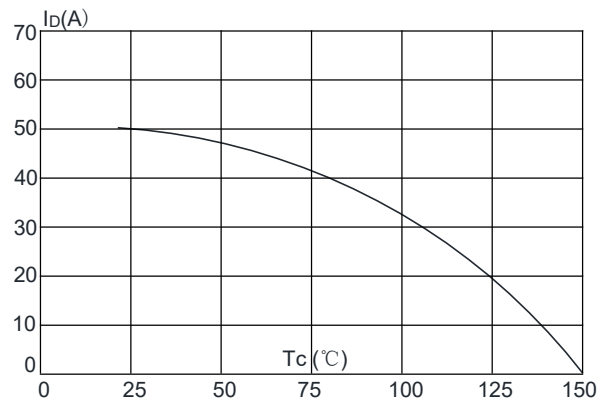
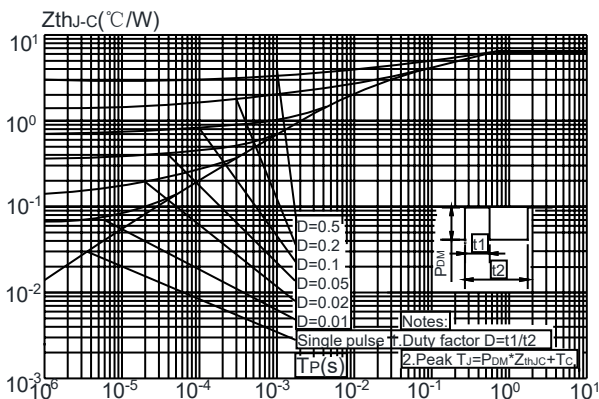


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (PDFN3.3\*3.3-8L)



Test Circuit

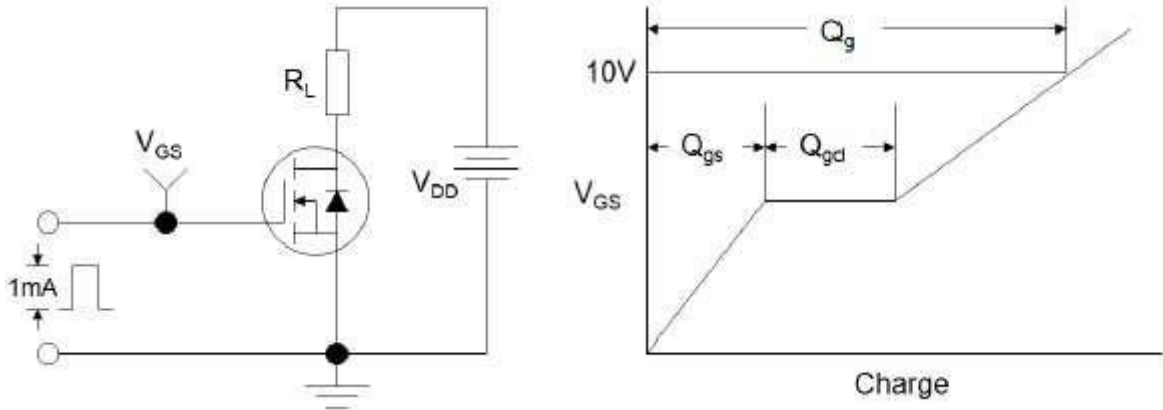


Figure1:Gate Charge Test Circuit & Waveform

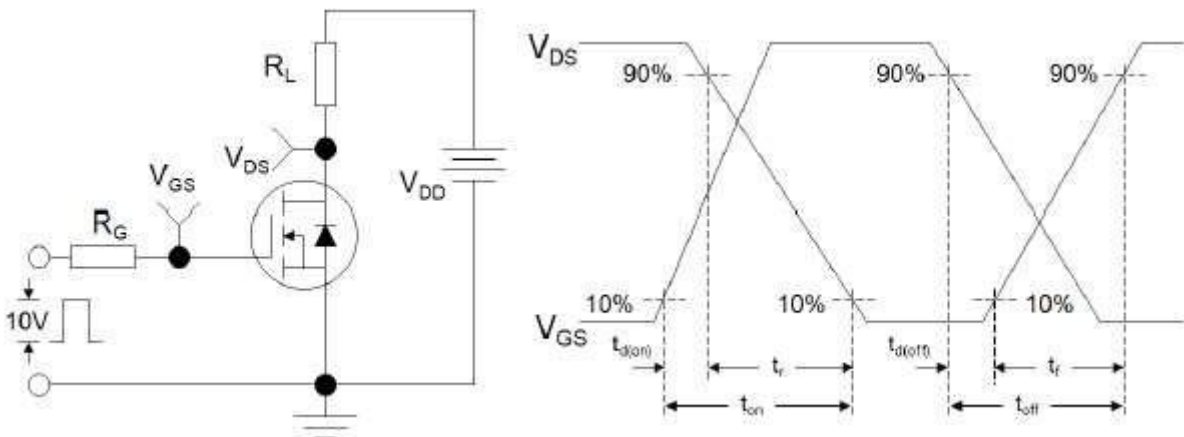


Figure 2: Resistive Switching Test Circuit & Waveforms

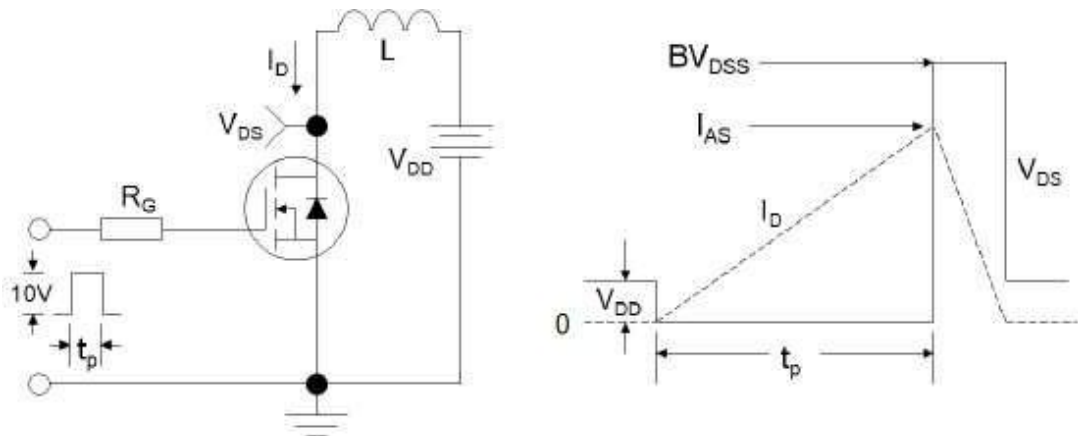
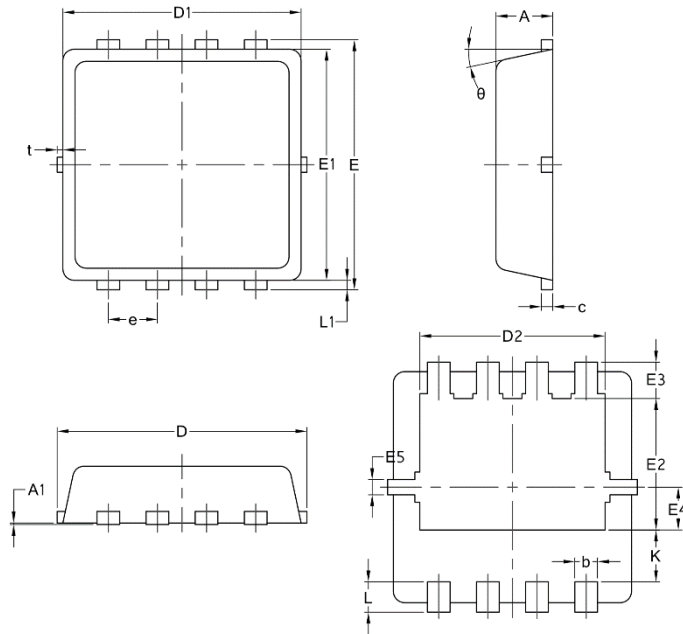


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

## Package Mechanical Data: DFN3x3-8L



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

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