
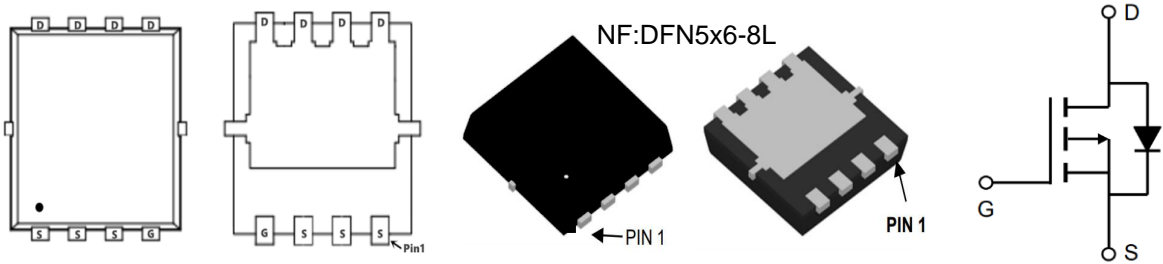




**TM0072P03NF**

**P-Channel Enhancement Mosfet**

<p><b>General Description</b></p> <ul style="list-style-type: none"> <li>• Low <math>R_{DS(ON)}</math></li> <li>• RoHS and Halogen-Free Compliant</li> </ul> <p><b>Applications</b></p> <ul style="list-style-type: none"> <li>• Load switch</li> <li>• PWM</li> </ul>	<p><b>General Features</b></p> <p><math>V_{DS} = -30V</math> <math>I_D = -60A</math>  <math>R_{DS(ON)} = 7.2m\Omega</math>(typ.) @ <math>V_{GS} = -10V</math></p> <p>100% UIS Tested                  100% <math>R_g</math> Tested</p> 
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NF:DFN5x6-8L

Marking: 60P03

**Absolute Maximum Ratings** ( $T_A = 25^\circ C$  Unless Otherwise Noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C = 25^\circ C$	-60
		$T_C = 100^\circ C$	-35
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	-168	A
Single Pulse Avalanche Energy <sup>2</sup>	<b>EAS</b>	45	mJ
Total Power Dissipation	$T_C = 25^\circ C$	$P_D$	45
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	65	$^\circ C/W$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	3.36	$^\circ C/W$

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Electrical Characteristics ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static Characteristics</b>							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V	
Gate-body Leakage current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30V, V_{GS} = 0V$	$T_J = 25^\circ\text{C}$	-	-	-1	$\mu A$
			$T_J = 100^\circ\text{C}$	-	-	-100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-	-2.5	V	
Drain-Source On-Resistance <sup>4</sup>	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -30A$	-	7.2	9.0	m $\Omega$	
		$V_{GS} = -4.5V, I_D = -15A$	-	10	18		
Forward Transconductance <sup>4</sup>	$g_{fs}$	$V_{DS} = -5V, I_D = -30A$	-	57	-	S	
<b>Dynamic Characteristics<sup>5</sup></b>							
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0V, f = 1MHz$	-	2396	-	pF	
Output Capacitance	$C_{oss}$		-	325	-		
Reverse Transfer Capacitance	$C_{rss}$		-	283	-		
Gate Resistance	$R_g$	$f = 1MHz$	-	10.5	-	$\Omega$	
<b>Switching Characteristics<sup>5</sup></b>							
Total Gate Charge	$Q_g$	$V_{GS} = -10V, V_{DS} = -15V, I_D = -30A$	-	30	-	nC	
Gate-Source Charge	$Q_{gs}$		-	5	-		
Gate-Drain Charge	$Q_{gd}$		-	7.5	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -15V, R_G = 3\Omega, I_D = -30A$	-	14.1	-	ns	
Rise Time	$t_r$		-	20	-		
Turn-Off Delay Time	$t_{d(off)}$		-	94	-		
Fall Time	$t_f$		-	65	-		
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -30A, di/dt = 100A/\mu s$	-	19	-	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	9	-	nC	
<b>Drain-Source Body Diode Characteristics</b>							
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	$I_S = -1A, V_{GS} = 0V$	-	-	-1.2	V	
Continuous Source Current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	-60	A	

Note :

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)} = 150^\circ\text{C}$ .
2. The EAS data shows Max. rating . The test condition is  $V_{DD} = -25V, V_{GS} = -10V, L = 0.1mH, I_{AS} = -30A$ .
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test.



Typical Characteristics

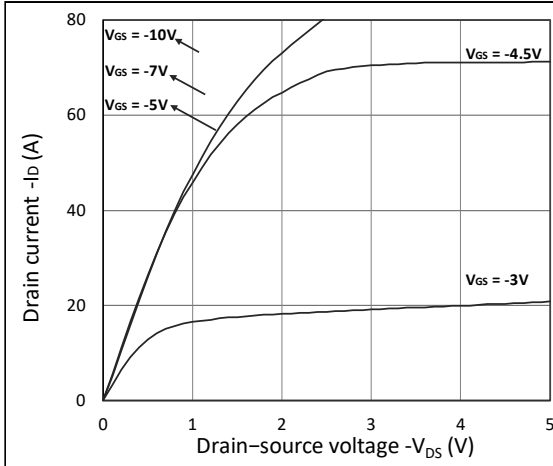


Figure 1. Output Characteristics

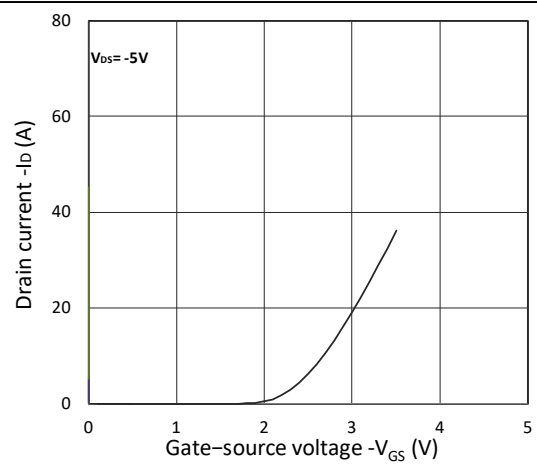


Figure 2. Transfer Characteristics

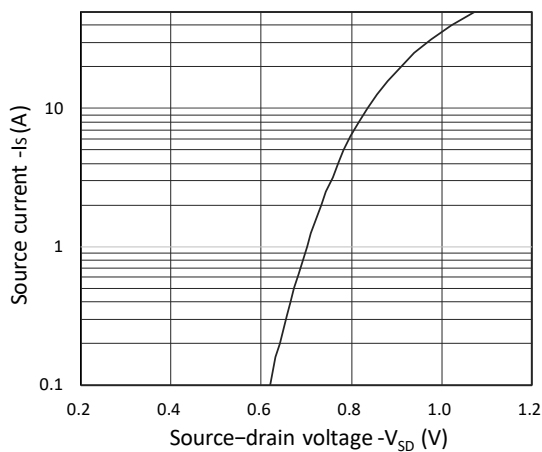


Figure 3. Forward Characteristics of Reverse

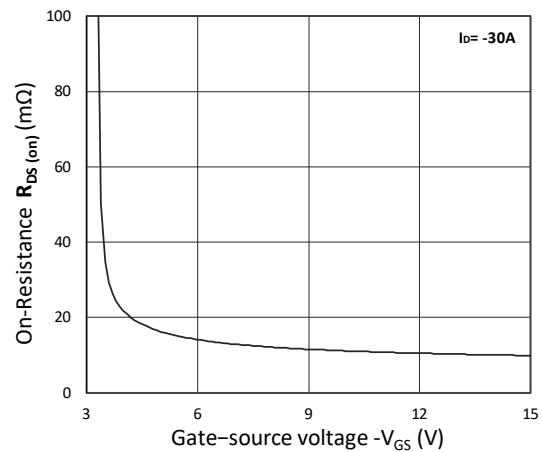


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

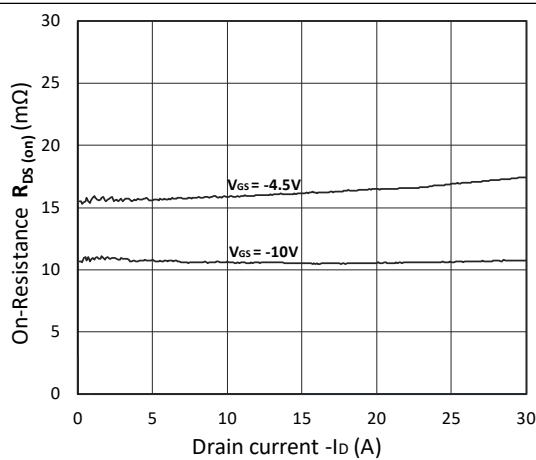


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

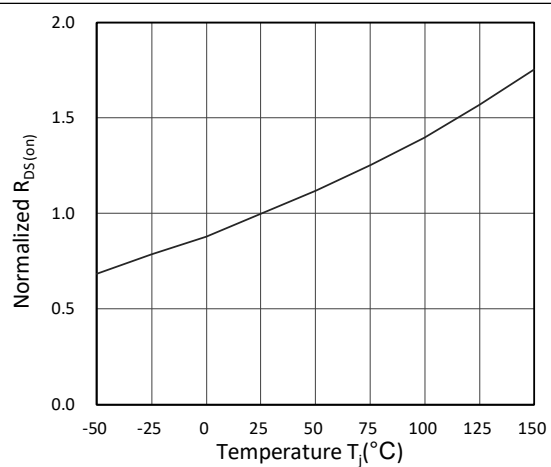


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

**TM0072P03NF**

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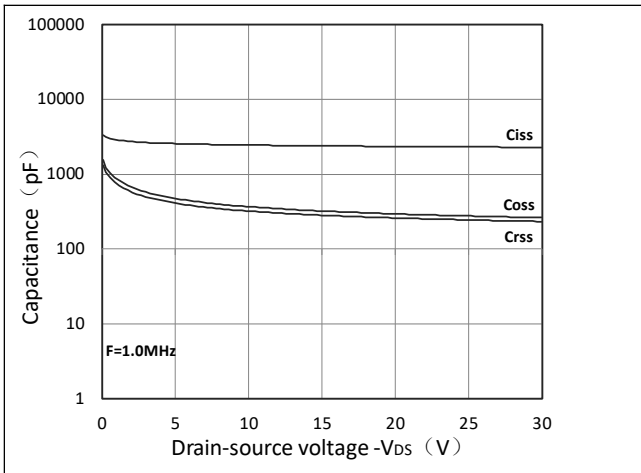


Figure 7. Capacitance Characteristics

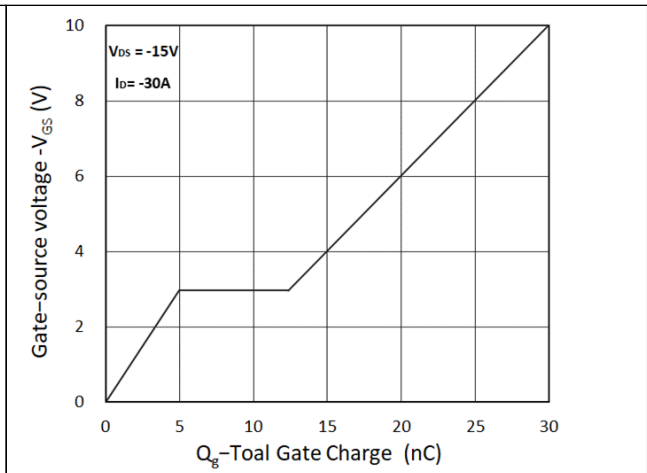


Figure 8. Gate Charge Characteristics

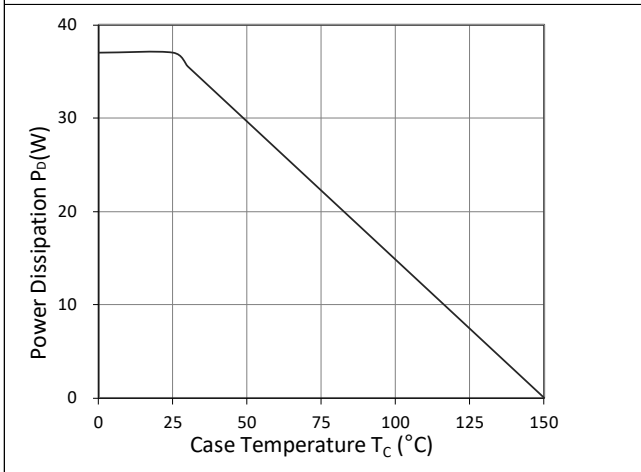


Figure 9. Power Dissipation

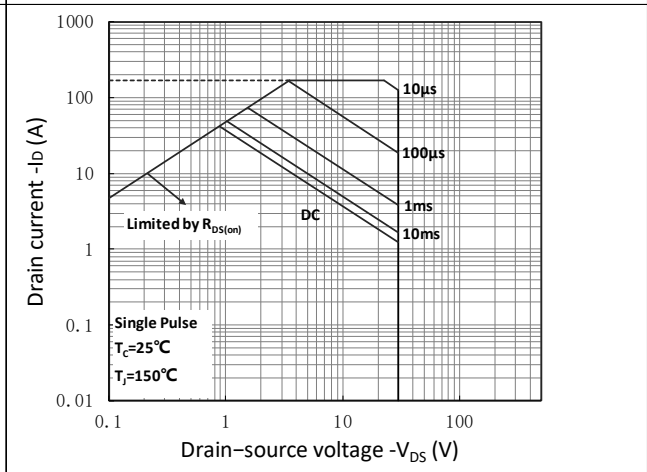


Figure 10. Safe Operating Area

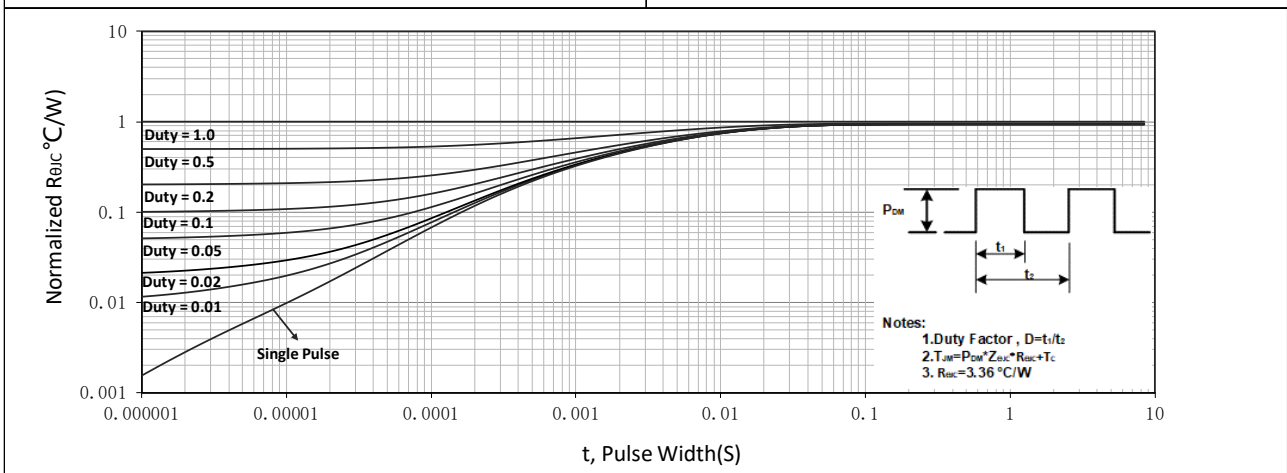


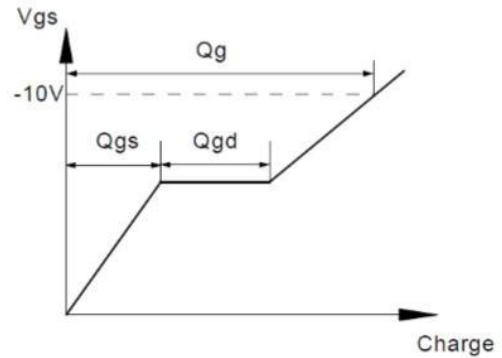
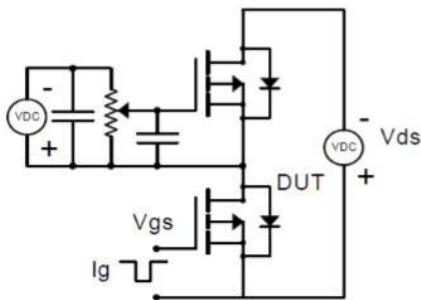
Figure 11. Normalized Maximum Transient Thermal Impedance



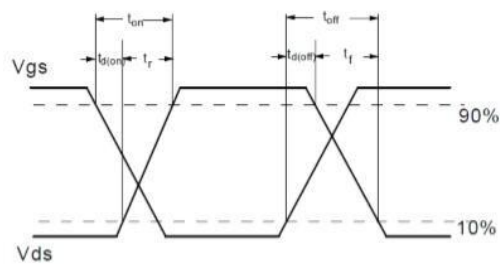
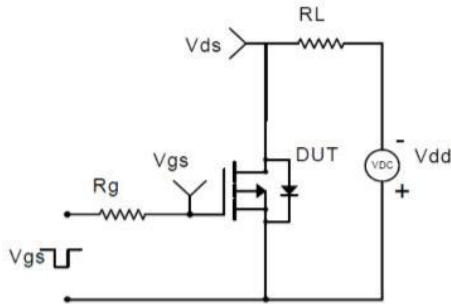


### Test Circuit

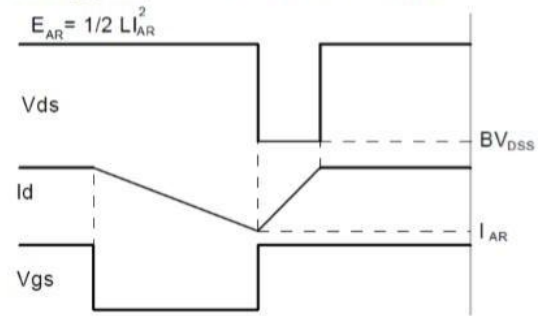
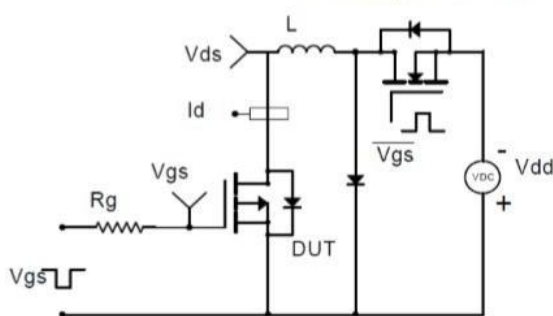
Gate Charge Test Circuit & Waveform



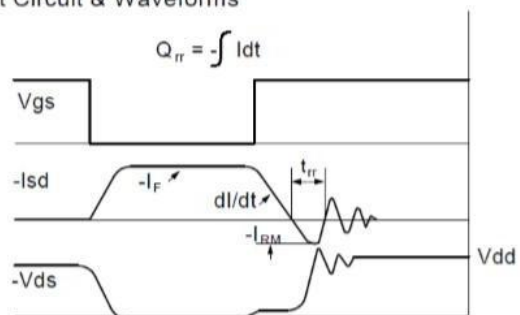
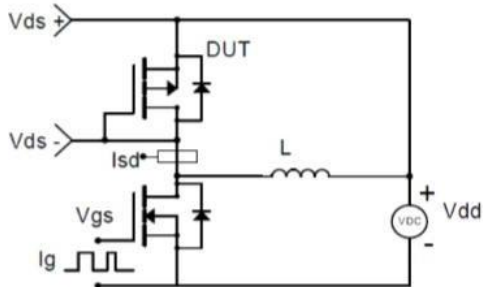
Resistive Switching Test Circuit & Waveforms



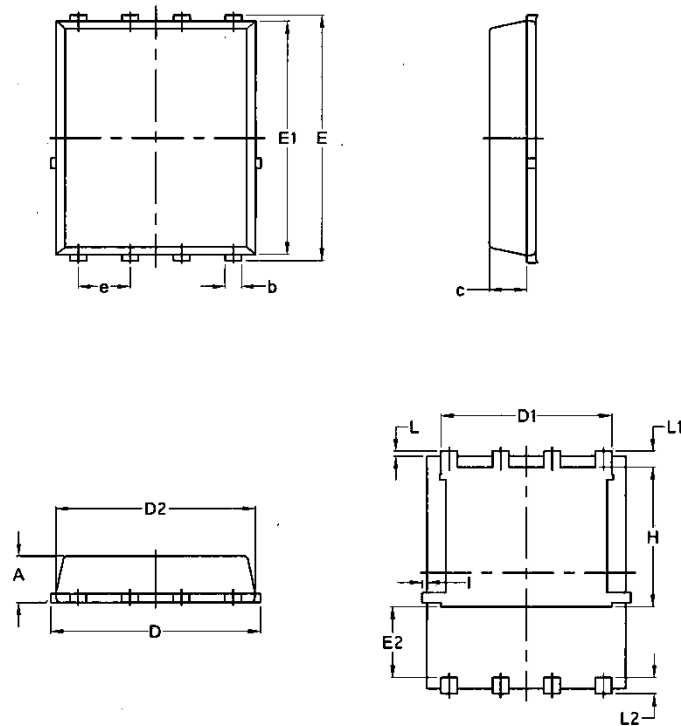
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



## Package Mechanical Data: DFN5x6-8L



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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