

TM009N03BDF

N-Channel Enhancement Mosfet

**General Description**

- Low  $R_{DS(ON)}$
- RoHS and Halogen-Free Compliant

**Applications**

- Load switch
- PWM

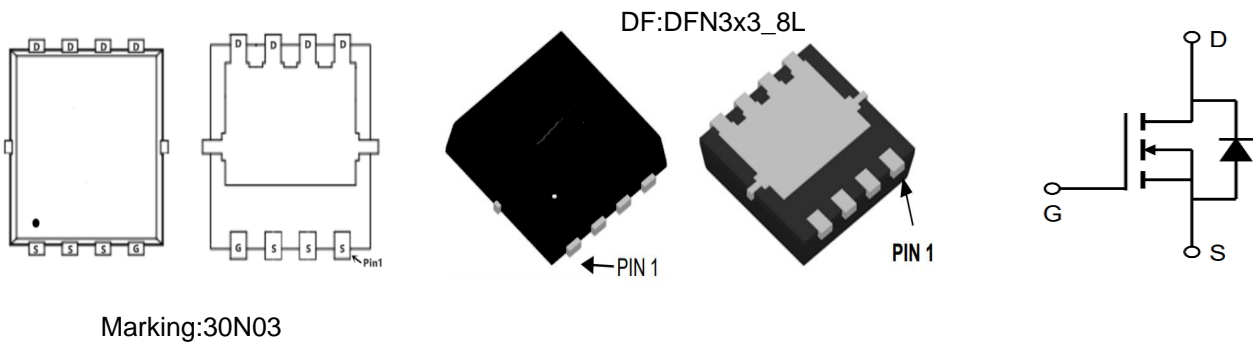
**General Features**

$V_{DS} = 30V$   $I_D = 30A$

$R_{DS(ON)} = 9m\Omega$ (typ.) @  $V_{GS} = 10V$

100% UIS Tested

100%  $R_g$  Tested



**Absolute Maximum Ratings** ( $T_A = 25^\circ C$  Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	30	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	10	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	90	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	19	mJ
$I_{AS}$	Avalanche Current	25	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>4</sup>	10	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	---	85	$^\circ C/W$



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**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)

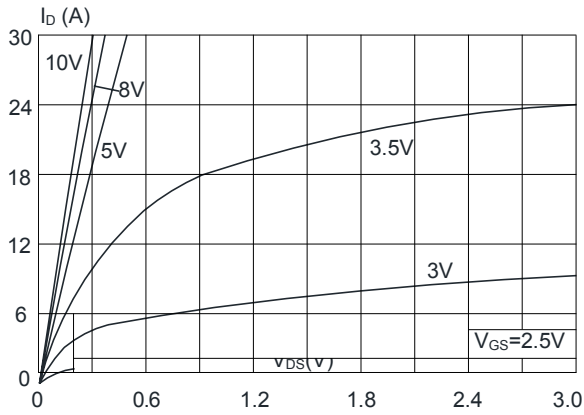
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V,$	-	-	1.0	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
$R_{DS(on)}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10V, I_D=10A$	-	9	14	m $\Omega$
		$V_{GS}=4.5V, I_D=5A$	-	15	22.5	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V,$ $f=1.0MHz$	-	633	-	pF
$C_{oss}$	Output Capacitance		-	120	-	pF
$C_{riss}$	Reverse Transfer Capacitance		-	99	-	pF
$Q_g$	Total Gate Charge	$V_{DS}=15V, I_D=10A,$ $V_{GS}=10V$	-	15	-	nC
$Q_{gs}$	Gate-Source Charge		-	4.7	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	3.6	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=30V, I_D=18A,$ $R_{GEN}=3\Omega, V_{GS}=10V$	-	5	-	ns
$t_r$	Turn-on Rise Time		-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	21	-	ns
$t_f$	Turn-off Fall Time		-	7	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	30	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	72	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=18A$	-	-	1.2	V
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=18A, di/dt=100A/\mu s$	-	7	-	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	5.9	-	nC

Note :

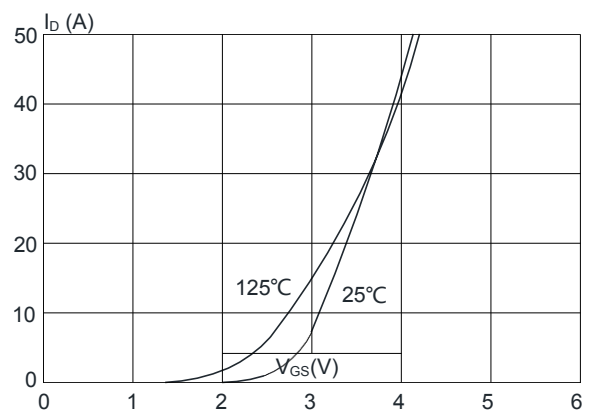
1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
2. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=20A$
4. The power dissipation is limited by 150 $^\circ\text{C}$  junction temperature
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

### Typical Performance Characteristics

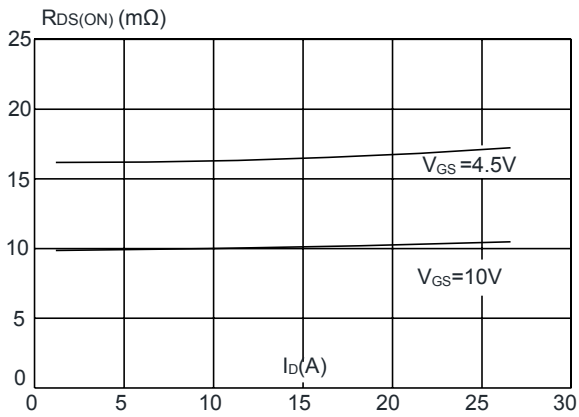
**Figure 1: Output Characteristics**



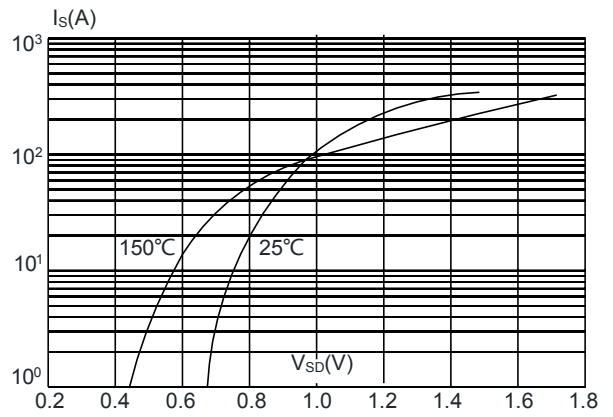
**Figure 2: Typical Transfer Characteristics**



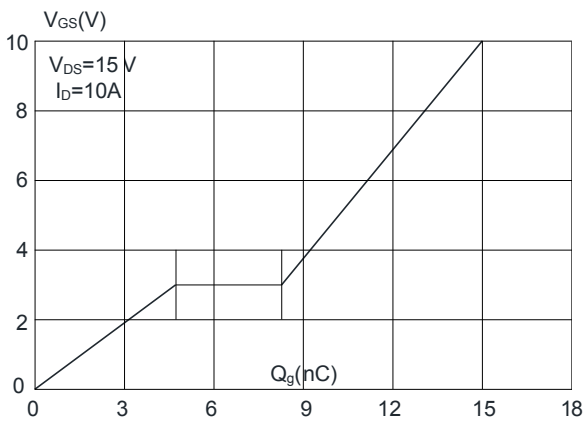
**Figure 3: On-resistance vs. Drain Current**



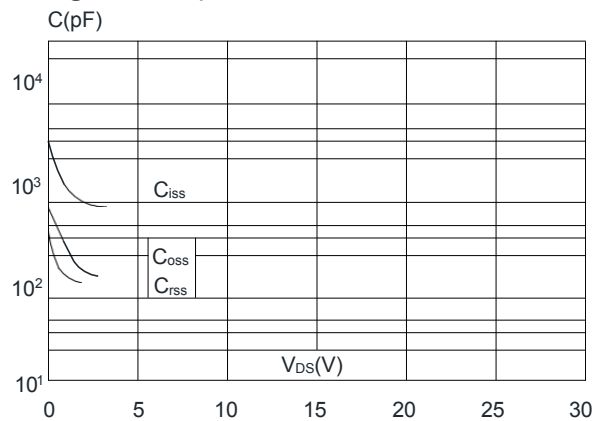
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**



**Figure 6: Capacitance Characteristics**



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Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

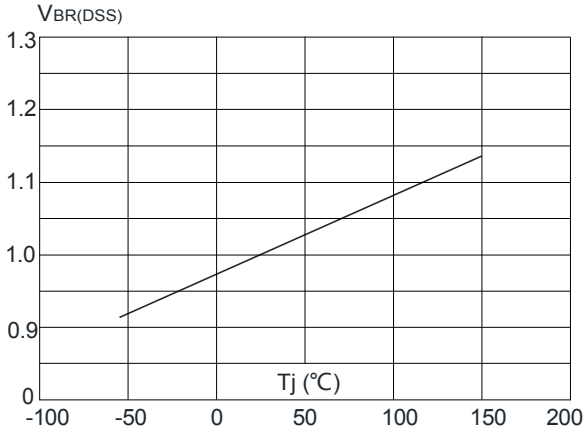


Figure 8: Normalized on Resistance vs. Junction Temperature

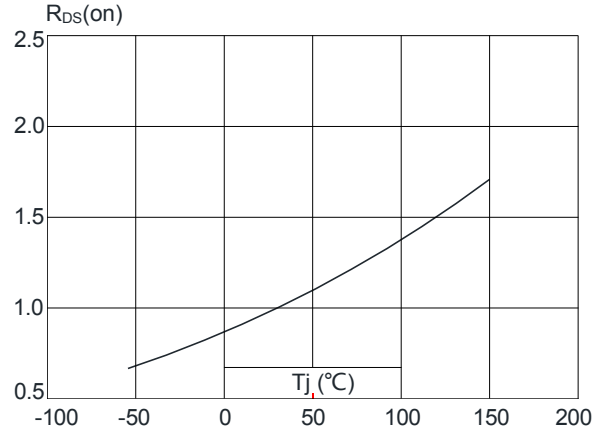


Figure 9: Maximum Safe Operating Area

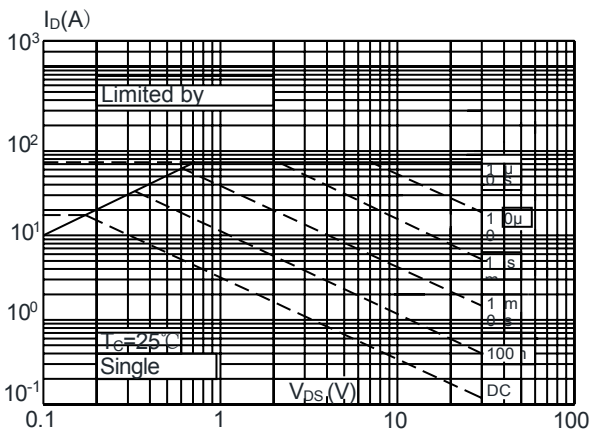


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

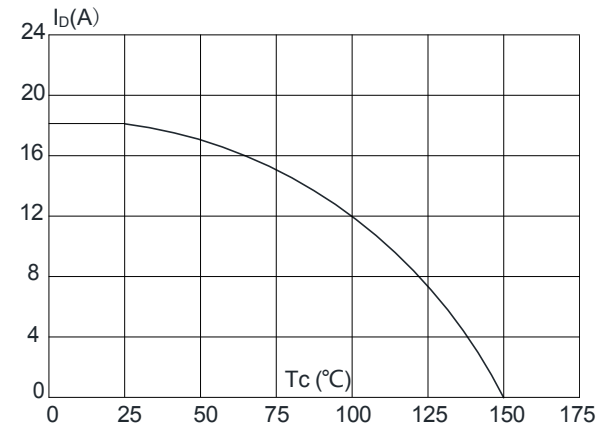
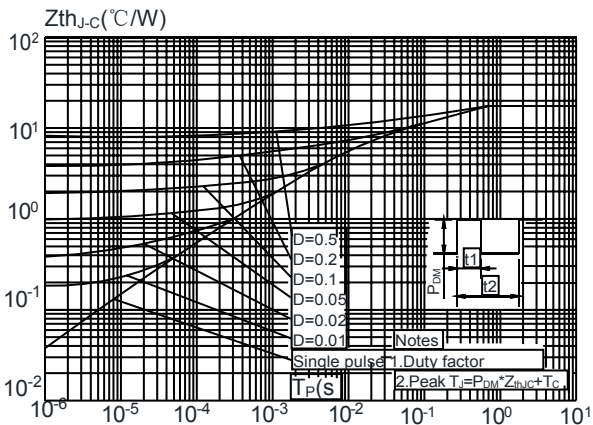


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Test Circuit

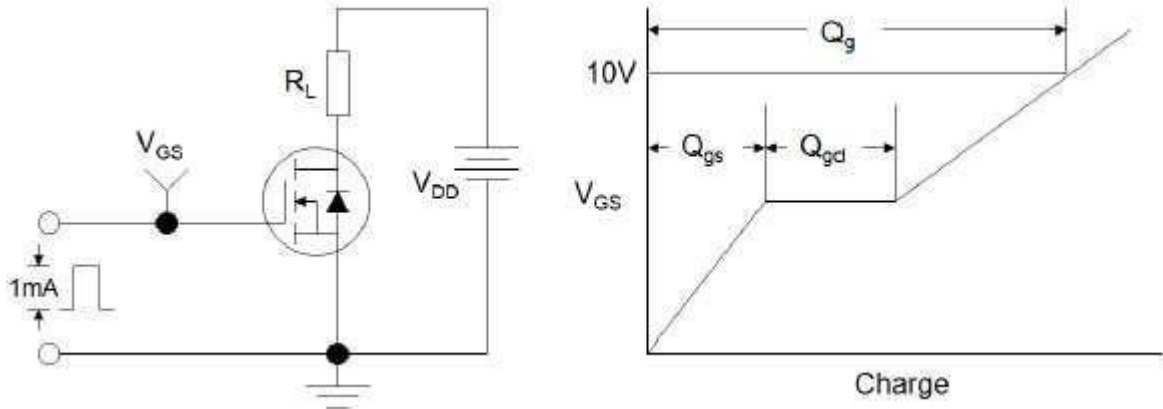


Figure1:Gate Charge Test Circuit & Waveform

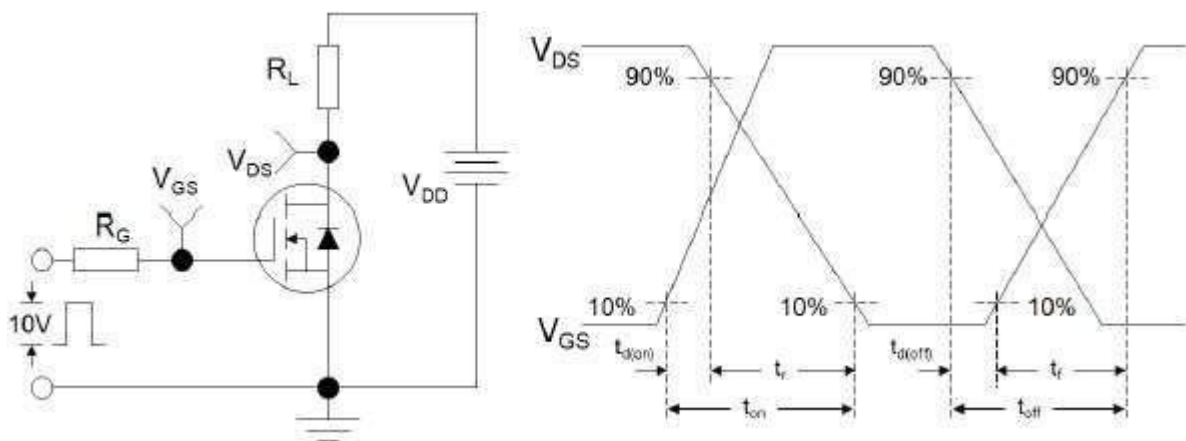


Figure 2: Resistive Switching Test Circuit & Waveforms

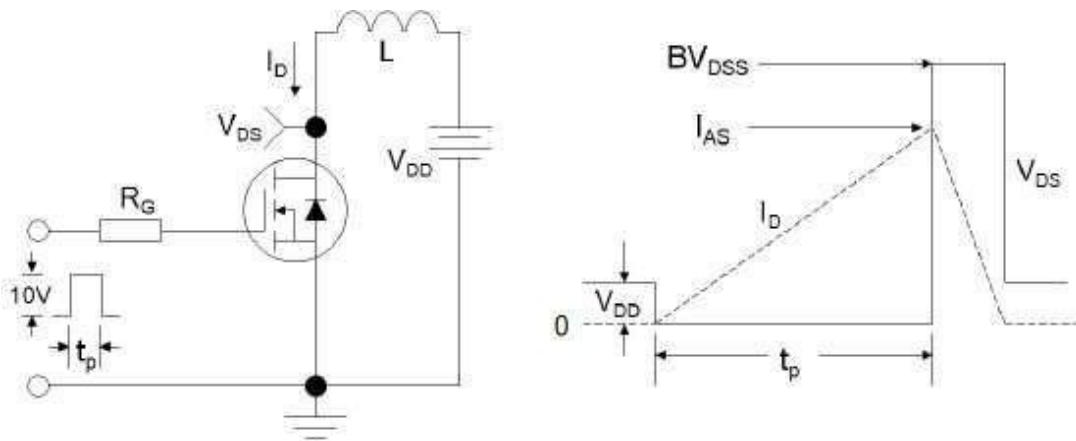
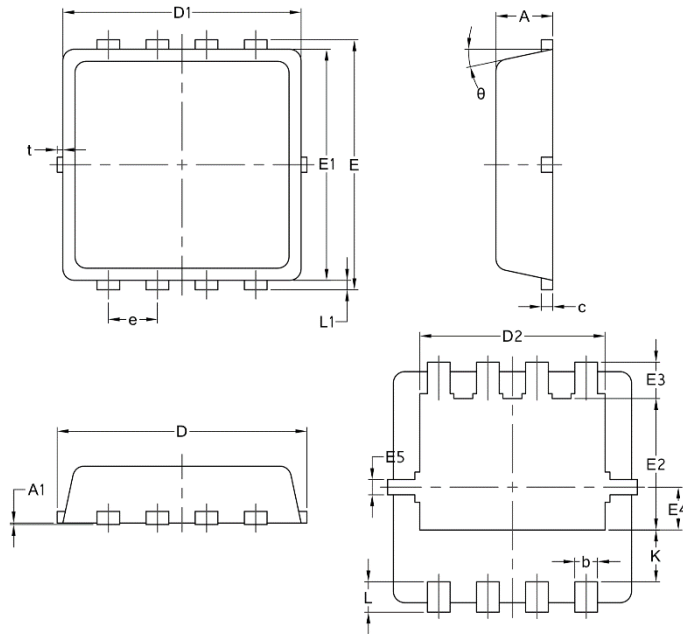


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

## Package Mechanical Data:DFN3x3–8L



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

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