
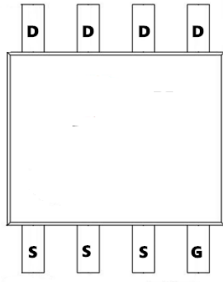




TM4485

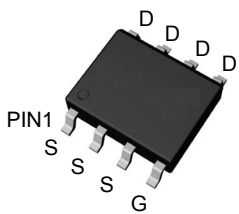
P-Channel Enhancement MOSFET

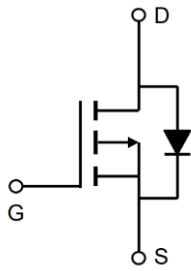
<p>General Description</p> <ul style="list-style-type: none"> • Low $R_{DS(ON)}$ • RoHS and Halogen-Free Compliant <p>Applications</p> <ul style="list-style-type: none"> • Load switch • PWM 	<p>General Features</p> <p>$V_{DS} = -40V$ $I_D = -15 A$</p> <p>$R_{DS(ON)} = 15m\Omega (typ.) @ V_{GS} = -10 V$</p> <p>100% UIS Tested 100% R_g Tested</p> 
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PIN1

S:SOP-8L





Marking 15P04 OR 4485

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 25	
I_D^a	Continuous Drain Current ($V_{GS} = -10V$)	$T_A = 25^\circ C$	-11
		$T_A = 70^\circ C$	-9
I_{DM}^a	300 μs Pulsed Drain Current ($V_{GS} = -10V$)	-15	A
I_S^a	Diode Continuous Forward Current	-3	mJ
I_{AS}^b	Avalanche Current, Single pulse ($L = 0.1mH$)	-33	
E_{AS}^b	Avalanche Energy, Single pulse ($L = 0.1mH$)	54	
T_J	Maximum Junction Temperature	150	$^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150	
P_D^a	Maximum Power Dissipation	$T_A = 25^\circ C$	3.1
		$T_A = 70^\circ C$	2.0
$R_{\theta JA}^a$	Thermal Resistance-Junction to Ambient	$t \leq 10s$	40
		Steady State	75
$R_{\theta JL}^c$	Thermal Resistance-Junction to Lead	Steady State	24

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

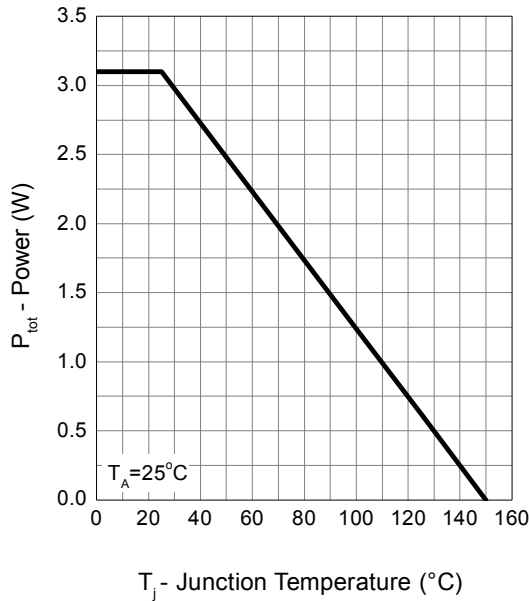
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-32V, V _{GS} =0V T _J =85°C	-	-	-1	μA
			-	-	-30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250μA	-1.0	-1.5	-2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^a	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-11A	-	15	19	mΩ
		V _{GS} =-4.5V, I _{DS} =-7A	-	19.5	22	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =-1A, V _{GS} =0V	-	-0.75	-1	V
t _r	Reverse Recovery Time	I _{SD} =-11A, dI _{SD} /dt=100A/μs	-	24	-	ns
Q _{rr}	Reverse Recovery Charge		-	18	-	nC
Dynamic Characteristics^b						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	-	2.3	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-20V, Frequency=1.0MHz	-	1500	-	pF
C _{oss}	Output Capacitance		-	235	-	
C _{rss}	Reverse Transfer Capacitance		-	180	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =-20V, R _L =20Ω, I _{DS} =-1A, V _{GEN} =-10V, R _G =6Ω	-	14	-	ns
t _r	Turn-on Rise Time		-	12	-	
t _{d(OFF)}	Turn-off Delay Time		-	41	-	
t _f	Turn-off Fall Time		-	22	-	
Gate Charge Characteristics^b						
Q _g	Total Gate Charge	V _{DS} =-20V, V _{GS} =-10V, I _{DS} =-11A	-	32	-	nC
Q _{gs}	Gate-Source Charge		-	5.2	-	
Q _{gd}	Gate-Drain Charge		-	8	-	

Note a: Pulse test; pulse width≤300μs, duty cycle≤2%.

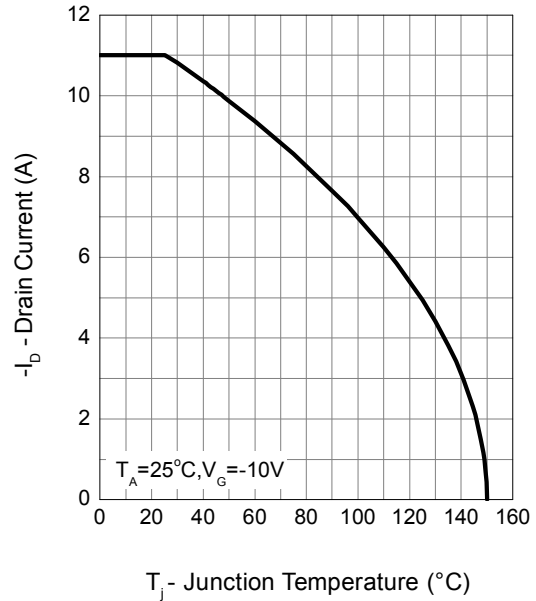
Note b: Guaranteed by design, not subject to production testing.

Typical Characteristics

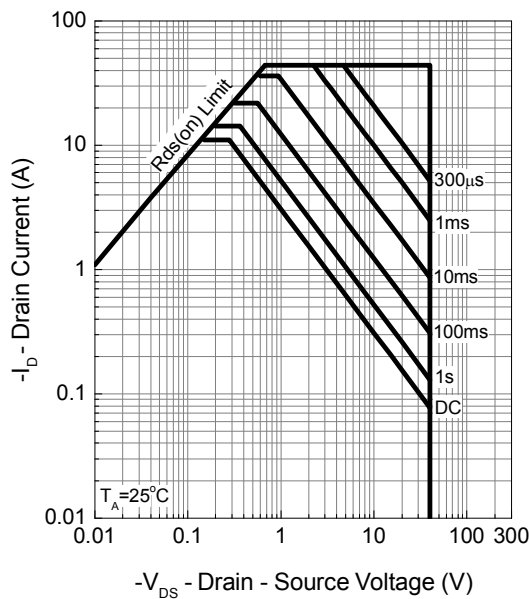
Power Dissipation



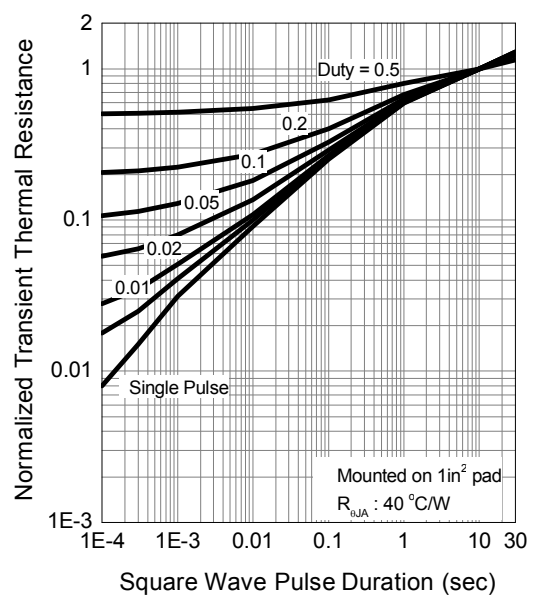
Drain Current



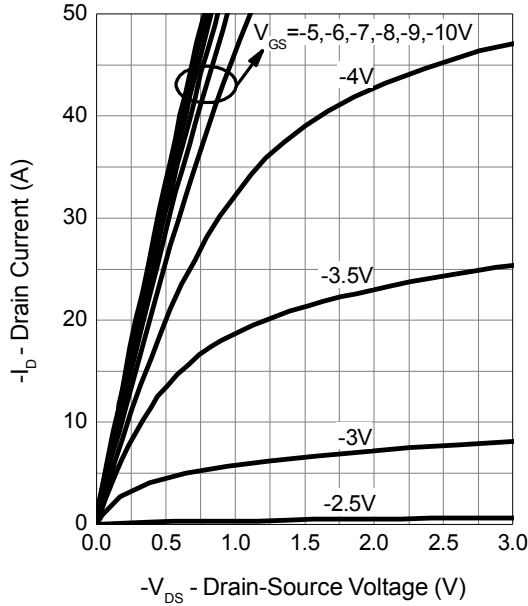
Safe Operation Area



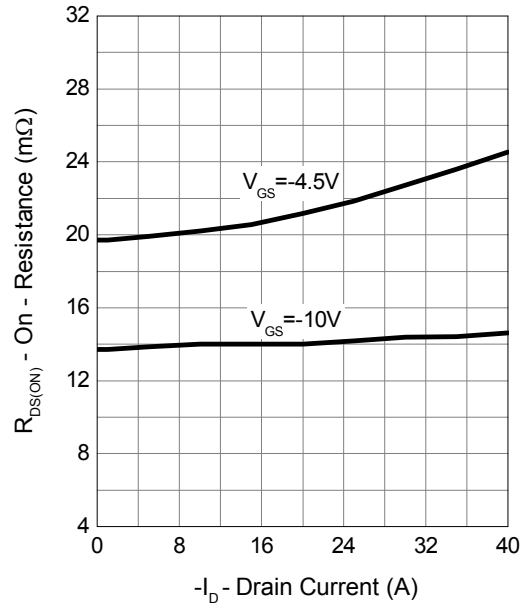
Thermal Transient Impedance



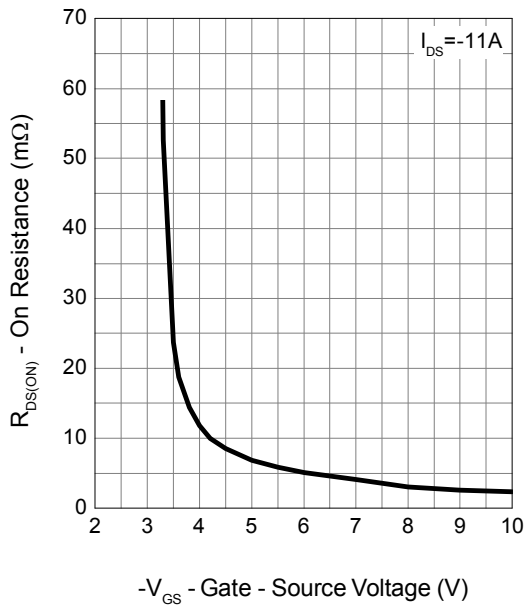
Output Characteristics



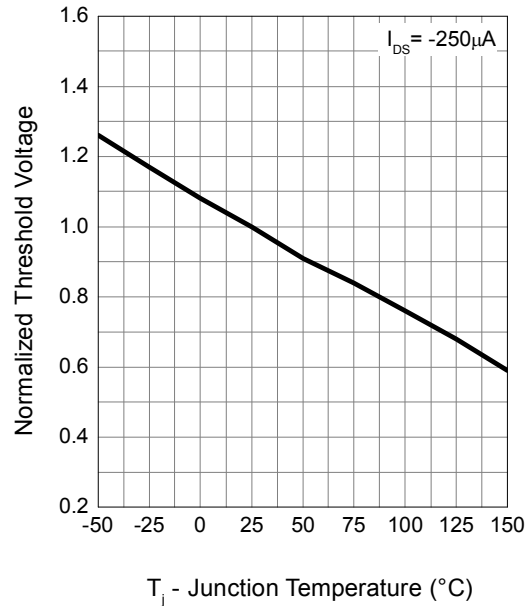
Drain-Source On Resistance



Gate-Source On Resistance

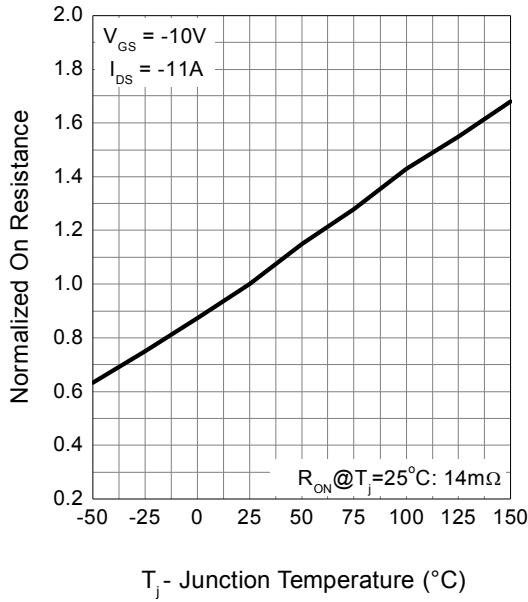


Gate Threshold Voltage

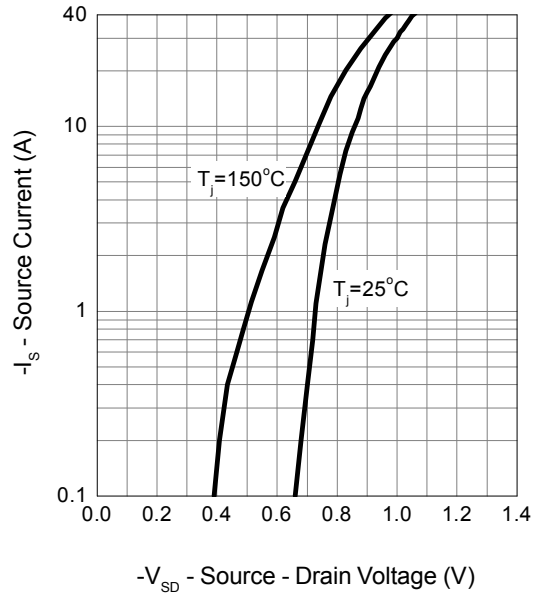




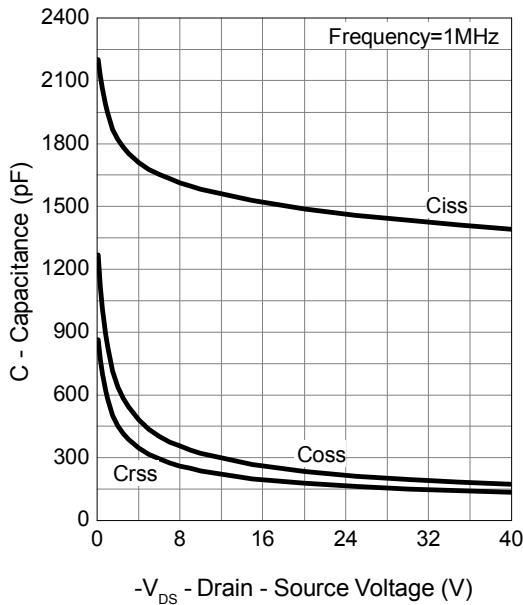
Drain-Source On Resistance



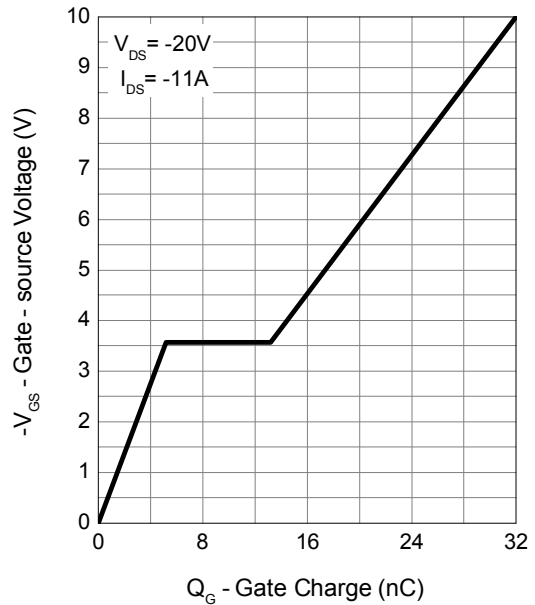
Source-Drain Diode Forward



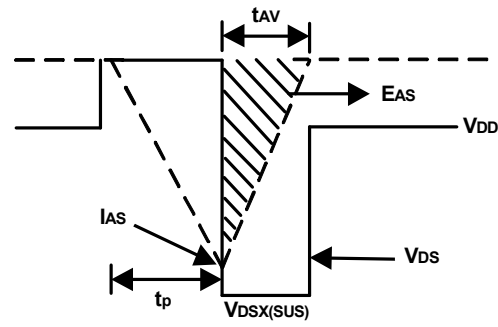
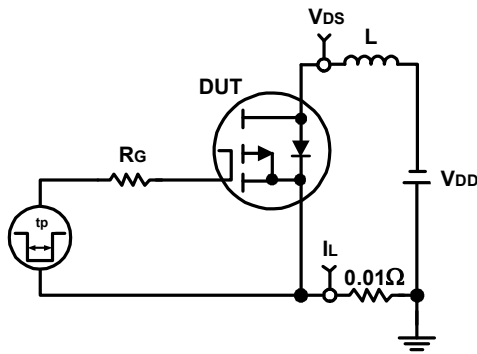
Capacitance



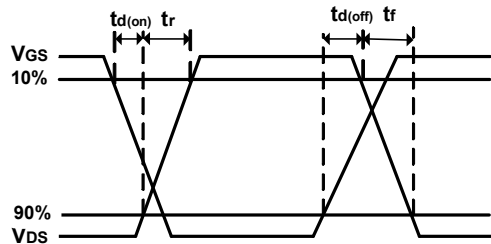
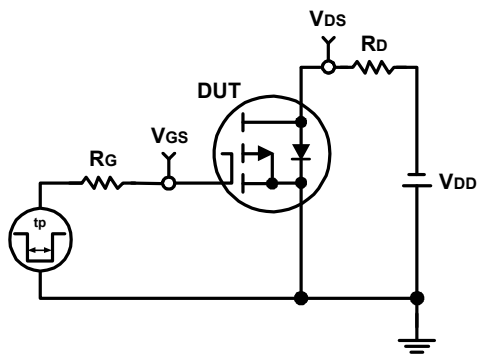
Gate Charge



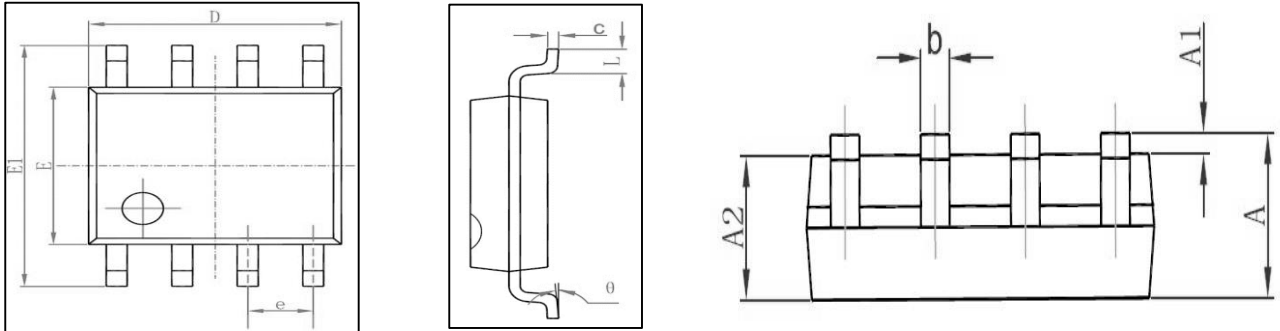
Avalanche Test Circuit and Waveforms



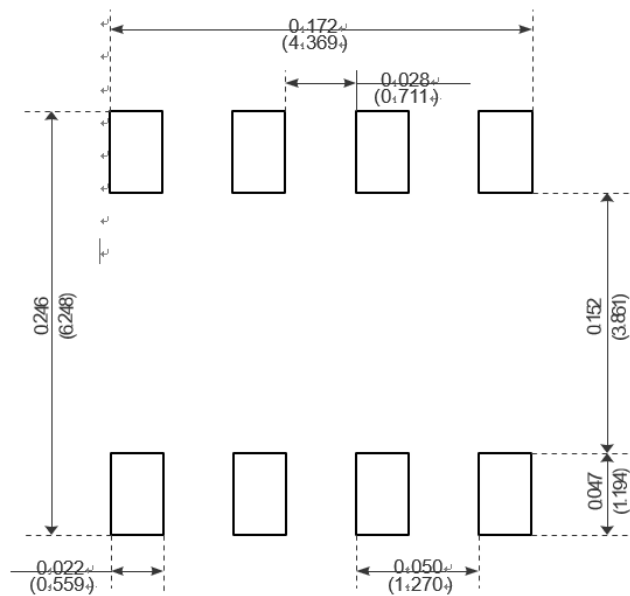
Switching Time Test Circuit and Waveforms



Package Mechanical Data-SOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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