
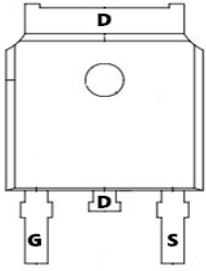




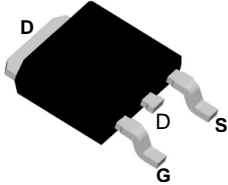
**TM50P02D**

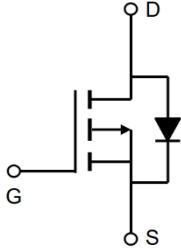
**P -Channel Enhancement Mosfet**

<p><b>General Description</b></p> <ul style="list-style-type: none"> <li>• Low <math>R_{DS(ON)}</math></li> <li>• RoHS and Halogen-Free Compliant</li> </ul> <p><b>Applications</b></p> <ul style="list-style-type: none"> <li>• Load switch</li> <li>• PWM</li> </ul>	<p><b>General Features</b></p> <p><math>V_{DS} = -20V</math> <math>I_D = -50A</math></p> <p><math>R_{DS(ON)} = 12m\Omega</math> (typ.) @ <math>V_{GS} = -4.5V</math></p> <p>100% UIS Tested 100% <math>R_g</math> Tested</p> 
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D:TO-252-3L





Marking: 50P02

**Absolute Maximum Ratings (TC=25°C unless otherwise noted)**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-50	A
$I_D @ T_C = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-25	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-68	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation <sup>3</sup>	38	W
$P_D @ T_C = 70^\circ C$	Total Power Dissipation <sup>3</sup>	18	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

**Thermal Data**

Symbol	Parameter	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	75	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup> (t ≤ 10s)	40	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	4.2	°C/W



## TM50P02D

## P -Channel Enhancement Mosfet

Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1mA$	---	-0.012	---	$V/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-4.5V, I_D=-10A$	---	12	18	m $\Omega$
		$V_{GS}=-2.5V, I_D=-8A$	---	17	20	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.4	-0.7	-1.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.94	---	mV/ $^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-15V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=-5V, I_D=-10A$	---	43	---	S
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-10V, V_{GS}=-4.5V, I_D=-10A$	---	35	---	nC
$Q_{gs}$	Gate-Source Charge		---	5.0	---	
$Q_{gd}$	Gate-Drain Charge		---	10	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-10V, V_{GS}=-4.5V,$ $R_G=3.3\Omega, I_D=-10A$	---	12.0	---	ns
$T_r$	Rise Time		---	40.0	---	
$T_{d(off)}$	Turn-Off Delay Time		---	30	---	
$T_f$	Fall Time		---	10	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	---	2800	---	pF
$C_{oss}$	Output Capacitance		---	690	---	
$C_{rss}$	Reverse Transfer Capacitance		---	590	---	

## Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	-50.0	A
$I_{SM}$	Pulsed Source Current <sup>2,4</sup>		---	---	---	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=-10A, dI/dt=100A/\mu s,$	---	27	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	17.8	---	nC

Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
3. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



TM50P02D

P-Channel Enhancement Mosfet

Typical Characteristics

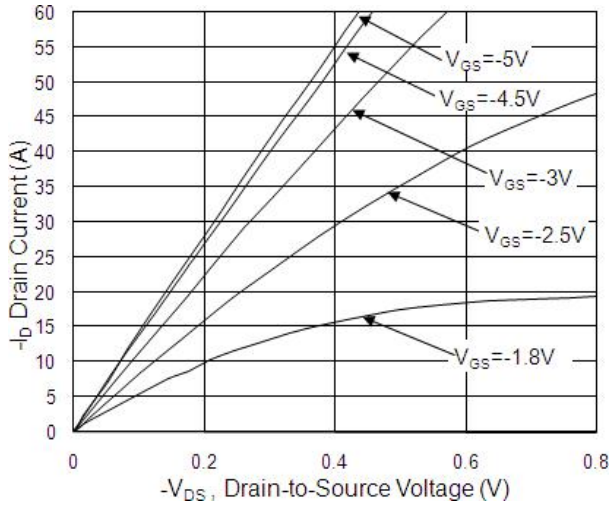


Fig.1 Typical Output Characteristics

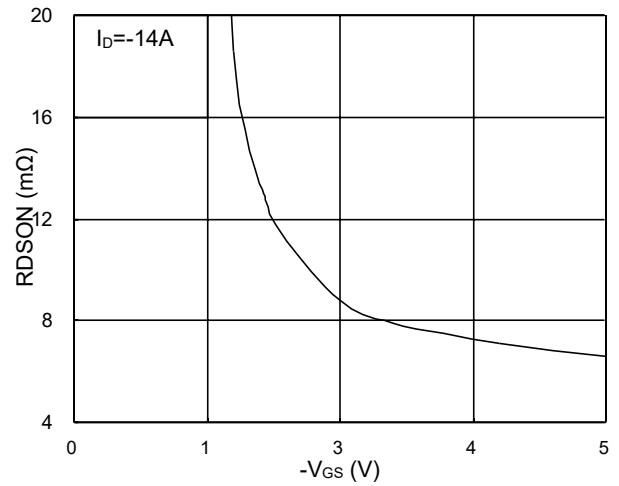


Fig.2 On-Resistance vs. G-S Voltage

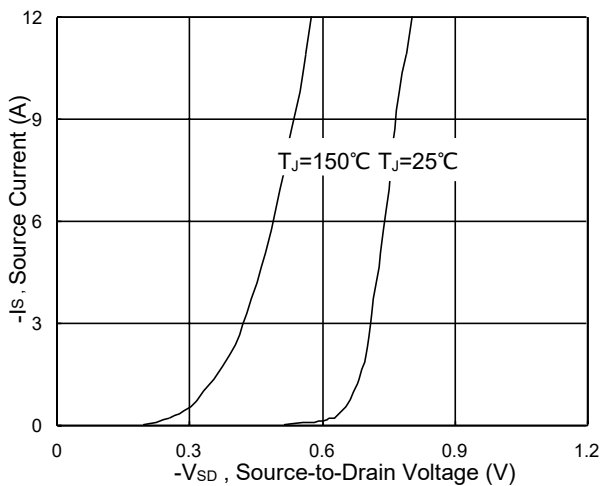


Fig.3 Forward Characteristics of Reverse

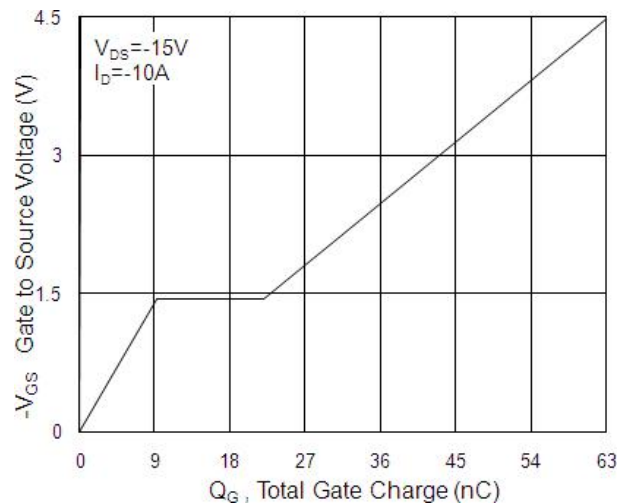


Fig.4 Gate-charge Characteristics

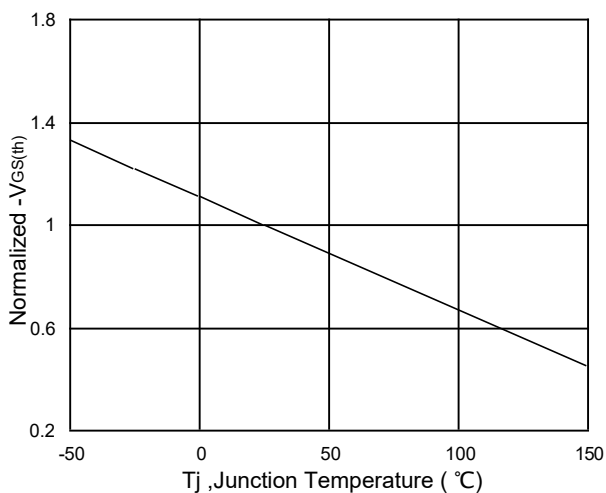


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

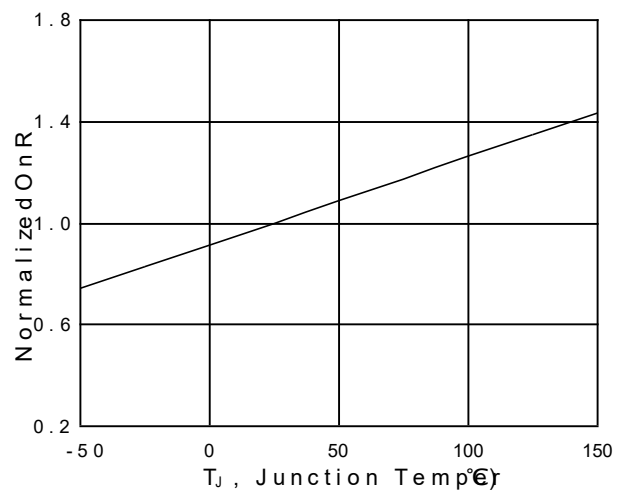


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$



# TM50P02D

# P-Channel Enhancement Mosfet

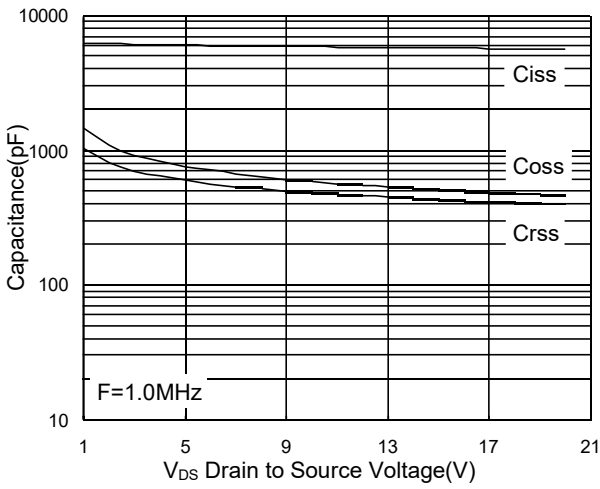


Fig.7 Capacitance

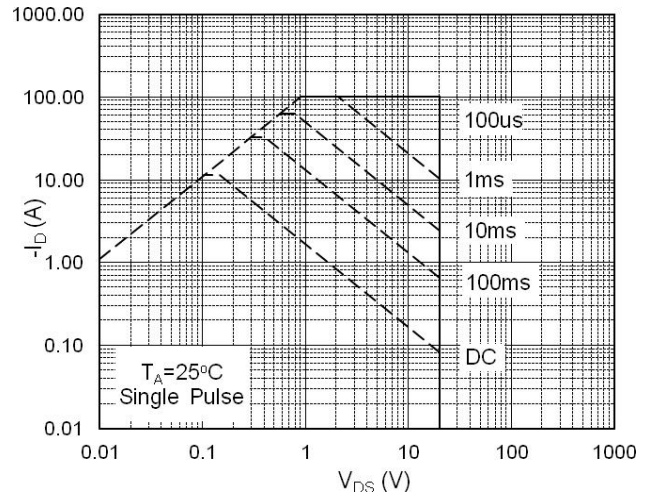


Fig.8 Safe Operating Area

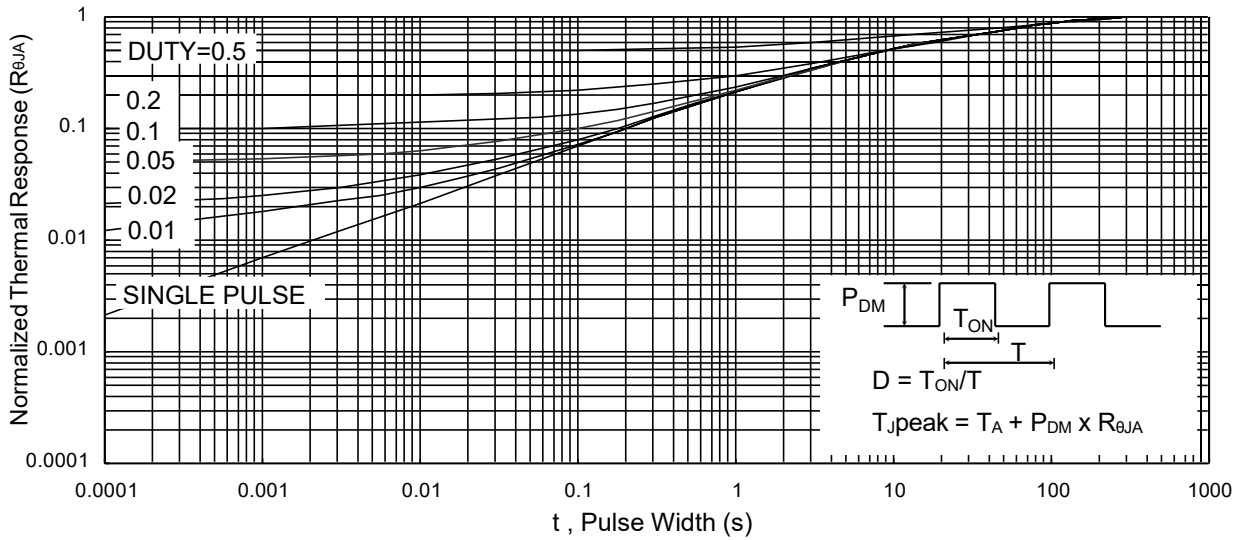


Fig.9 Normalized Maximum Transient Thermal Impedance

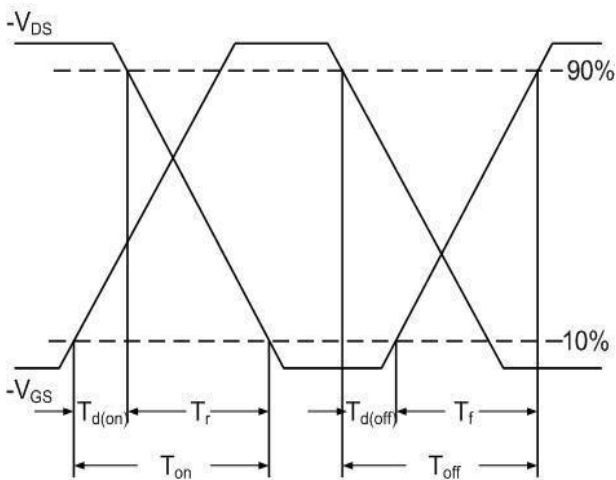


Fig.10 Switching Time Waveform

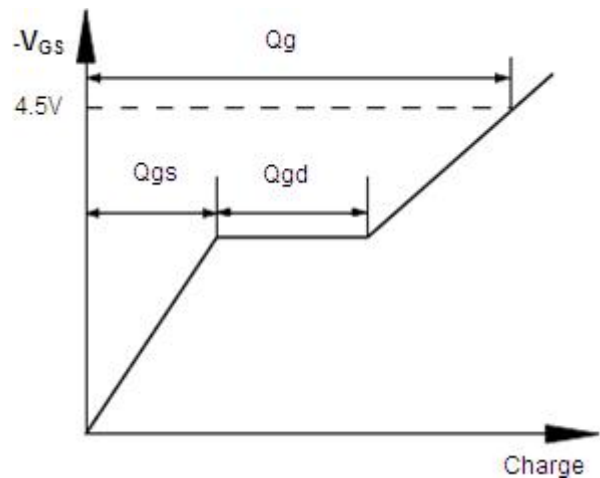
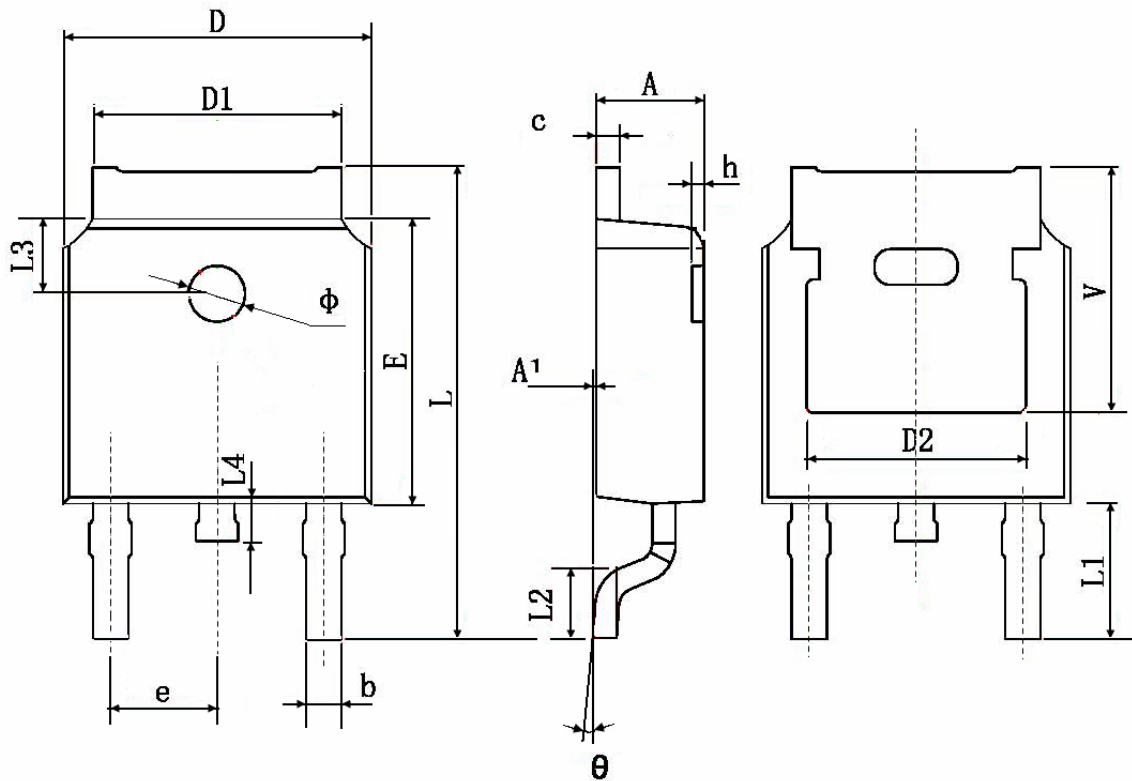


Fig.11 Gate Charge Waveform

## Package Mechanical Data: TO-252-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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