

# TSA50N20MK 200V N-Channel MOSFET

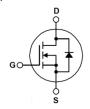
#### **General Description**

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

#### **Features**

- 50A,200V,Max.R<sub>DS(on)</sub>=0.038 $\Omega$  @ V<sub>GS</sub> =10V
- Low gate charge
- High ruggedness
- Fast switching
- 100% avalanche tested
- · Improved dv/dt capability



### **Absolute Maximum Ratings**

T<sub>J</sub>=25°C unless otherwise specified

<b>Absolute Maximum Ratings</b> $T_C = 25^{\circ}C$ , unless otherwise noted							
Parameter	Symbol	Value	Unit				
Drain-Source Voltage (note1)	V <sub>DSS</sub>	200	V				
Continuous Drain Current	I <sub>D</sub>	50	- A				
Pulsed Drain Current (note2)	I <sub>DM</sub>	200					
Gate-Source Voltage	$V_{GSS}$	±20	V				
Single Pulse Avalanche Energy (note2)	E <sub>AS</sub>	400	mJ				
Power Dissipation (T <sub>C</sub> = 25°C)	$P_{D}$	34	W/ºC				
Operating Junction and Storage Temperature Range	$T_J,T_stg$	-55~+150					

### **Thermal Resistance Characteristics**

Thermal Resistance					
Parameter	Symbol	Value	Unit		
Thermal Resistance, Junction-to-Case	R <sub>thJC</sub>	0.5	· °C/W		
Thermal Resistance, Junction-to-Ambient	R <sub>thJA</sub>	45			

## Electrical Characteristics $T_J=25^{\circ}C$ unless otherwise specified

			Value			
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static				•		
Drain-Source Breakdown Voltage	V(BR)DSS	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	200			V
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C			1	μΑ
Gate-Source Leakage	IGSS	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA
Gate-Source Threshold Voltage	VGS(th)	$V_{DS} = V_{GS}$ , $I_D = 250\mu A$	2		4	V
Drain-Source On-Resistance (Note4)	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A		0.030	0.038	Ω
Dynamic				•		
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0MHz$		3538		pF
Output Capacitance	C <sub>oss</sub>			657		
Reverse Transfer Capacitance	C <sub>rss</sub>			280		
Total Gate Charge	Qg	$V_{DD} = 160V, I_{D} = 50A,$ $V_{GS} 0 \text{ to } 10V$		244		nC
Gate-Source Charge	Q <sub>gs</sub>			16		
Gate-Drain Charge	Q <sub>gd</sub>			144		
Turn-on Delay Time	<sup>t</sup> d(on)	V <sub>DD</sub> = 100V, I <sub>D</sub> = 50A, VGS =10V.RG = 25Ω		53		
Turn-on Rise Time	t <sub>r</sub>			65		ns
Turn-off Delay Time	<sup>t</sup> d(off)		-	689		
Turn-off Fall Time	t <sub>f</sub>			230		
Drain-Source Body Diode Characte	ristics					
Continuous Source Current	ISD	Integral PN-diode in MOSFET			50	А
Pulsed Source Current	I <sub>SM</sub>				200	
Body Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V			1.5	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0V,I <sub>F</sub> = 10A,		208		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di <sub>F</sub> /dt =100A /μs		2.04		μC

#### NOTES

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature
- 2. L = 10mH,  $V_{DD}$  = 50V,  $R_G$  = 25  $\Omega$ , Starting  $T_J$  = 25  $^{\circ}$ C
- 3. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 1%

## **Typical Characteristics** $T_J = 25^{\circ}$ C, unless otherwise noted

Figure 1. Output Characteristics (T<sub>J</sub> = 25°C)

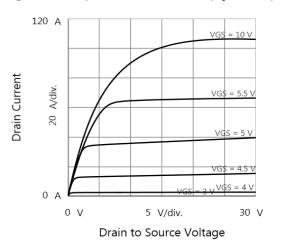


Figure 2. Transfer Characteristics

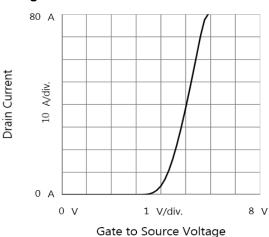
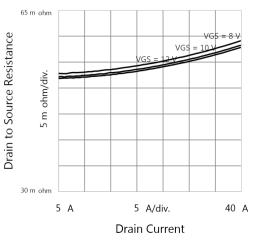


Figure 3. Drain to Source Resistance vs. Drain Current Figure 4. Drain to Source Resistance vs. Gate to Source Voltage



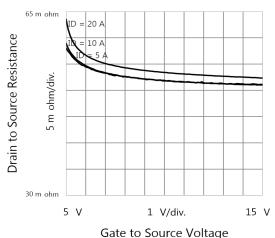


Figure 5. Drain to Source Voltage vs. Gate to Source Voltage

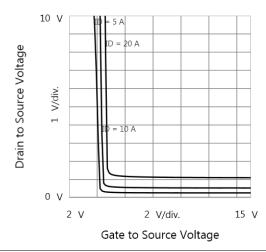
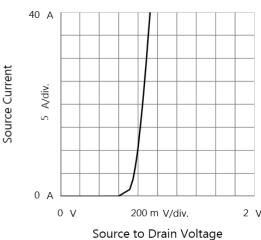


Figure 6. Body Diode Forward Characteristics



## **Typical Characteristics** $T_J = 25^{\circ}$ C, unless otherwise noted

Gate to Source Voltage

Figure 7. Capacitance

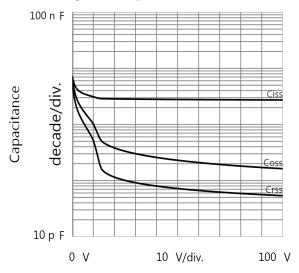
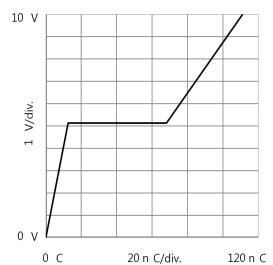
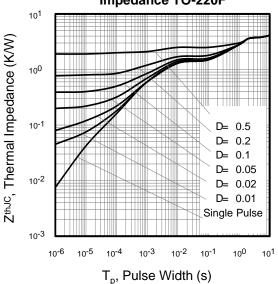


Figure 8. Gate Charge

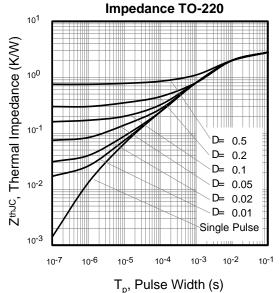


Drain to Source Voltage

Figure 9. Transient Thermal Impedance TO-220F



Gate Charge
Figure 10. Transient Thermal



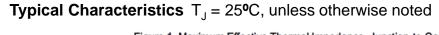


Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case **Duty Factor** 1.000 =50% -20% Z<sub>0,JC</sub>, Thermal Impedance 10% 0.100 5% (Normalized) 0.010 NOTES: DUTY FACTOR: D=t1/t2 PEAK T<sub>J</sub>=P<sub>DM</sub> x Z<sub>0</sub>JC x R<sub>0</sub>JC+T<sub>C</sub> 0.001 1E-05 1E-04 1E-03 1E-02 1E-01 1E+00 1E+01 t<sub>n</sub>, Rectangular Pulse Duration (s)

Figure 2. Maximum Power Dissipation vs Case Temperature

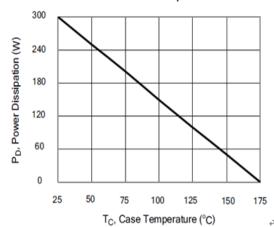


Figure 4. Typical Output Characteristics

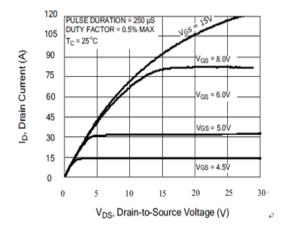


Figure3. Maximum Continuous Drain Current vs Case Temperature

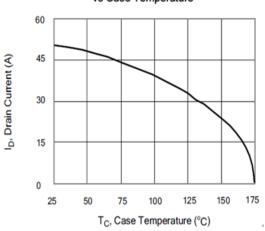
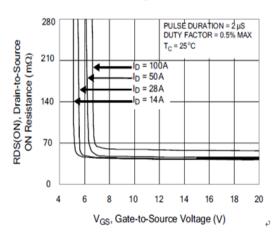
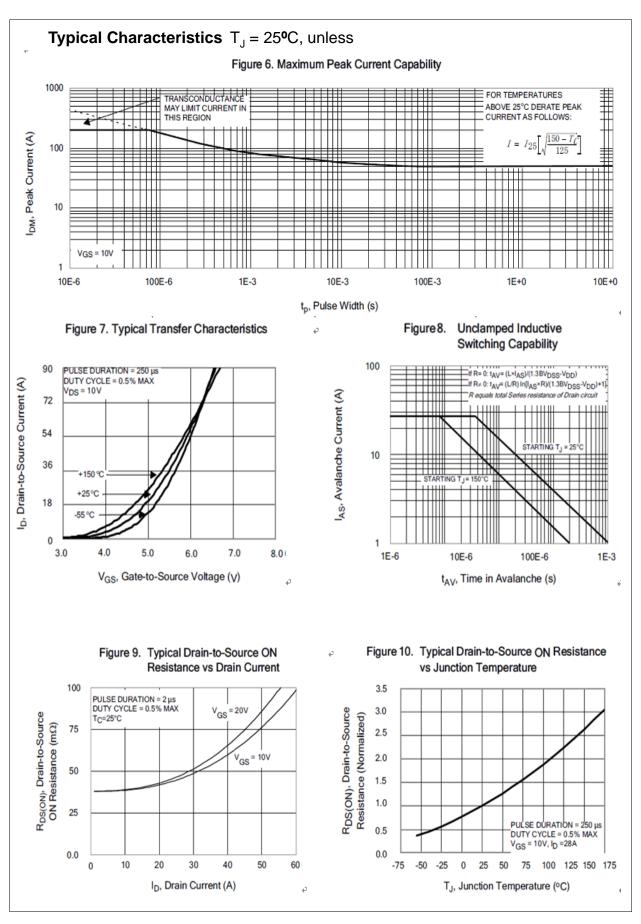


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current





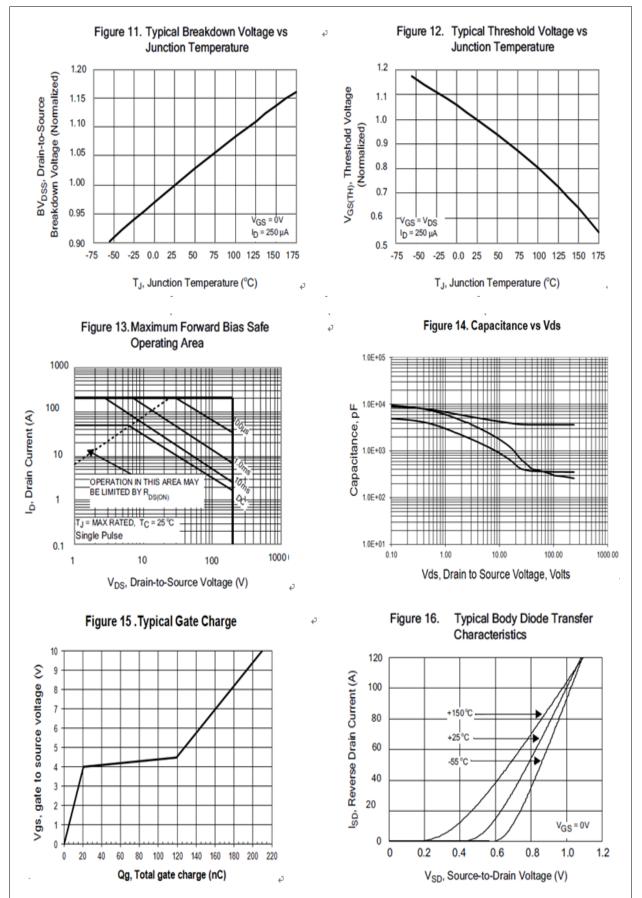


Figure A: Gate Charge Test Circuit and

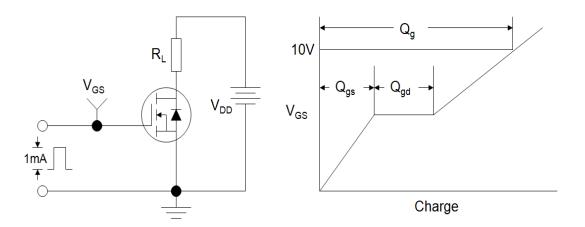


Figure B: Resistive Switching Test Circuit and Waveform

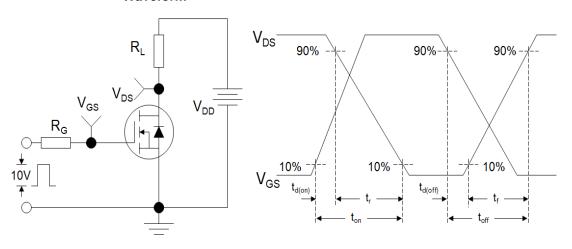
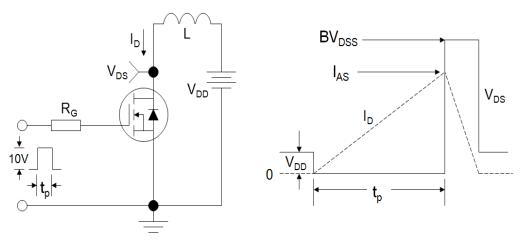


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



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