# TSF16N25M

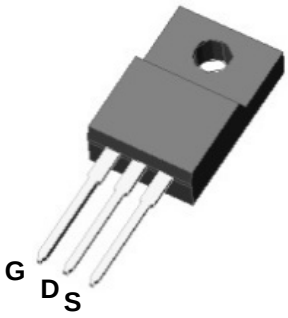
## 250V N-Channel MOSFET

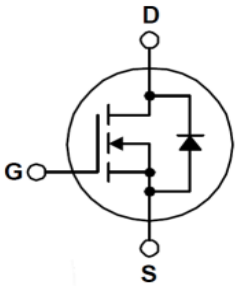
**General Description**

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

### Features

• 16A,250V,Max.$R_{DS(on)}$=0.25Ω @ $V_{GS}$ =10V




## Absolute maximum ratings ($T_C$=25°C unless otherwise noted)

| Characteristic | Symbol | | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | $V_{DSS}$ | | 250 | V |
| Gate-source voltage | $V_{GSS}$ | | ±30 | V |
| Drain current (DC) * | $I_D$ | $T_C$=25℃ | 16 | A |
| | | $T_C$=100℃ | 7.2 | A |
| Drain current (Pulsed) * | $I_{DM}$ | | 64 | A |
| Power dissipation | $P_D$ | | 50 | W |
| Avalanche current (Single) ② | $I_{AS}$ | | 16 | A |
| Single pulsed avalanche energy ② | $E_{AS}$ | | 480 | mJ |
| Avalanche current (Repetitive) ① | $I_{AR}$ | | 16 | A |
| Repetitive avalanche energy ① | $E_{AR}$ | | 13.9 | mJ |
| Junction temperature | $T_J$ | | 150 | °C |
| Storage temperature range | $T_{stg}$ | | -55~150 | |

* Limited by maximum junction temperature

| Characteristic | | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Thermal resistance | Junction-case | $R_{th(J-C)}$ | - | 2.5 | ℃/W |
| | Junction-ambient | $R_{th(J-A)}$ | - | 62.5 | |

## Electrical Characteristics ($T_C$=25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | $BV_{DSS}$ | $I_D$=250uA, $V_{GS}$=0V | 250 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $I_D$=250uA, $V_{DS}$=$V_{GS}$ | 2.0 | - | 4.0 | V |
| Drain-source cut-off current | $I_{DSS}$ | $V_{DS}$=250V, $V_{GS}$=0V | - | - | 1 | uA |
| Gate leakage current | $I_{GSS}$ | $V_{DS}$=0V, $V_{GS}$=±30V | - | - | ±100 | nA |
| Drain-source on-resistance ④ | $R_{DS(on)}$ | $V_{GS}$=10V, $I_D$=8.0A | - | 0.22 | 0.25 | Ω |
| Forward transfer conductance ④ | $g_{fs}$ | $V_{DS}$=10V, $I_D$=8.0A | - | 10.5 | - | S |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0V, $V_{DS}$=25V f=1 MHz | - | 968 | 1275 | pF |
| Output capacitance | $C_{oss}$ | | - | 204 | 278 | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 49 | 64 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=125V, $I_D$=16A $R_G$=25Ω ③④ | - | 15 | - | ns |
| Rise time | $t_r$ | | - | 45 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 50 | - | |
| Fall time | $t_f$ | | - | 50 | - | |
| Total gate charge | $Q_g$ | $V_{DS}$=200V, $V_{GS}$=10V $I_D$=16A ③④ | - | 45 | 50 | nC |
| Gate-source charge | $Q_{gs}$ | | - | 7.1 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 5.9 | - | |

## Source-Drain Diode Ratings and Characteristics ($T_C$=25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Source current (DC) | $I_S$ | Integral reverse diode in the MOSFET | - | - | 16 | A |
| Source current (Pulsed) ① | $I_{SM}$ | | - | - | 64 | |
| Forward voltage ④ | $V_{SD}$ | $V_{GS}$=0V, $I_S$=16A | - | - | 1.4 | V |
| Reverse recovery time | $t_{rr}$ | $I_S$=16A, $V_{GS}$=0V $dI_F/dt$=100A/us | - | 208 | - | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 2.63 | - | uC |

Note ;

① Repetitive rating : Pulse width limited by maximum junction temperature

② L=3.0mH, $I_{AS}$=16A, $V_{DD}$=50V, $R_G$=25Ω, Starting $T_J$=25℃

③ Pulse Test : Pulse width≤300us, Duty cycle≤2%

④ Essentially independent of operating temperature

# Electrical Characteristic Curves

**Fig. 1 $I_D$ - $V_{DS}$**

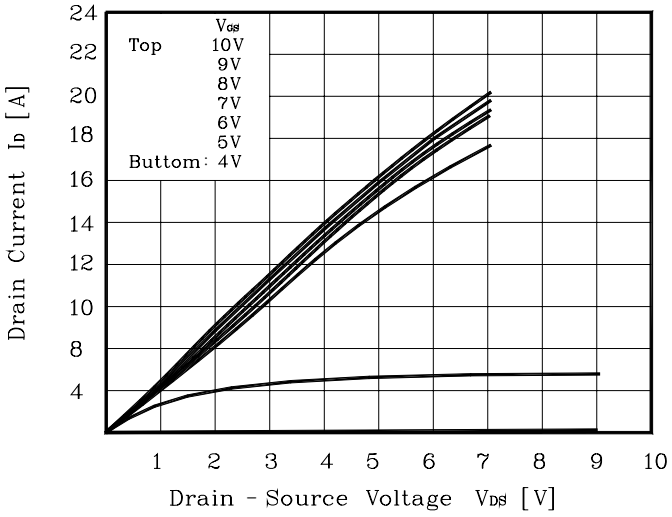



**Fig. 2 $I_D$ - $V_{GS}$**

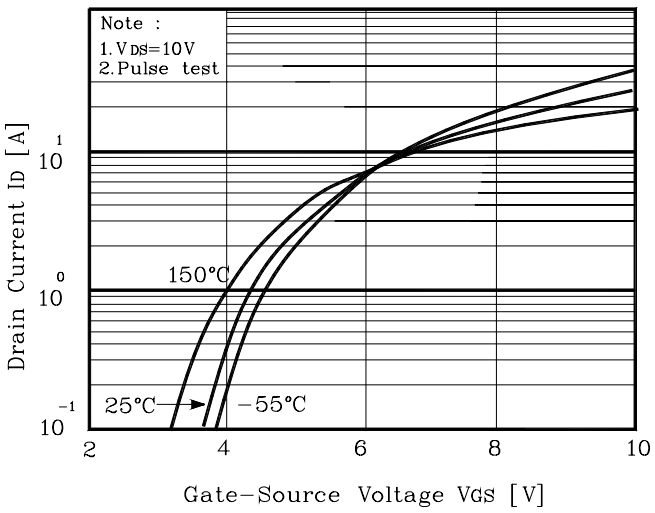



**Fig. 3 $R_{DS(on)}$ - $I_D$**

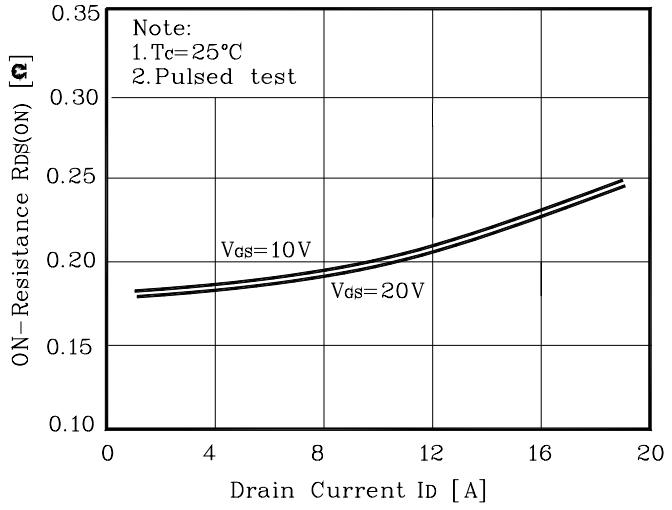



**Fig. 4 $I_S$ - $V_{SD}$**

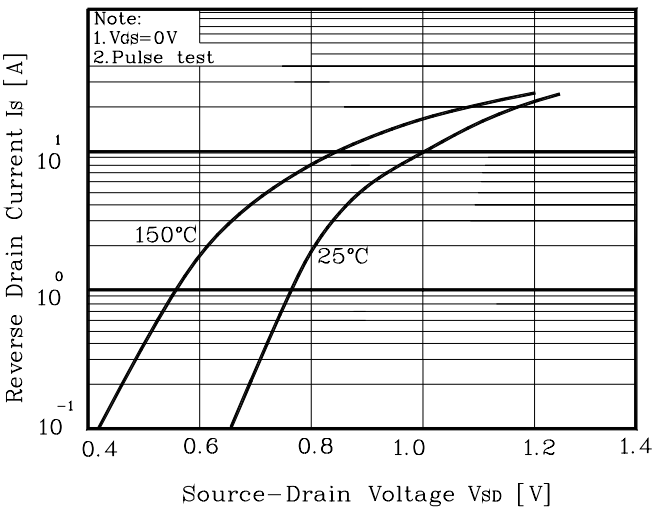



**Fig. 5 Capacitance - $V_{DS}$**

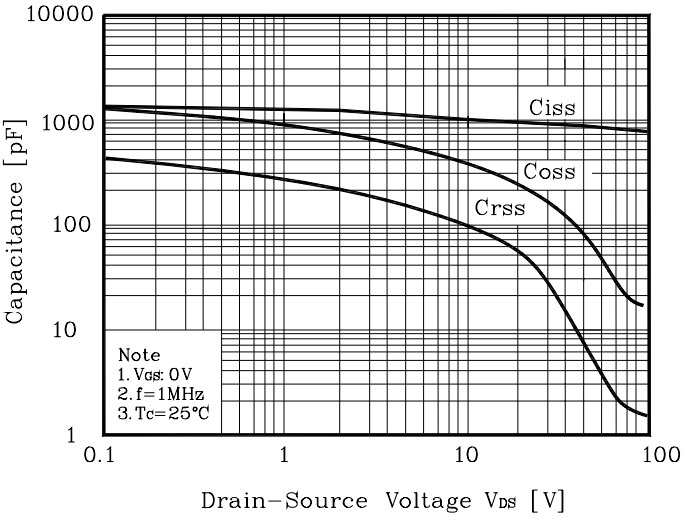



**Fig. 6 $V_{GS}$ - $Q_G$**

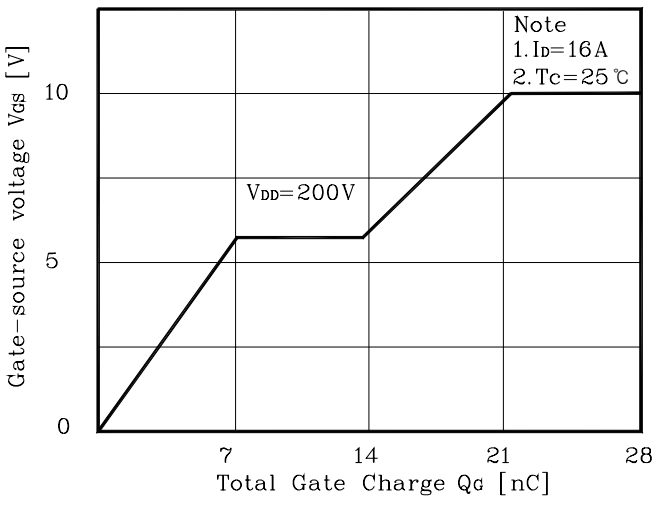


**Fig. 7 $V_{DSS}$ - $T_J$**

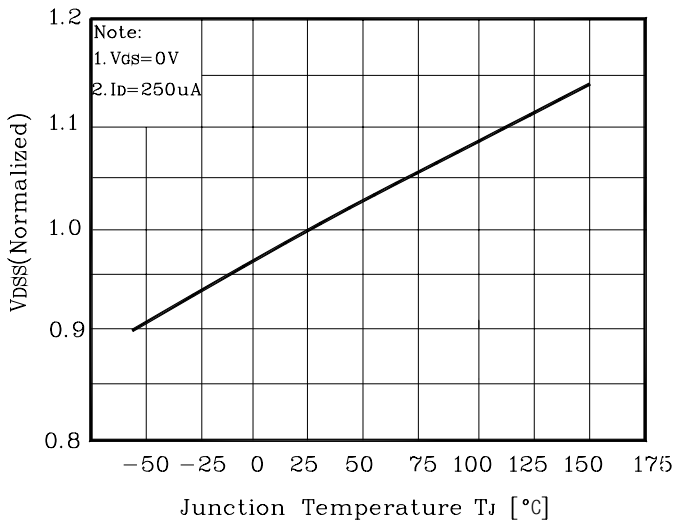



**Fig. 8 $R_{DS(on)}$ - $T_J$**

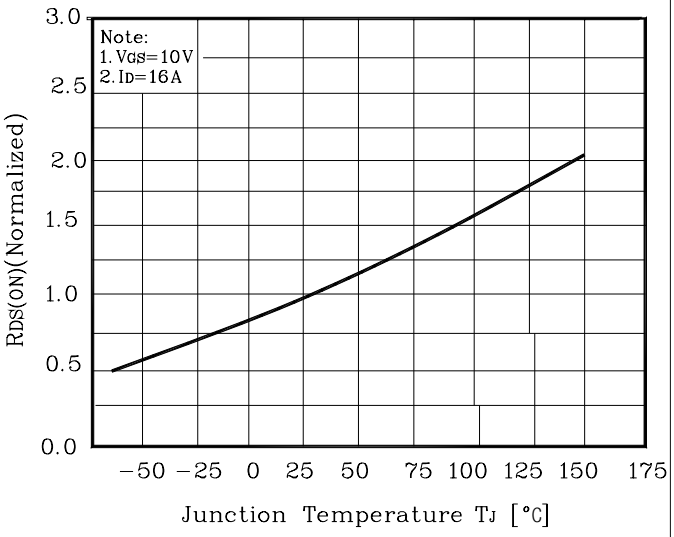



**Fig. 9 $I_D$ - $T_C$**

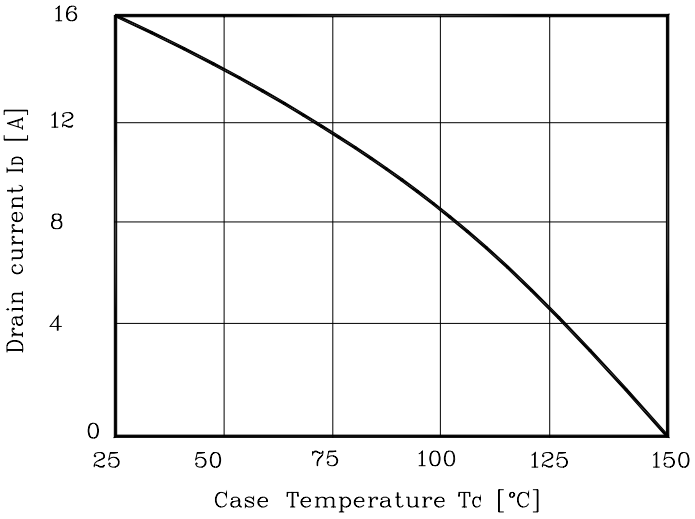



**Fig. 10 Safe Operating Area**

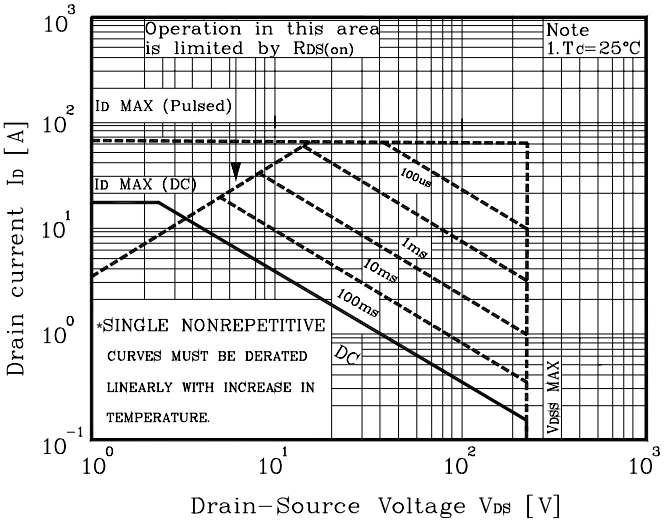


**Fig. 11 Gate Charge Test Circuit & Waveform**

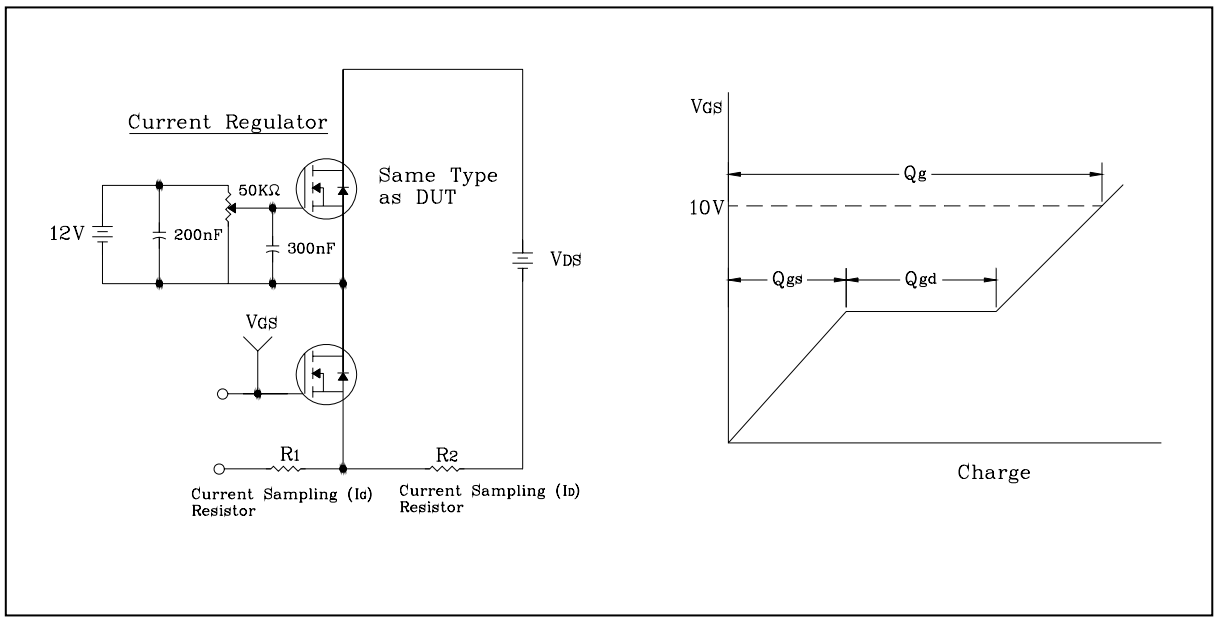



**Fig. 12 Resistive Switching Test Circuit & Waveform**

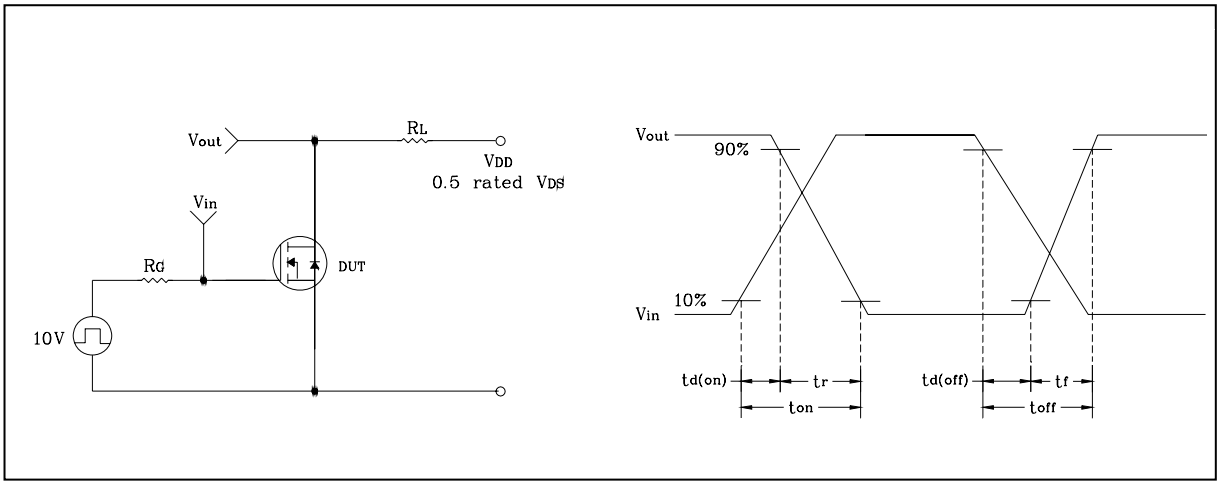



**Fig. 13 $E_{AS}$ Test Circuit & Waveform**

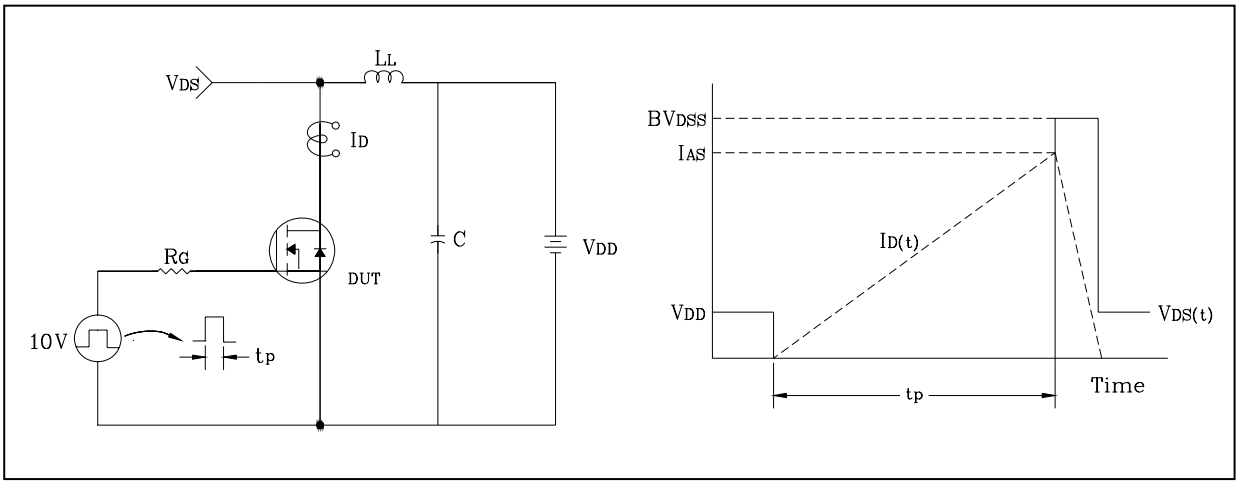
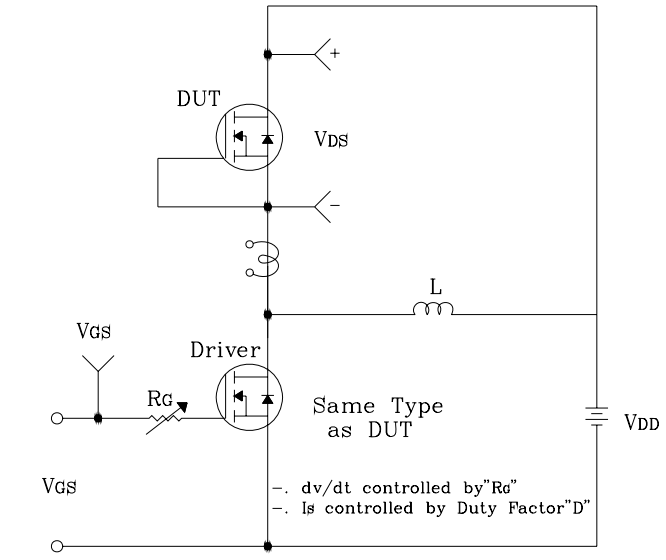
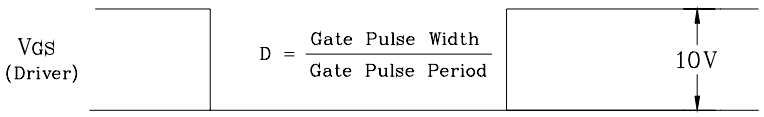
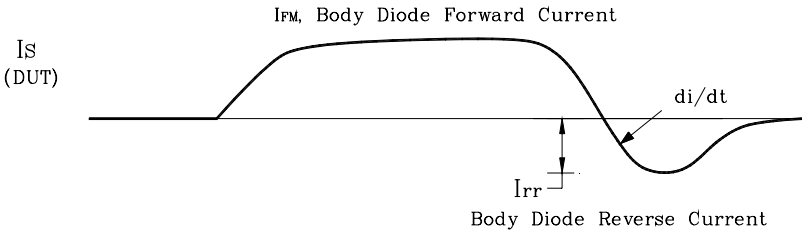
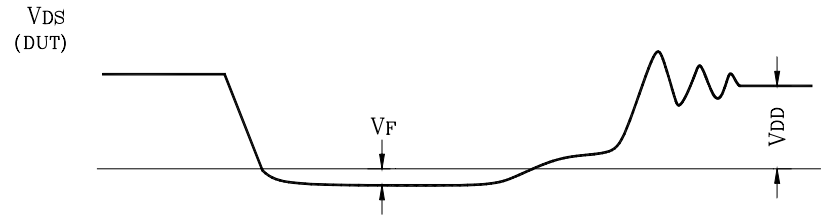


**Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform**



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