



TSP50N25M

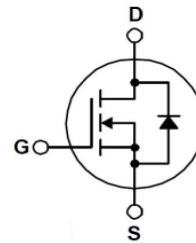
250V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

- 50A, 250V, Max. RDS(on)=0.078Ω @ VGS =10V
 - ◆ Fast switching speed
 - ◆ Low gate charge
 - ◆ RoHS compliant device
- Applications
- ◆ Synchronous Rectification
 - ◆ Power Management in Inverter System



Absolute Maximum Ratings T_c=25°C unless otherwise specified

Symbol	Parameter	Value	Units
V _{DSS}	Drain-Source Voltage	250	V
V _{GS}	Gate-Source Voltage	± 30	V
I _D	Drain Current	T _c = 25°C	50
		T _c = 100°C	31.6
I _{DM}	Pulsed Drain Current	200	A
E _{AS}	Single Pulsed Avalanche Energy (Note 1)	1250	mJ
I _{AS}	Single avalanche current	20	A
P _D	Power Dissipation (T _c = 25°C)	194	W
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C

* Limited only maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	--	0.64	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	62.0	°C/W

Electrical Characteristics $T_c=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	--	4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$	--	0.065	0.078	Ω
Rg	Internal gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	--	0.8	--	Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	250	--	--	V
I_{DSS}	Drain-source cut-off current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSS}	Gate leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$	--	--	± 100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ (Note 3,4)	--	5521	--	pF
C_{oss}	Output Capacitance		--	395	--	pF
C_{rss}	Reverse Transfer Capacitance		--	42	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DD} = 125\text{ V}, I_D = 50\text{ A},$ $R_G = 25\text{ }\Omega, V_{GS}=10\text{ V}$ (Note 3,4)	--	55	--	ns
t_r	Turn-On Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	212	--	ns
t_f	Turn-Off Fall Time		--	31	--	ns
Q_g	Total Gate Charge	$V_{DS} = 200\text{ V}, I_D = 50\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 3,4)	--	76	--	nC
Q_{gs}	Gate-Source Charge		--	20	--	nC
Q_{gd}	Gate-Drain Charge		--	25	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	50	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	200		
V_{SD}	Source-Drain Diode Forward Voltage	$I_{SD}=50\text{A}, V_{GS} = 0\text{ V}$	--	--	1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 50\text{ A}, V_{GS} = 0\text{ V}$ $di_f/dt = 100\text{ A}/\mu\text{s}$	--	271	--	ns
Q_{rr}	Reverse Recovery Charge	(Note 3,4)	--	2.4	--	μC

NOTES:

- 1.L=5mH, IAS=20 VDD=50V, Starting $T_J=25\text{ }^\circ\text{C}$
- 2.Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
3. Essentially independent of operating temperature typical characteristics
- 4.Guaranteed by design, not subject to production testing.

Typical Electrical Characteristics Curves

Fig. 1 $I_D - V_{DS}$

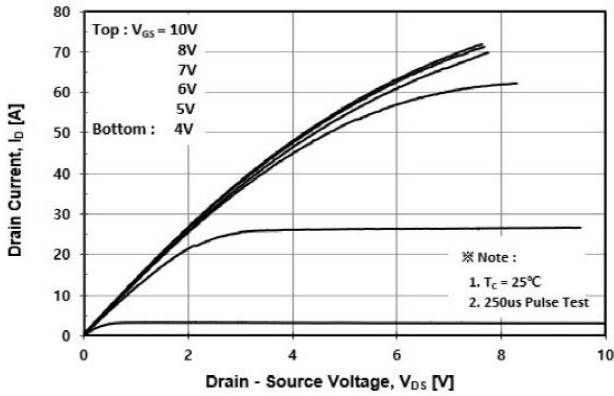


Fig. 2 $I_D - V_{GS}$

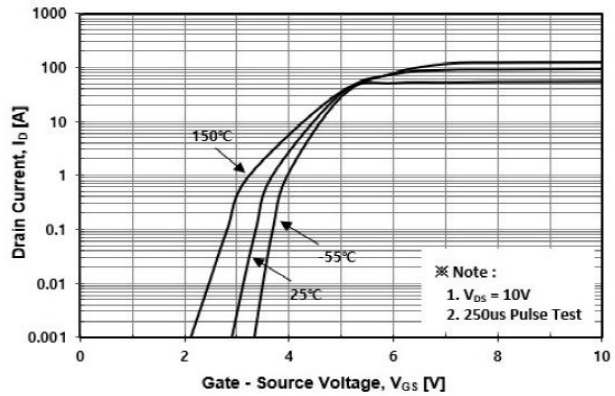


Fig. 3 $R_{DS(ON)} - I_D$

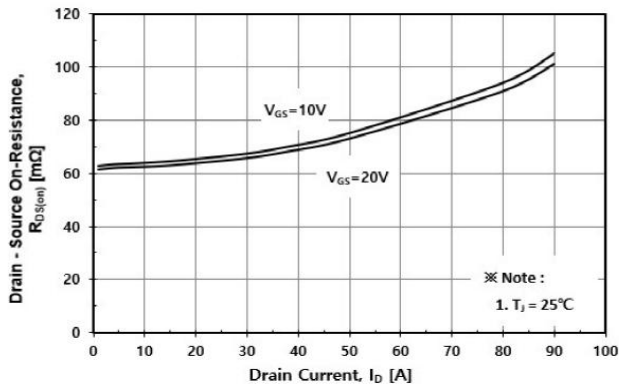


Fig. 4 $I_S - V_{SD}$

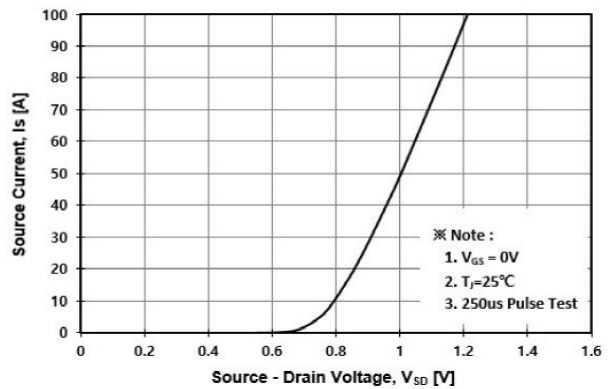


Fig. 5 Capacitance - V_{DS}

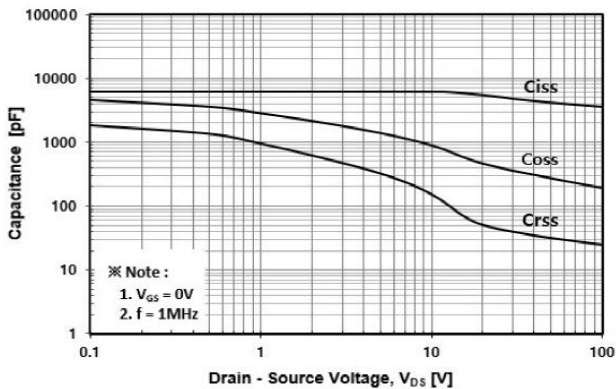
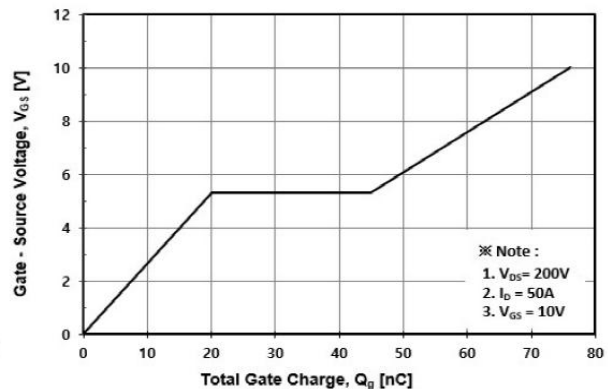


Fig. 6 $V_{GS} - Q_G$



Typical Electrical Characteristics Curves

Fig. 7 $BV_{DSS} - T_J$

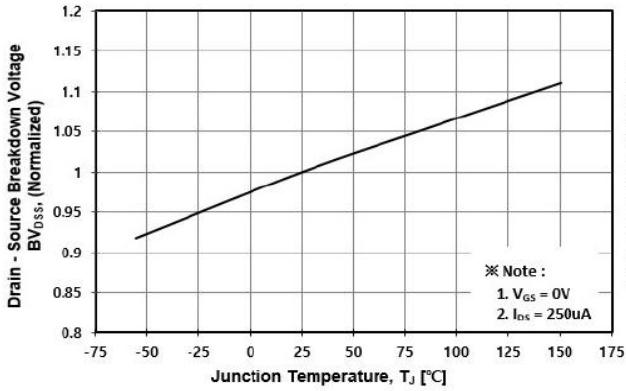


Fig. 8 $R_{DS(ON)} - T_J$

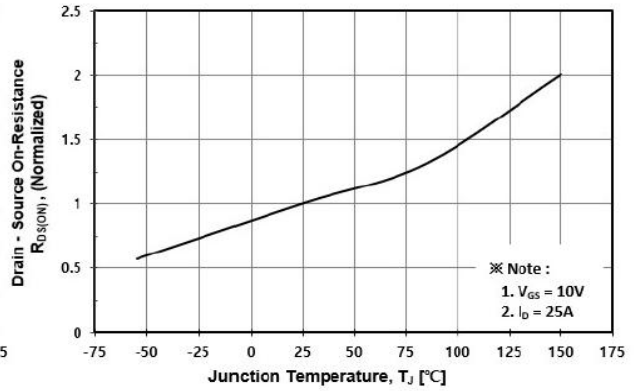


Fig. 9 $I_D - T_C$

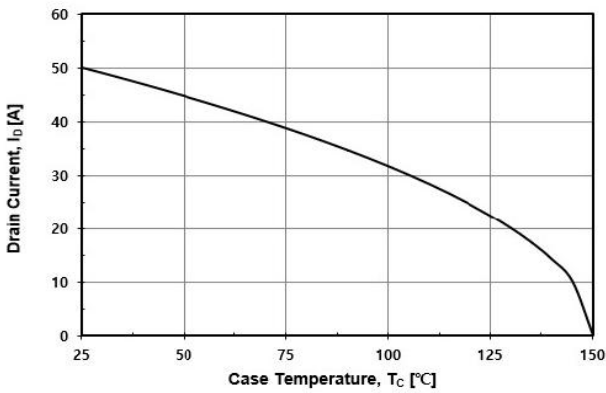


Fig. 10 Safe Operating Area

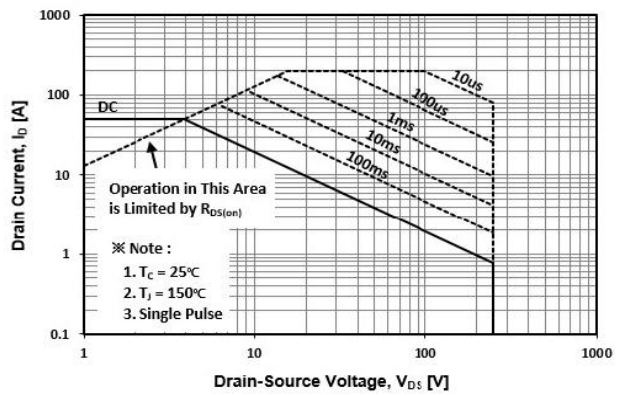


Fig. 11 Transient Thermal Impedance

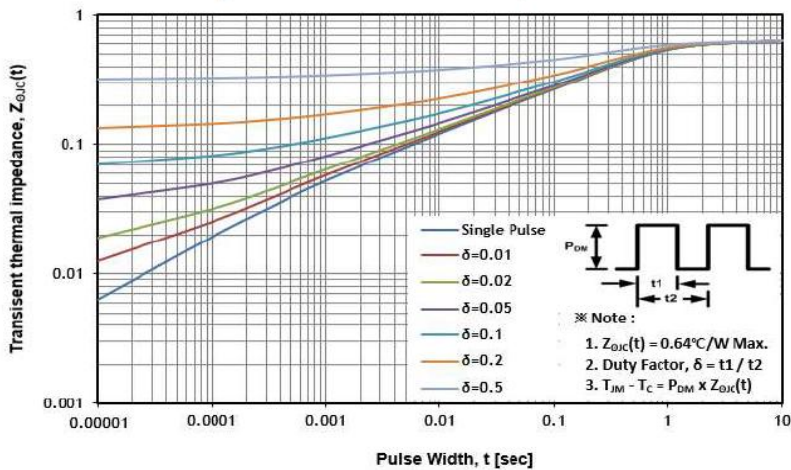


Fig. 12 Gate Charge Test Circuit & Waveform

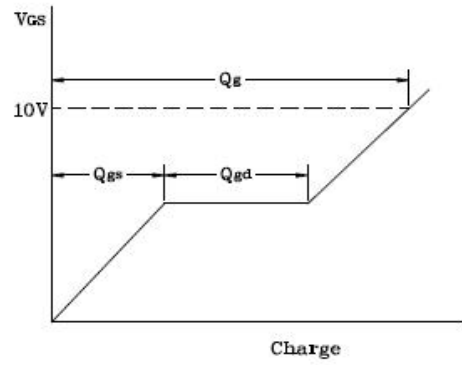
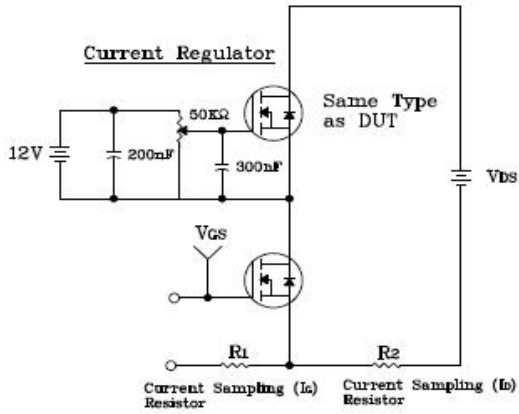


Fig. 13 Resistive Switching Test Circuit & Waveform

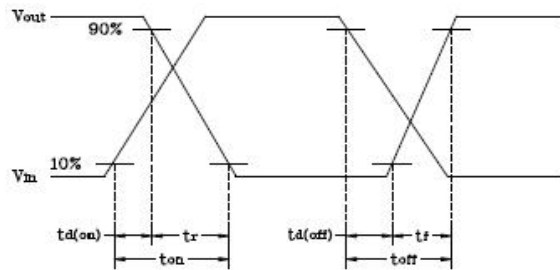
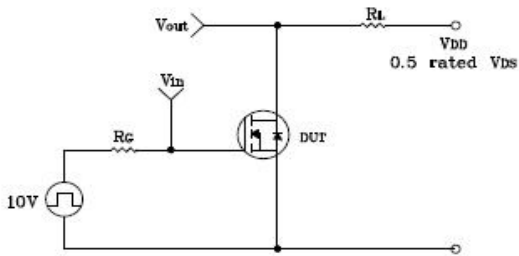


Fig. 14 EAS Test Circuit & Waveform

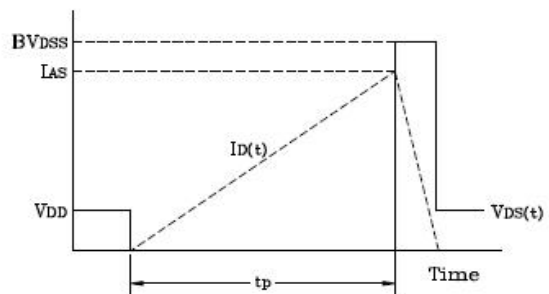
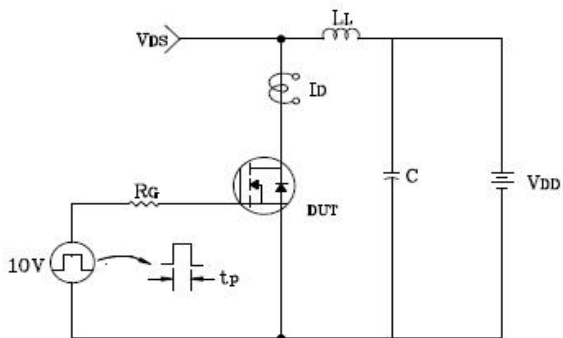
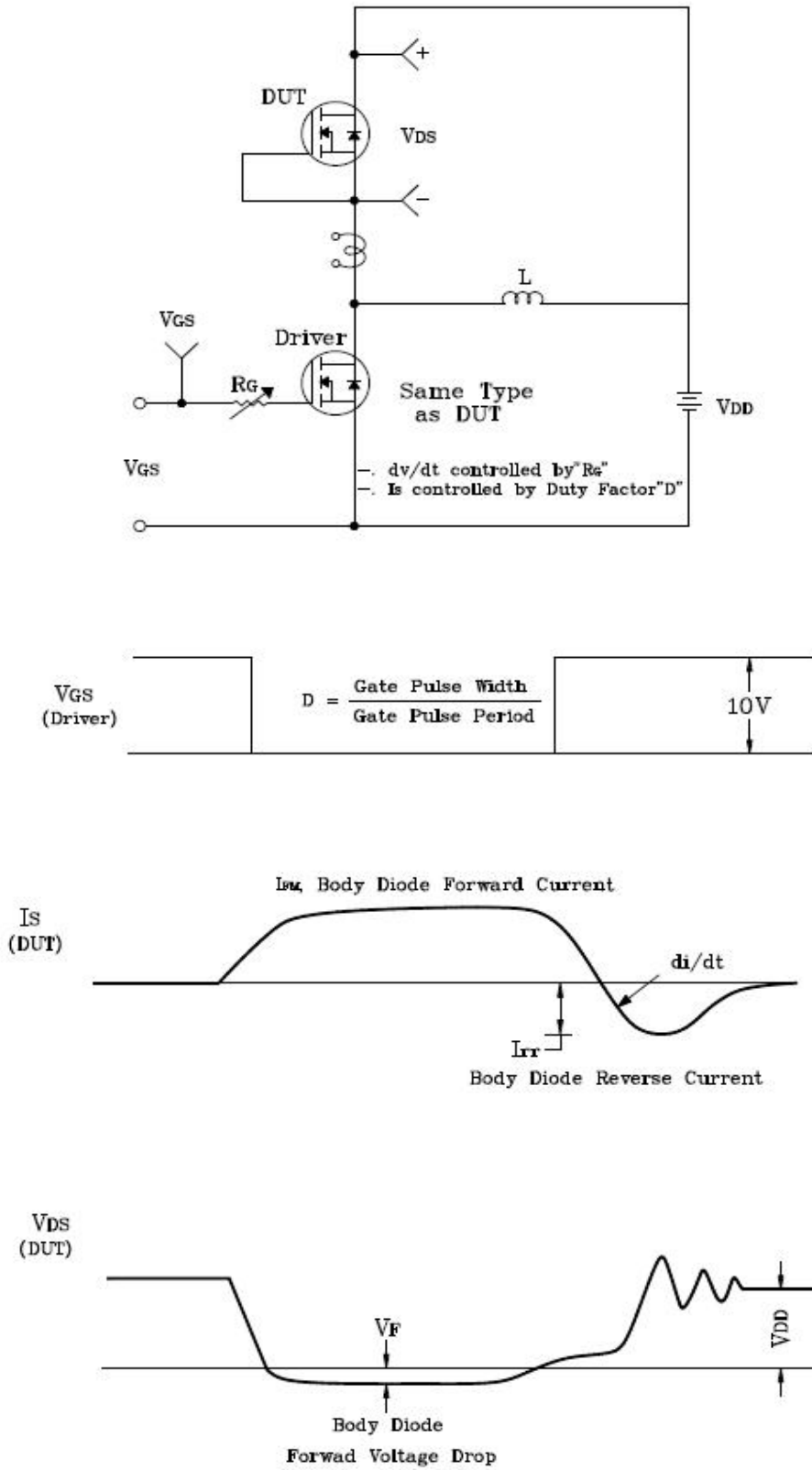


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



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