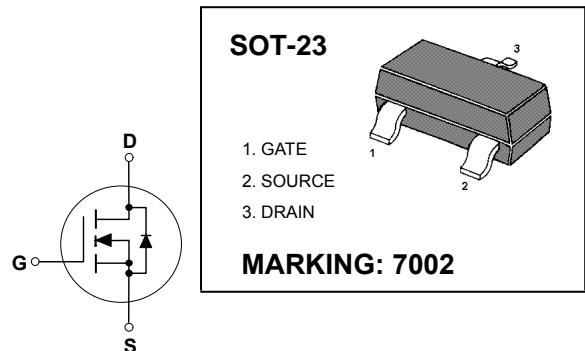


2N7002

N-Channel Enhancement Mode Field Effect Transistor

Description

These N-channel enhancement mode field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while providing rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400 mA DC and can deliver pulsed currents up to 2 A. These products are particularly suited for low-voltage, low-current applications, such as small servo motor control, power MOSFET gate drivers, and other switching applications.



Features

- High Density Cell Design for Low $R_{DS(ON)}$
- Voltage Controlled Small Signal Switch
- Rugged and Reliable
- High Saturation Current Capability

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1 \text{ M}\Omega$)	60	V
V_{GSS}	Gate-Source Voltage - Continuous	± 20	V
	Gate-Source Voltage - Non Repetitive ($t_p < 50 \mu\text{s}$)	± 40	
I_D	Maximum Drain Current - Continuous	115	mA
	Maximum Drain Current - Pulsed	800	
P_D	Maximum Power Dissipation Derated above 25°C	200	mW
		1.6	mW/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16-inch from Case for 10 Seconds	300	°C

Thermal Characteristics

Values are at $T_C = 25^\circ\text{C}$ unless otherwise noted.

	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	625	°C/W

Electrical Characteristics

Values are at $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BVDSS	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \mu\text{A}$	60			V
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_C = 125^\circ\text{C}$			0.5	mA
IGSSF	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
IGSSR	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
On Characteristics						
VGS(th)	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1	2.1	2.5	V
RDS(ON)	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$		1.2	7.5	Ω
		$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}, T_C = 100^\circ\text{C}$		1.7	13.5	
VDS(ON)	Drain-Source On-Voltage	$V_{GS} = 10 \text{ V}, I_D = 500 \text{ mA}$		0.6	3.75	V
		$V_{GS} = 5.0 \text{ V}, I_D = 50 \text{ mA}$		0.09	1.5	
ID(ON)	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} \geq 2 V_{DS(\text{on})}$	500	2700		mA
gFS	Forward Transconductance	$V_{DS} \geq 2 V_{DS(\text{on})}, I_D = 200 \text{ mA}$	80	320		mS
Dynamic Characteristics						
Ciss	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$		20	50	pF
Coss	Output Capacitance			11	25	
Crss	Reverse Transfer Capacitance			4	5	
ton	Turn-On Time	$V_{DD} = 30 \text{ V}, R_L = 150\Omega, I_D = 200 \text{ mA}, V_{GS} = 10 \text{ V}, R_{GEN} = 25\Omega$			20	ns
toff	Turn-Off Time	$V_{DD} = 30 \text{ V}, R_L = 150 \text{ } \Omega, I_D = 200 \text{ mA}, V_{GS} = 10 \text{ V}, R_{GEN} = 25\Omega$			20	ns
Drain-Source Diode Characteristics and Maximum Ratings						
Is	Maximum Continuous Drain-Source Diode Forward Current				115	mA
ISM	Maximum Pulsed Drain-Source Diode Forward Current				0.8	A
VSD	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 400 \text{ mA(1)}$		0.88	1.2	V

Note:

1. Pulse test : Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

Typical Characteristics

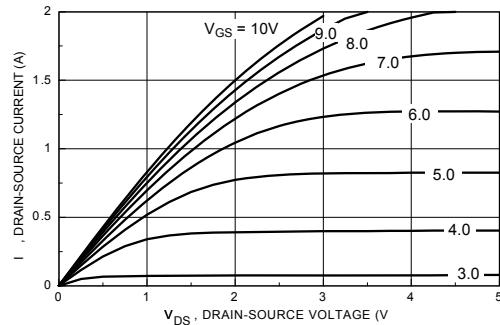


Figure 1. On-Region Characteristics

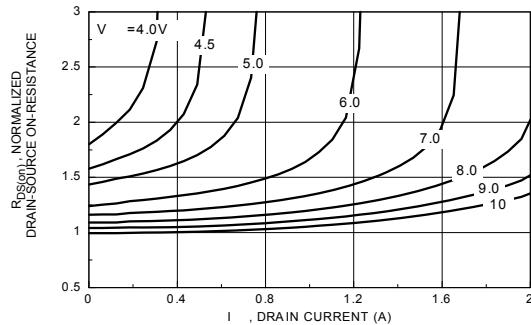


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

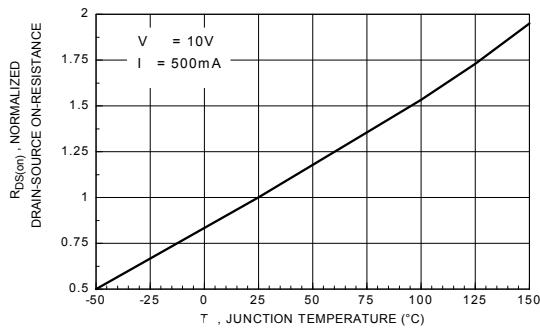


Figure 3. On-Resistance Variation with Temperature

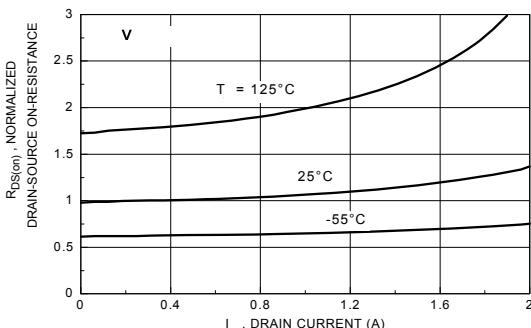


Figure 4. On-Resistance Variation with Drain Current and Temperature

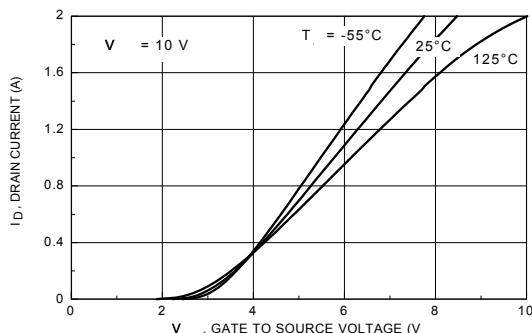


Figure 5. Transfer Characteristics

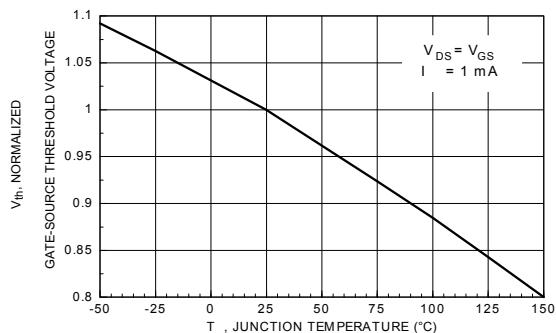


Figure 6. Gate Threshold Variation with Temperature

Typical Characteristics

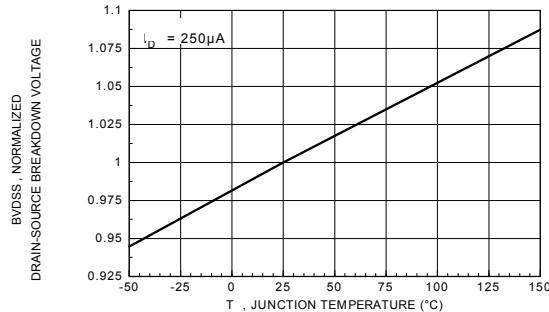


Figure 7. Breakdown Voltage Variation with Temperature

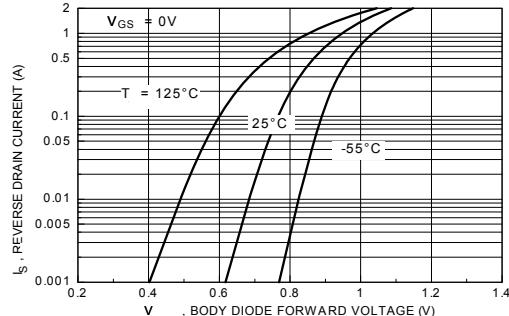


Figure 8. Body Diode Forward Voltage Variation with Temperature

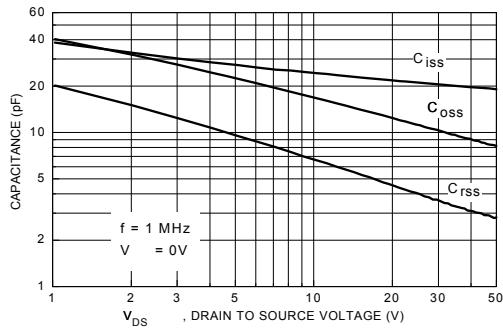


Figure 9. Capacitance Characteristics

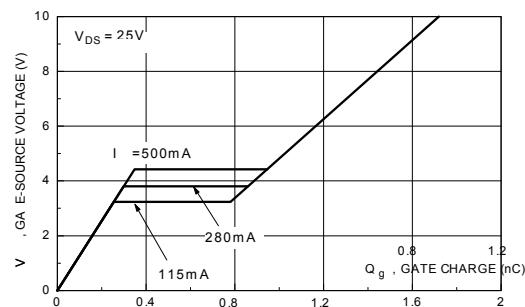


Figure 10. Gate Charge Characteristics

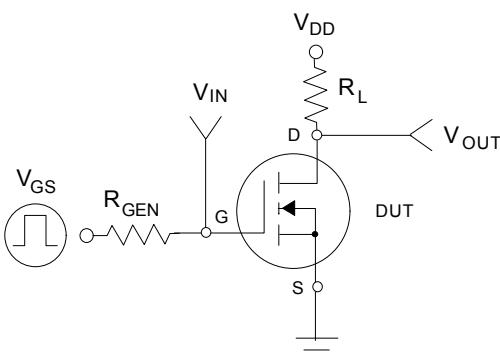


Figure 11. Switching Test Circuit

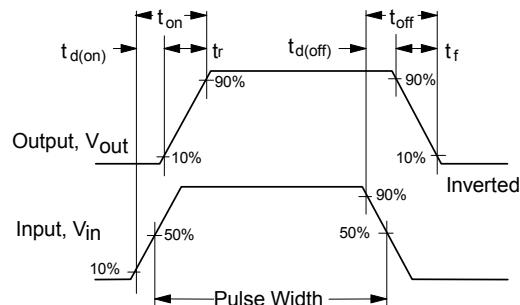
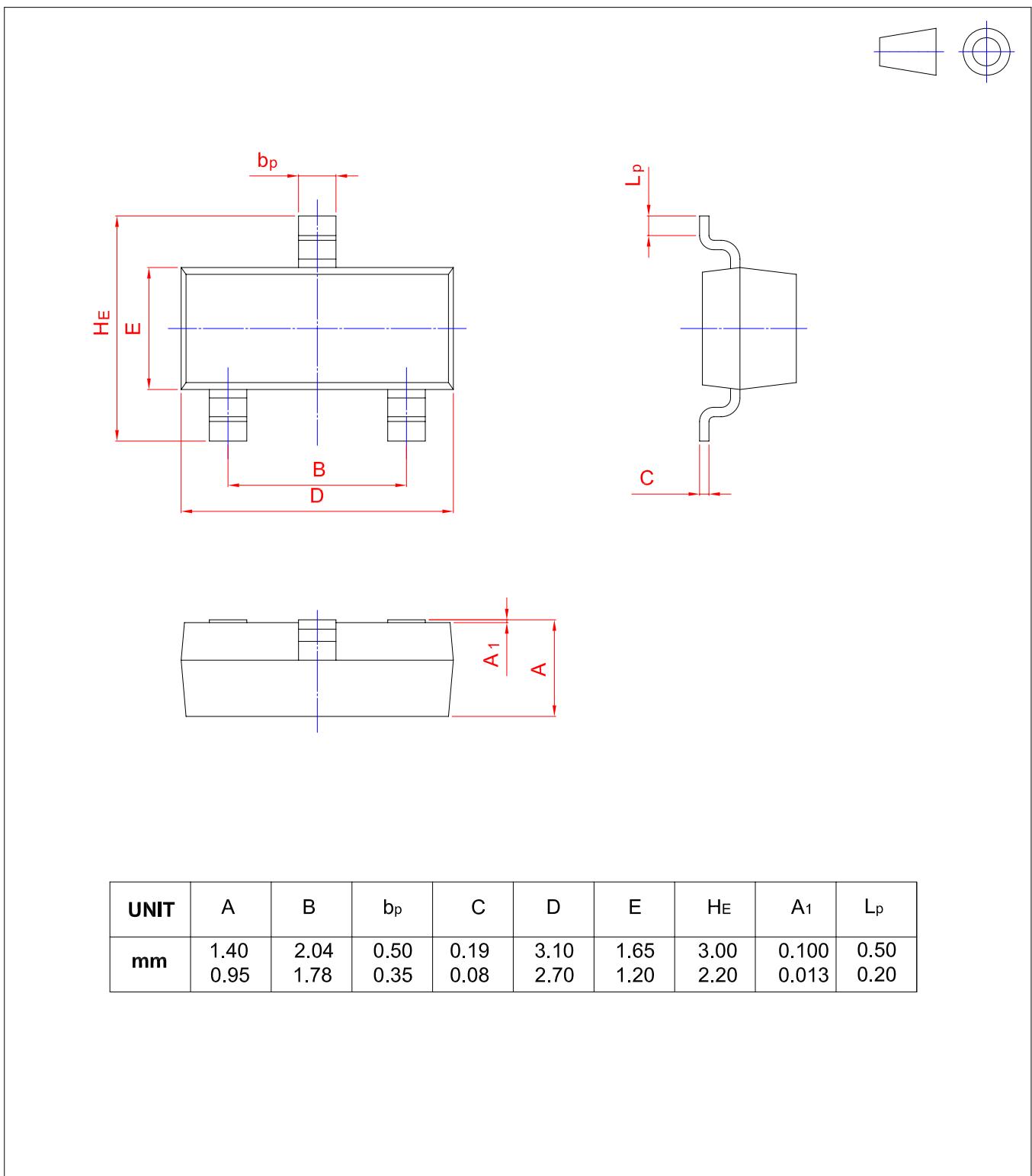


Figure 12. Switching Waveforms

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT-23



UNIT	A	B	b _p	C	D	E	H _E	A ₁	L _p
mm	1.40 0.95	2.04 1.78	0.50 0.35	0.19 0.08	3.10 2.70	1.65 1.20	3.00 2.20	0.100 0.013	0.50 0.20

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[SMAJ64A](#) [SMF48A](#) [SMF13A](#) [SMF100A](#) [ABS6](#) [ESD5321N](#) [SMBJ43CA](#) [SMBJ45CA](#) [SMF14A](#) [SMF22CA](#) [SMF75CA](#) [SMF64CA](#)
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