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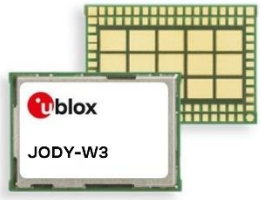
JODY-W3 series

Host-based automotive modules with Wi-Fi 6 and Bluetooth 5.3

Data sheet



Abstract

This technical data sheet describes the JODY-W3 series modules with Wi-Fi 802.11n/ac/ax and dual-mode Bluetooth 5.3. JODY-W3 is ideal for in-vehicle infotainment and telematics applications with simultaneous use cases requiring high data rates, such as in-car hotspots, Wi-Fi display applications such as Apple CarPlay, or video streaming across multiple clients. Connection to a host processor is through PCIe or SDIO interfaces for Wi-Fi and high-speed UART for Bluetooth.

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Product status	Corresponding content status	
Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
In Development / Prototype	Objective Specification	Target values. Revised and supplementary data will be published later.
Engineering Sample	Advance Information	Data based on early testing. Revised and supplementary data will be published later.
Initial Production	Early Production Information	Data from product verification. Revised and supplementary data may be published later.
Mass Production / End of Life	Production Information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Chipset	PCN reference	Product status
JODY-W354-A	JODY-W354-00A-00	NXP AW690	N/A	Mass production
JODY-W354-A	JODY-W354-20A-00	NXP AW690	N/A	Mass production
JODY-W374-A	JODY-W374-00A-00	NXP 88Q9098	N/A	Mass production
JODY-W374-A	JODY-W374-20A-00	NXP 88Q9098	N/A	Mass production
JODY-W374	JODY-W374-00B-00	NXP 88W9098	N/A	Mass production
JODY-W377-A	JODY-W377-00A-00	NXP 88Q9098	N/A	Mass production
JODY-W377	JODY-W377-00B-00	NXP 88W9098	N/A	Mass production

Contents

1 Functional description

1.1 Overview

The JODY-W3 series comprises compact modules based on the NXP AW690/88Q9098/88W9098 chipsets. The modules enable Wi-Fi, Bluetooth, and Bluetooth low energy communication, and are ideal for in-vehicle infotainment and telematics applications with common use cases that require high data rates, such as in-car hotspots, Wi-Fi display applications like Apple CarPlay, and video streaming across multiple clients. JODY-W3 modules can be operated in the following modes:

- Wi-Fi 1x1 and 2x2 802.11a/b/g/n/ac/ax in 2.4 GHz and 5 GHz
- Concurrent Dual Wi-Fi operation with independent MACs, supporting simultaneous Wi-Fi network operation at two different frequency bands
- Dual-mode Bluetooth 5.3, can be operated fully simultaneous with Wi-Fi

JODY-W3 modules undergo extended qualification testing in accordance with u-blox Qualification Policy based on AEC-Q104 and are manufactured in line with ISO/TS 16949 AEC-Q104. Host processor connections are made through various interfaces, including PCIe or SDIO for Wi-Fi and high-speed UART for Bluetooth.

1.2 Applications

Automotive applications

- In-car Access Point for internet access
- Usage of in-car applications like Apple CarPlay, Miracast, and so on
- Rear-seat display
- Rapid sync-n-go applications and fast content download to the vehicle
- Hands-free equipment (Bluetooth)

Industrial applications

- Manufacturing floor automation, wireless control terminals and point-to-point backhaul
- Machine control
- Medical in-hospital applications
- Security and surveillance
- Outdoor content distribution
- Robust wireless connectivity in a broad range of industrial applications

1.3 Block diagram

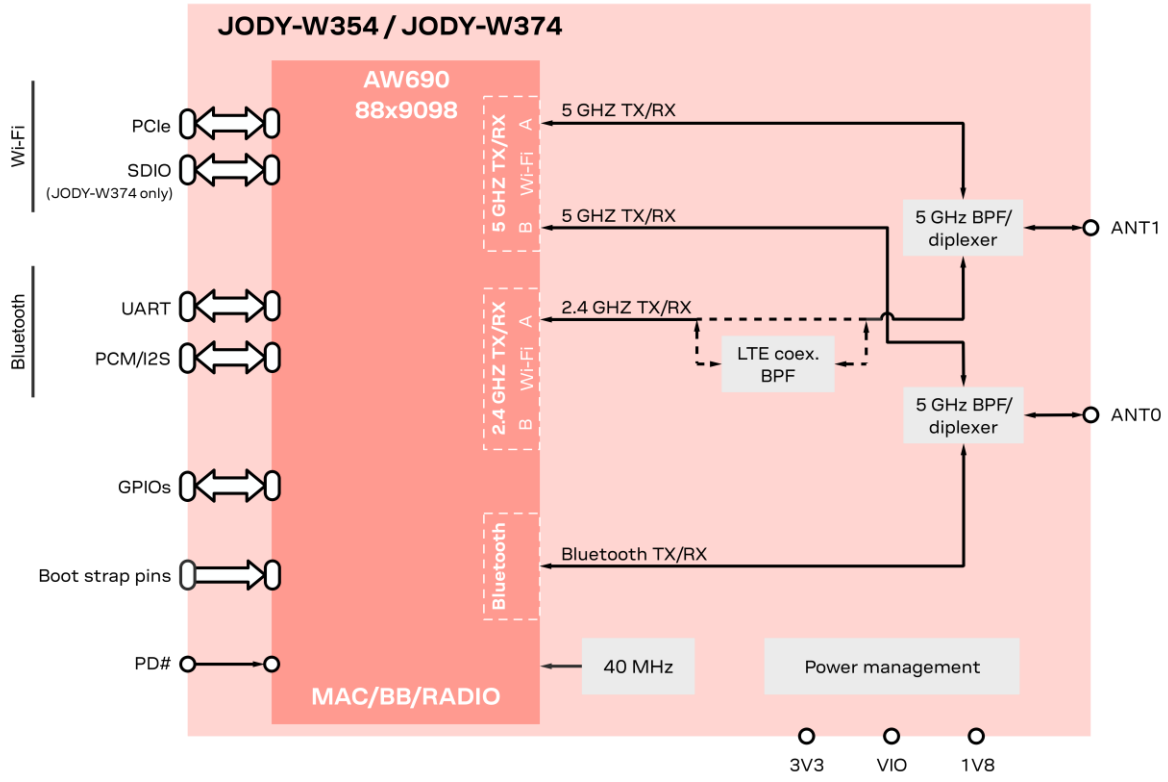

Figure 1: JODY-W354 and JODY-W374 block diagram

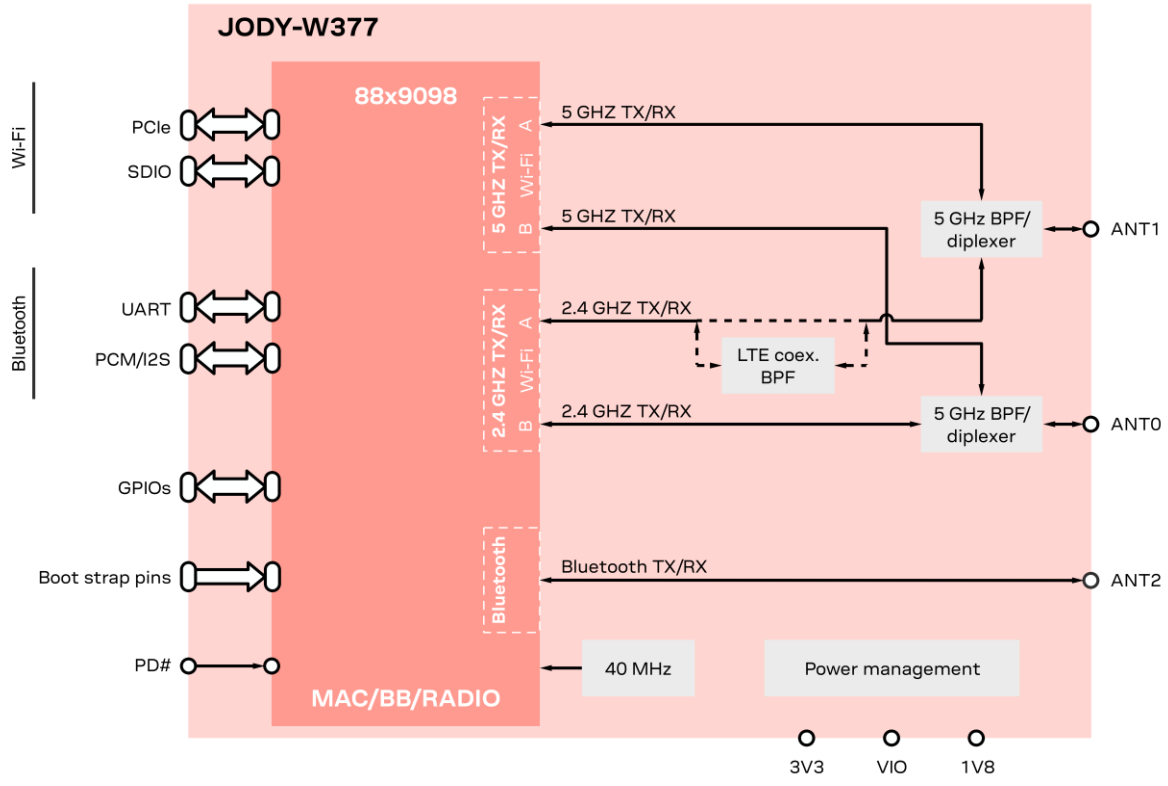

Figure 2: JODY-W377 block diagram

Table 1 shows the supported host interfaces, antenna, and LTE coexistence band pass filter configurations for JODY-W3 series modules.

Ordering code	Host i/f		Antenna configuration			LTE Coexistance BPF
	Wi-Fi	Bluetooth	ANT0	ANT1	ANT2	
JODY-W354-00A	PCIe	UART	5 GHz Wi-Fi and Bluetooth	2.4 and 5 GHz Wi-Fi	NC	No
JODY-W354-20A	PCIe	UART	5 GHz Wi-Fi and Bluetooth	2.4 and 5 GHz Wi-Fi	NC	Yes
JODY-W374-00A JODY-W374-00B	PCIe SDIO	UART	5 GHz Wi-Fi and Bluetooth	2.4 and 5 GHz Wi-Fi	NC	No
JODY-W374-20A	PCIe SDIO	UART	5 GHz Wi-Fi and Bluetooth	2.4 and 5 GHz Wi-Fi	NC	Yes
JODY-W377-00A JODY-W377-00B	PCIe SDIO	UART	2.4 and 5 GHz Wi-Fi	2.4 and 5 GHz Wi-Fi	Bluetooth	No

Table 1: Supported antenna and filter configurations for JODY-W3 series modules

☞ Module variants equipped with an LTE coexistence filter, as shown in Table 1, are recommended when co-located with LTE devices operating in LTE bands 7, 38, 40 or 41. See also LTE Coexistence performance.

1.4 Product features

Item	Description
Grade	JODY-W374: Professional JODY-W377: Professional JODY-W354-A: Automotive JODY-W374-A: Automotive JODY-W377-A: Automotive
Chipset	JODY-W374: NXP 88W9098 JODY-W377: NXP 88W9098 JODY-W354-A: NXP AW690 JODY-W374-A: NXP 88Q9098 JODY-W377-A: NXP 88Q9098
Antenna type	JODY-W354: Two antenna pins for Wi-Fi and Bluetooth JODY-W374: Two antenna pins for Wi-Fi and Bluetooth JODY-W377: Three antenna pins for Wi-Fi and Bluetooth
Supported Wi-Fi radio modes	Wi-Fi 6 (IEEE 802.11 a/b/g/n/ac/ax) See also Concurrent dual-band modes supported
Supported Wi-Fi bands	2.4 / 5 GHz (concurrent dual band)
Max. Wi-Fi output power conducted	19 dBm
Bluetooth version	5.3
Bluetooth profiles	HCI
Supported Bluetooth radio modes	Bluetooth BR/EDR Bluetooth Low Energy
Max. Bluetooth output power conducted	10 dBm
Supported Bluetooth LE data rates	1 Mbps 2 Mbps 500 kbps 125 kbps
LTE coexistence filter	JODY-W354-20A, JODY-W374-20A (Others on request)

Item	Description
OS support	Linux / Android
Interfaces	PCIe 2.0 (Wi-Fi) SDIO 3.0 (Wi-Fi, not supported on JODY-W354) UART (Bluetooth) PCM/I2S (Bluetooth digital audio)
Features	Micro access point with max. 64 connected clients
	Simultaneous client and access point mode
	WPA3
	RF parameters/MAC addresses in OTP
Max. ambient operating temperature	85 °C
Module size	19.8 x 13.8 mm

Table 2: JODY-W3 series product features

1.5 Wi-Fi features

- Standards:
  - IEEE 802.11a/b/g/n/ac/ax
  - IEEE 802.11e/h/i/k/mc/r/u/v/w/z[1]
- Concurrent 2.4 GHz and 5 GHz dual-band operation, see also Concurrent dual-band modes supported
- Single band Wi-Fi 6 operation modes supported:
  - JODY-W354: 1x1 2.4 GHz 802.11ax (40 MHz) or 2x2 5 GHz 802.11ax (80 MHz)
  - JODY-W374: 1x1 2.4 GHz 802.11ax (40 MHz) or 2x2 5 GHz 802.11ax (80 MHz)
  - JODY-W377: 2x2 2.4 GHz 802.11ax (40 MHz) or 2x2 5 GHz 802.11ax (80 MHz)
- MU-MIMO and OFDMA (STA mode)
- IEEE 802.11ax PHY data rates, 5 GHz up to 1.2 Gbps, and 2.4 GHz up to 458 Mbps
- Bandwidth support of 20, 40, and 80 MHz
- DFS master with Zero Wait (Zero Wait DFS not supported on JODY-W354)
- Simultaneous client and access point operation
- Support of Wi-Fi direct/P2P mode
- Wi-Fi channels:
  - 2.4 GHz: 1-13
  - 5 GHz: 36-165
- Encryption: AES/CCMP, AES/GCMP, WAPI
- WPA2/WPA3 support
- SDIO 3.0 and PCIe v2.0 host interface for Wi-Fi (JODY-W354 only PCIe)
- Support of 64 clients in AP mode

2.4 GHz band			5 GHz band		
Mode	**Technology**	**Bandwidth**	**Mode**	**Technology**	**Bandwidth**
2x2 (-W377) 1x1 (-W354, -W374)	802.11n	40 MHz	2x2 (-W374, -W377) 1x1 (-W354)	802.11ax	80 MHz
	802.11ax	40 MHz		802.11ac	40 MHz
	802.11n	40 MHz	1x1 1RX (-W374, -W377)	802.11ax Zero Wait DFS	80 MHz 80 MHz

Table 3: Concurrent dual-band modes supported

[1] 802.11k/r/u/v in STA mode only

1.6 Bluetooth features

- Bluetooth 5.3 with Bluetooth Low Energy (LE)
- BR and EDR packet types – 1 Mbps, 2 Mbps, and 3 Mbps
- Bluetooth LE 1 Mbps and 2 Mbps PHY
- LE Data Length Extension
- LE Advertising Extension
- LE Long Range
- Bluetooth class 1.5 and 2
- UART HCI transport layer
- PCM/I2S interface for voice applications

1.7 Reserved MAC addresses

The JODY-W3 series has four unique consecutive MAC addresses reserved for each module. The first three of these four addresses are already stored in the configuration during production.

The first address is used for Bluetooth communication while the second and third addresses are configured for Wi-Fi communication. The Data Matrix Code on the label includes the Bluetooth MAC address. See also Product labeling. The remaining MAC address is not used in the manufacturing configuration but is reserved for use with the module.

MAC address	Assignment	Last two bits of MAC address	Example
Module1, address 1	Bluetooth	0b00	*D4:CA:6E:44:00:04*
Module1, address 2	Wi-Fi (MAC1)	0b01	D4:CA:6E:44:00:05
Module1, address 3	Wi-Fi (MAC2)	0b10	D4:CA:6E:44:00:06
Module1, address 4	(free for use)	0b11	D4:CA:6E:44:00:07
Module2, address 1	Bluetooth	0b00	*D4:CA:6E:44:00:08*
Module2, address 2	Wi-Fi (MAC1)	0b01	D4:CA:6E:44:00:09
Module2, address 3	Wi-Fi (MAC2)	0b10	D4:CA:6E:44:00:0A
Module2, address 4	(free for use)	0b11	D4:CA:6E:44:00:0B

Table 4: MAC address assignment

For further details about using the MAC address for secondary Wi-Fi interfaces, see “Assigning MAC addresses” in the system integration manual [2].

2 Interfaces

2.1 Configuration pins

JODY-W3 series modules require configuration pins to be set following a reset. The definition of these configuration pins changes immediately (approximately 1 ms) after reset to their usual function.

To set a configuration bit to 0, attach a 51 kΩ resistor to **GND**. No external pull-up resistor is required to set a configuration bit to 1. The configuration pins **CONFIG[2:0]** are used for the firmware boot options.

Configuration bits	Pin name	Pin number	Configuration setting
CON[10]	PCM_CLK	16	1
CON[9]	PCM_OUT	17	1
CON[8]	PCM_IN	18	1
CON[7]	GPIO_17	88	1
CON[6]	BT_HOST_WAKE	12, 87	1
CON[5]	WL_HOST_WAKE	10, 86	1
CON[4]	GPIO_14	85	0 (A 51 kΩ resistor to GND is attached on the module. No external resistor is required. Do not pull high during boot-up)

Firmware boot options

NOTE: Boot code must use this host boot strap status to decide the correct boot sequence.

CON[2:0]	CONFIG[2:0]	CONFIG[2]: 6 CONFIG[1]: 8 CONFIG[0]: 7	**Strap value**	**Wi-Fi**	**Bluetooth**
			000	SDIO	UART
			011	PCIe	UART
			other	reserved	reserved

Table 5: Configuration pins

2.2 SDIO interface

The SDIO device interface conforms to the industry standard SDIO 3.0 specification (UHS-I, up to 104 MB/s) and allows a host controller using the SDIO bus protocol to access the Wi-Fi functions in JODY-W374 and JODY-W377 modules. The interface supports 4-bit SDIO transfer mode at the full clock range up to 208 MHz.

☞ For SDIO 2.0 running at 25 MHz and 50 MHz clock frequency, only 1.8 V is supported.

SDIO mode	Max clock frequency (MHz)	Signal voltage (V)	Speed (MB/s)
DS: Default Speed	25	1.8	12.5
HS: High Speed	50	1.8	25
SDR12	25	1.8	12.5
SDR25	50	1.8	25
SDR50	100	1.8	50
SDR104	208	1.8	104
DDR50	50	1.8	50

Table 6: Supported SDIO modes

2.2.1 Default speed and High Speed modes (1.8 V)

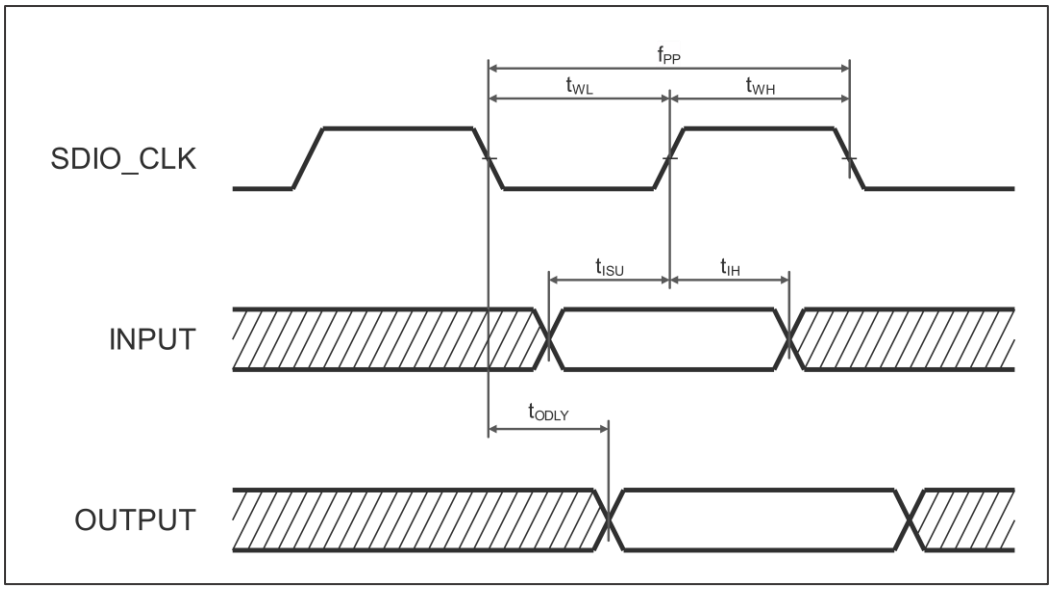

Figure 3: SDIO Protocol timing diagram- Default Speed mode (1.8 V)

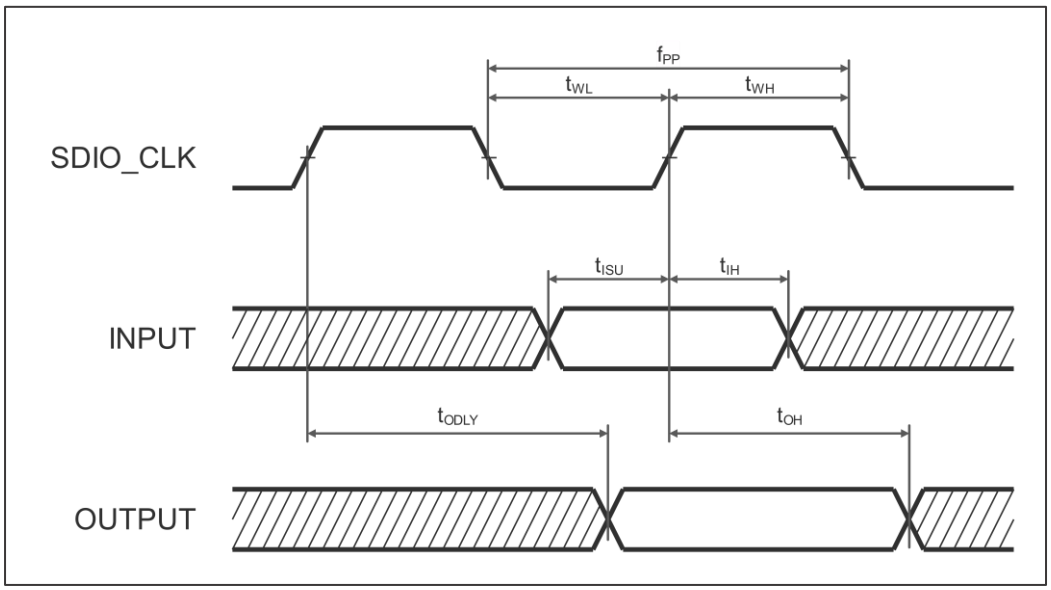

Figure 4: SDIO Protocol timing diagram – High Speed mode (1.8 V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency – Data Transfer Mode	Normal	0	-	25	MHz
		High speed	0	-	50	MHz
f_{OD}	Clock frequency – Identification Mode	Normal	0		400	kHz
		High speed	0	-	400	kHz
t_{WL}	Clock low time	Normal	10	-	-	ns
		High speed	7	-	-	ns
t_{WH}	Clock high time	Normal	10	-	-	ns
		High speed	7	-	-	ns
t_{ISU}	Input setup time	Normal	5	-	-	ns
		High speed	6	-	-	ns
t_{IH}	Input hold time	Normal	5	-	-	ns
		High speed	2	-	-	ns
t_{ODLY}	Output delay time	Normal	-	-	14	ns
t_{ODLY}	Output delay time CL ≤ 40 pF (1 card)	High speed	-	-	14	ns
t_{OH}	Output hold time	High speed	2.5	-	-	ns

Table 7: SDIO Timing data – Default speed, High Speed modes (1.8 V)

2.2.2 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8 V)

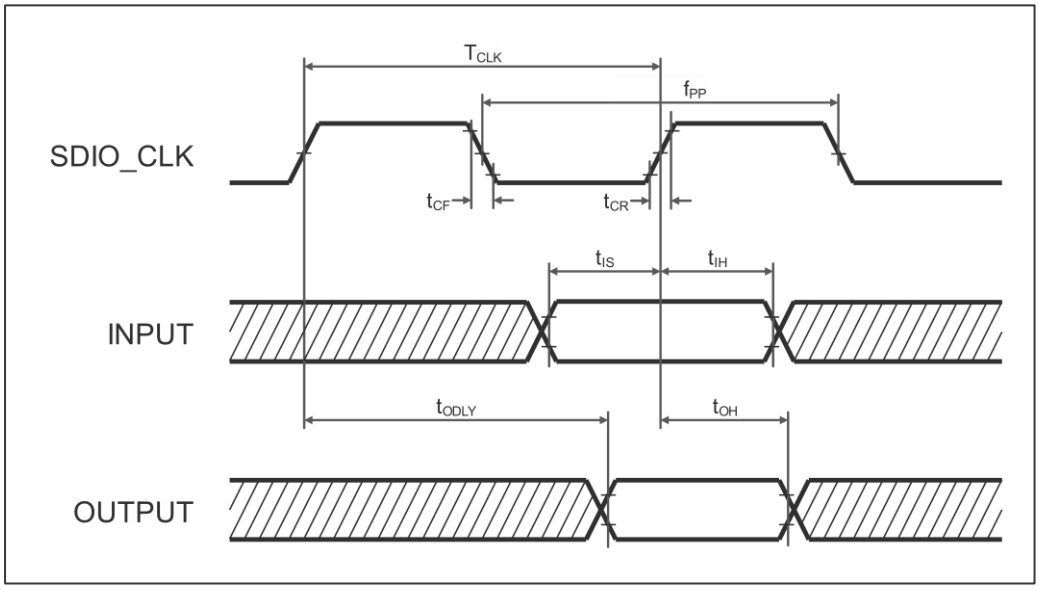

Figure 5: SDIO Protocol timing diagram – SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8 V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency	SDR12	0	-	25	MHz
		SDR25	0	-	50	MHz
		SDR50	0	-	100	MHz
t_{IS}	Input setup time	SDR12/25/50	3	-	-	ns
t_{IH}	Input hold time	SDR12/25/50	0.8	-	-	ns
t_{CLK}	Clock time	SDR12/25/50	10	-	40	ns
t_{CR}, t_{CF},	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50		-	0.2*T_{CLK}	ns
t_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12/25/50	-		7.5	ns
t_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	-	-	ns

Table 8: SDIO Timing data – SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8 V)

2.2.3 SDR104 mode (208 MHz) (1.8 V)

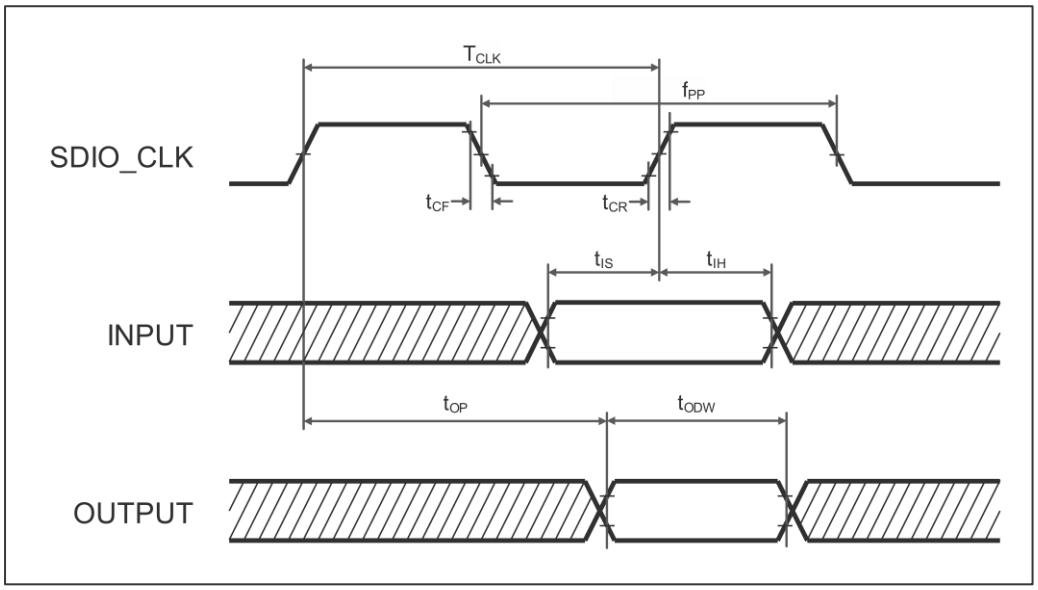

Figure 6: SDIO Protocol timing diagram – SDR104 mode (208 MHz) (1.8 V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency	SDR104	0	-	208	MHz
T_{IS}	Input setup time	SDR104	1.4	-	-	ns
T_{IH}	Input hold time	SDR104	0.8	-	-	ns
T_{CLK}	Clock time	SDR104	4.8	-	-	ns
t_{CR}, t_{CF},	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104		-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	-	-	ns

Table 9: SDIO Timing data – SDR104 mode (208 MHz) (1.8 V)

2.2.4 DDR50 mode (50 MHz) (1.8 V)

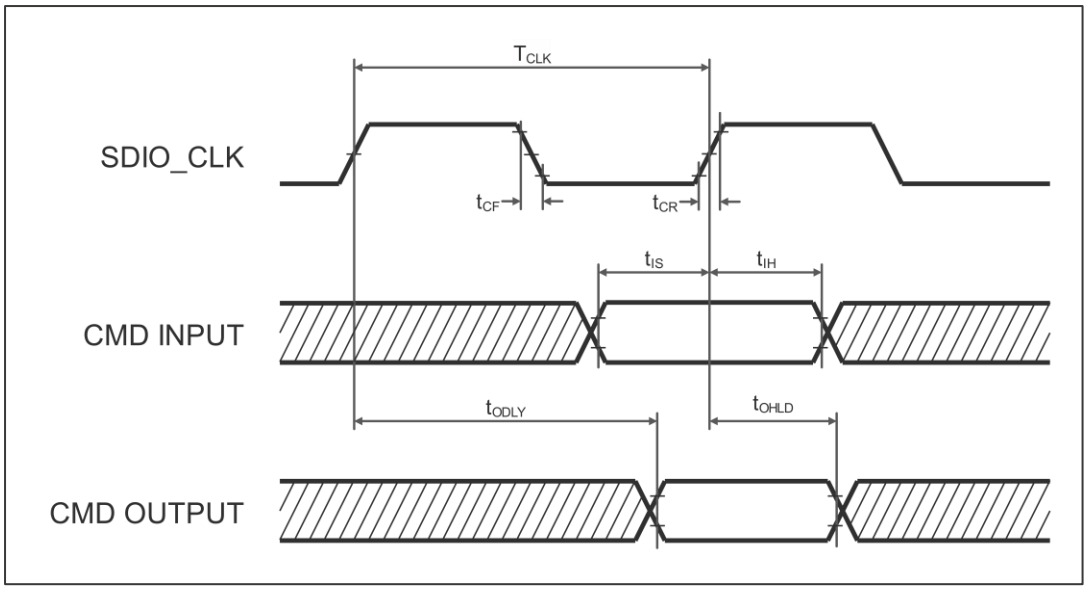

Figure 7: SDIO CMD timing diagram – DDR50 mode (50 MHz) (1.8 V)

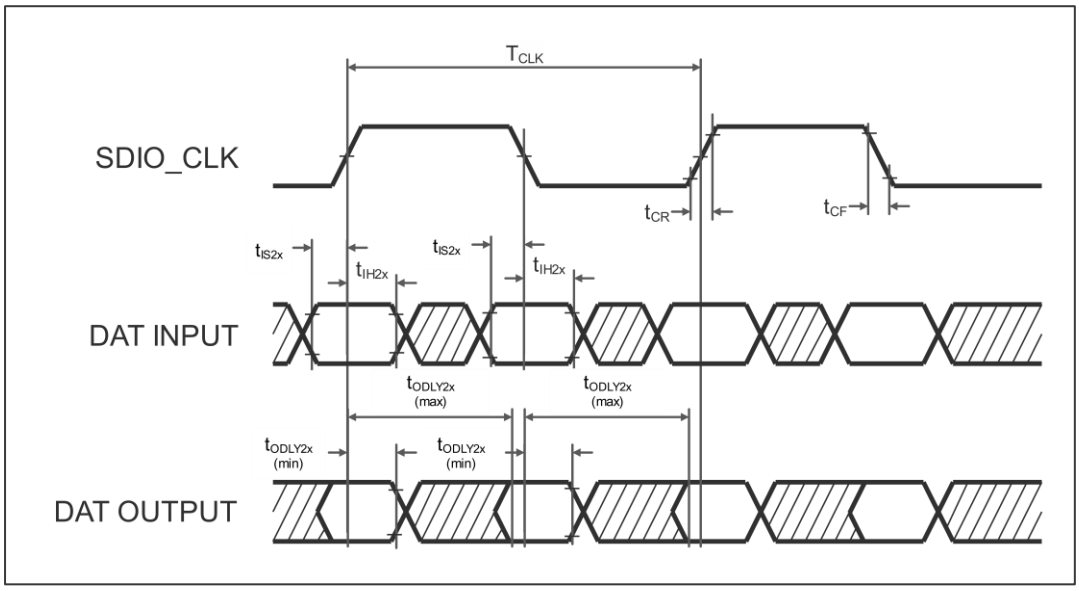

Figure 8: SDIO DAT[3:0] timing diagram – DDR50 mode (50 MHz) (1.8 V)

Symbol	Parameter	Condition	Min.	Typ	Max.	Units
Clock						
TCLK	Clock time 50 MHz (max) between rising edges	DDR50	20	-	-	ns
tCR, tCF,	Rise time, fall time TCR, TCF < 4.00 ns (max) at 50 MHz CCARD = 10 pF	DDR50	-	-	0.2*TCLK	ns
Clock Duty		DDR50	45	-	55	%
CMD Input (referenced to clock rising edge)						
tIS	Input setup time CCARD ≤ 10 pF (1 card)	DDR50	6	-	-	ns
tIH	Input hold time CCARD ≤ 10 pF (1 card)	DDR50	0.8	-	-	ns
CMD Output (referenced to clock rising edge)						
tODLY	Output delay time during data transfer mode CL ≤ 30 pF (1 card)	DDR50	-	-	13.7	ns
tOHLD	Output hold time CL ≥ 15 pF (1 card)	DDR50	1.5	-	-	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
tIS2x	Input setup time CCARD ≤ 10 pF (1 card)	DDR50	3			ns
tIH2x	Input hold time CCARD ≤ 10 pF (1 card)	DDR50	0.8			ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
tODLY2x (max)	Output delay time during data transfer mode CL ≤ 25 pF (1 card)	DDR50			7.0	ns
tODLY2x (min)	Output hold time CL ≥ 15 pF (1 card)	DDR50	1.5			ns

Table 10: SDIO Timing data – DDR50 mode (50 MHz) (1.8 V)

2.3 PCI Express interface

The PCI Express interface complies with the PCIe 2.0 standard at 2.5/5 GT/s speeds. It allows a host controller using the PCIe bus protocol to access Wi-Fi functionality of JODY-W3 series modules.

Table 11 shows the parameter specifications for the PCI Express 2.5 GT/s interface.

PCI Express specifications for 2.5 GT/s						
Parameter	**Symbol**	**Comments**	**Min.**	**Typ.**	**Max.**	**Units**
		General				
Unit Interval (UI)	UI	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.	399.88	-	400.12	ps
		Receiver				
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Power down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	200	-	-	kΩ
Input voltage	VRX-DIFFp-p-CC	Differential RX peak-to-peak voltage for common Refclk Rx architecture	0.175	-	1.2	V
	VRX-DIFFp-p-DC	Differential RX peak-to-peak voltage for data clocked RX architecture	0.175	-	1.2	V
	VRX-CM-ACp	AC peak common mode input voltage	-	-	150	mV
RX eye time opening	TRX-EYE	Minimum eye time at RX pins to Yield a 10^{-12} BER.	0.40	-	-	UI
RX jitter tolerance	TRX-EYE-MEDIAN-to-MAX-JITTER	Maximum time delta between median and deviation from median	-	-	0.30	UI
Return loss	RLRX-DIFF	Differential return loss	15	-	-	dB
	RLRX-CM	Common-mode return loss	0	-	3.6	dB
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	-	175	mV
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition	-	-	10	ms
Total skew	LRX-SKEW	Total skew	-	-	20	ns
		Transmitter				
Output voltage	VTX-DIFFp-p	Differential peak-to-peak TX voltage swing	0.8	-	1.2	V
	VTX-DIFFp-p-LOW	Low power differential peak-to-peak TX voltage swing	0.4	-	1.2	V
TX de-emphasis level ratio	VTX-DE-RATIO-3.5dB	TX de-emphasis level ratio (3.5 dB)	3.0	-	4.0	dB
Output voltage rise and fall time	VTX-RISE-FALL	Measured differentially from 20% to 80% of swing.	0.125	-	-	UI
TX jitter	TTX-EYE	TX eye including all jitter sources	0.75	-	-	UI
	TTX-EYE-MEDIAN-to-MAX-JITTER	Maximum time between jitter median and maximum deviation from median	-	-	0.125	UI
Return loss	RLTX-DIFF	TX package plus Si differential return loss	10	-	-	dB
	RLTX-CM	TX package plus Si common mode	6	-	-	dB

PCI Express specifications for 2.5 GT/s						
Parameter	**Symbol**	**Comments**	**Min.**	**Typ.**	**Max.**	**Units**
		return loss				
TX AC peak common-mode voltage	VTX-CM-AC-P	TX AC common mode voltage	-	20	-	mV
DC common mode voltage	VTX-DC-CM	TX DC common mode voltage	0	-	3.6	V
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electrical idle	0	-	100	mV
Idle differential output voltage	VTX-IDLE-DIFF-AC-p	Electrical idle differential peak output voltage	0	-	20	mV
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection	-	-	600	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground	-	-	90	mA
Electrical idle timings	TTX-IDLE-MIN	Minimum time spent in electrical idle	20	-	-	ns
	TTX-IDLE-SET-TO-IDLE	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	-	-	8	ns
	TTX-IDLE-TO-DIFF-DATA	Maximum time to transition to valid differential signaling after leaving electrical idle	-	-	8	ns
Crosslink timeout	TCROSSLINK	Crosslink random timeout	-	-	1.0	ms

Table 11: PCI Express interface parameters for 2.5 GT/s

Table 12 shows the parameter specifications for the PCI Express 5 GT/s interface.

PCIe specifications for 5 GT/s						
Parameter	**Symbol**	**Comments**	**Min.**	**Typ.**	**Max.**	**Units**
		General				
Unit Interval (UI)	UI	The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.	199.94	-	200.06	ps
		Receiver				
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Power down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	200	-	-	kΩ
Input voltage	VRX-DIFFp-p-CC	Differential RX peak-to-peak voltage for common Refclk Rx architecture	0.12	-	1.2	V
	VRX-DIFFp-p-DC	Differential RX peak-to-peak voltage for data clocked RX architecture	0.10	-	1.2	V
	VRX-CM-Acp	AC peak common mode input voltage	-	-	150	mV
RX jitter tolerance	TRX-TJ-CC	Maximum RX inherent total timing error for common Refclk RX architecture	-	-	0.40	UI
	TRX-TJ-DC	Maximum RX inherent total timing error for data clocked RX architecture	-	-	0.34	UI
	TRX-DJ-DD-CC	Maximum Rx inherent deterministic timing error for common Refclk	-	-	0.30	UI

PCIe specifications for 5 GT/s						
Parameter	**Symbol**	**Comments**	**Min.**	**Typ.**	**Max.**	**Units**
		architecture				
	TRX-DJ-DD-DC	Maximum RX inherent deterministic timing error for data clocked RX architecture	-	-	0.24	UI
	TRX-MIN-PULSE	Minimum width pulse at RX Measured to account for worst Tj at 10^{-12} BER	0.6	-	-	UI
Return loss	RLRX-DIFF	Differential return loss	15	-	-	dB
	RLRX-CM	Common-mode return loss	0	-	3.6	dB
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	-	175	mV
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition	-	-	10	ms
Total skew	LRX-SKEW	Total skew	-	-	20	ns
		Transmitter				
Output voltage	VTX-DIFFp-p	Differential peak-to-peak TX voltage swing	0.8	-	1.2	V
	VTX-DIFFp-p-LOW	Low power differential peak-to-peak TX voltage swing	0.4	-	1.2	V
TX de-emphasis level ratio	VTX-DE-RATIO-3.5dB	TX de-emphasis level ratio (3.5 dB)	3.0	-	4.0	dB
	VTX-DE-RATIO-6dB	TX de-emphasis level ratio (6 dB)	5.5	-	6.5	dB
Output voltage rise and fall time	VTX-RISE-FALL	Measured differentially from 20% to 80% of swing.	0.15	-	-	UI
Instantaneous lone pulse width	TMIN-Pulse	Measured relative to rising/falling pulse.	0.9	-	-	UI
TX jitter	TTX-EYE	TX eye including all jitter sources	0.75	-	-	UI
	TTX-HF-DJ-DD	TX deterministic jitter > 1.5 MHz Deterministic jitter only	-	-	0.15	UI
	TTX-LF-RMS	TX RMS jitter < 1.5 MHz Total energy measured over a 10 kHz–1.5 MHz range.	-	3.0	-	ps RMS
Return loss	RLTX-DIFF	TX package plus Si differential return loss (0.05–1.25 GHz)	10	-	-	dB
		TX package plus Si differential return loss (1.25–2.5 GHz)	8	-	-	dB
	RLTX-CM	TX package plus Si common mode return loss	6	-	-	dB
TX AC peak common-mode voltage	VTX-CM-AC-PP	TX AC common mode voltage	-	-	100	mVPP
DC common mode voltage	VTX-DC-CM	TX DC common mode voltage	0	-	3.6	V
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electrical idle	0	-	100	mV
Idle differential output voltage	VTX-IDLE-DIFF-AC-p	Electrical idle differential peak output voltage	0	-	20	mV
	VTX-IDLE-DIFF-DC	DC electrical idle differential output voltage	0	-	5	mV

PCIe specifications for 5 GT/s						
Parameter	**Symbol**	**Comments**	**Min.**	**Typ.**	**Max.**	**Units**
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection	-	-	600	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground	-	-	90	mA
Electrical idle timings	TTX-IDLE-MIN	Minimum time spent in electrical idle	20	-	-	ns
	TTX-IDLE-SET-TO-IDLE	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	-	-	8	ns
	TTX-IDLE-TO-DIFF-DATA	Maximum time to transition to valid differential signaling after leaving electrical idle	-	-	8	ns
Crosslink timeout	TCROSSLINK	Crosslink random timeout	-	-	1.0	ms

Table 12: PCI Express interface parameters for 5 GT/s

2.4 UART interface

JODY-W3 series modules support a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface in compliance with the industry standard 16550 specification.

The main features of the UART interface include:

- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit and receive operations
- Two flow control pins
- Interrupt triggers for low-power, high-throughput operation
- High throughput (up to 4 Mbit/s)
- The default baud rate after reset is 115200 baud and 3000000 baud after firmware is loaded.

Baud rate (bits per second)				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	

Table 13: Supported UART baud rates

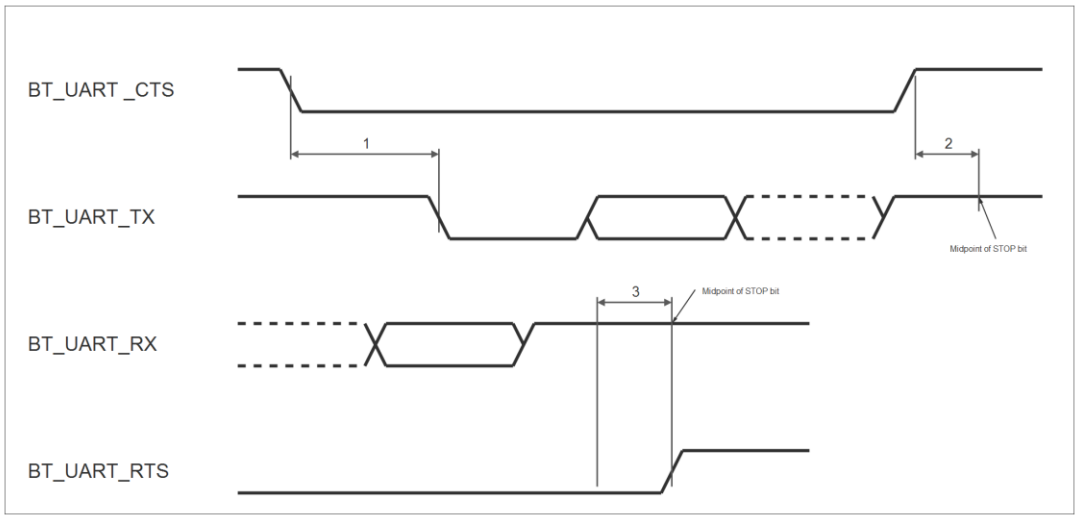

Figure 9: UART timing

Reference	Characteristic	Min.	Typ.	Max.	Units
1	Delay time, BT_UART_CTS low to BT_UART_TX valid	-	-	1.5	Bit period
2	Setup time, BT_UART_CTS high before midpoint of stop bit	-	-	0.5	Bit period
3	Delay time, midpoint of stop bit to BT_UART_RTS high	-	-	0.5	Bit period

Table 14: UART timing specification

2.5 Audio interfaces

2.5.1 PCM interface

JODY-W3 series modules support a Pulse Code Modulation (PCM) interface that features:

- Master and slave mode
- PCM bit-width size of 8 or 16 bits
- Up to four slots with configurable bit width and start positions
- Tri-state PCM interface capability
- PCM short frame and long frame synchronization
- PCM pins shared with I2S

In PCM master mode, the interface generates a 2 MHz or a 2.048 MHz **PCM_CLK** and 8 kHz or 16 kHz **PCM_SYNC** signal.

In slave mode, the interface has both **PCM_CLK** and **PCM_SYNC** as inputs, which let another unit on the PCM bus generate the signals.

PCM Interface specifications

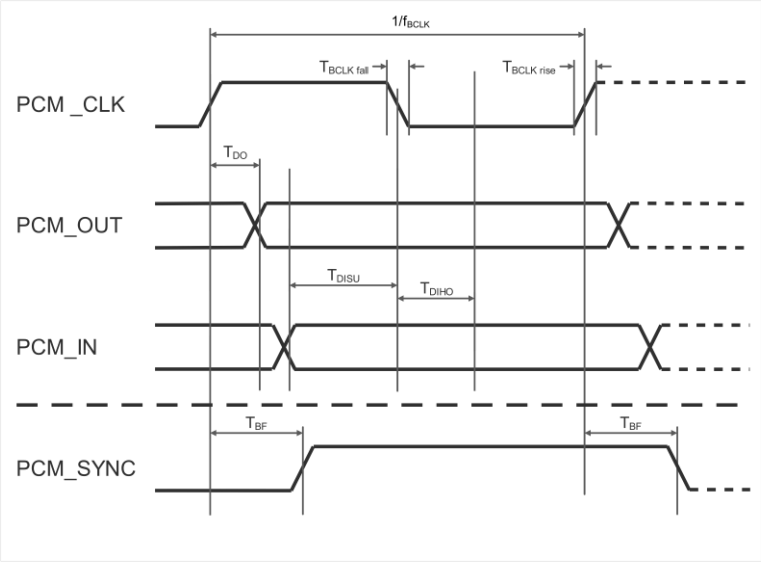

Figure 10: PCM timing specification for data signals and the PCM_SYNC signal – master mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{BCLK}	Bit clock frequency	-	2	2/2.048	2.048	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle		0.4	0.5	0.6	-
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	-	-	3	-	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	-	-	-	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	-	20	-	-	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	-	15	-	-	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	-	-	-	15	ns

Table 15: PCM timing specification – master mode

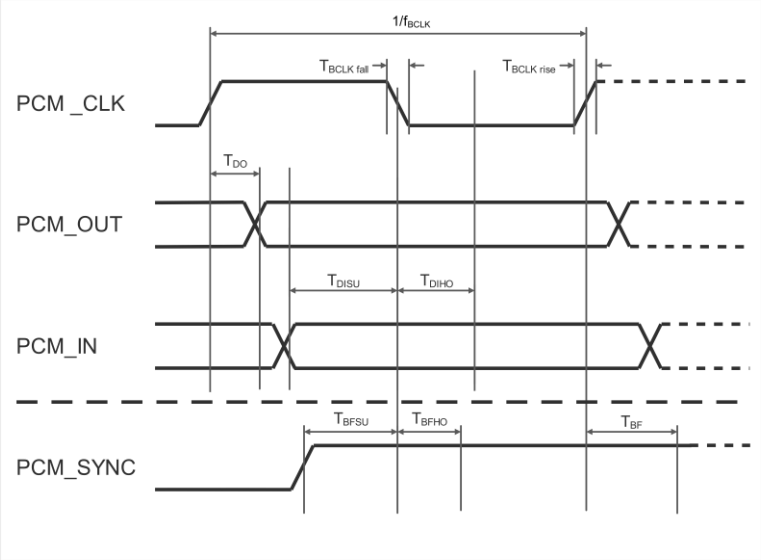

Figure 11: PCM timing specification for data signals and the PCM_SYNC signal – slave mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{BCLK}	Bit clock frequency	-	0.512	2/2.048	4	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle		0.4	0.5	0.6	-
$T_{BCLK\ rise/fall}$	PCm_CLK rise/fall time	-	-	3	-	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	-	-	-	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	-	15	-	-	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	-	10	-	-	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	-	15	-	-	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	-	10	-	-	ns

Table 16: PCM timing specification – slave mode

2.5.2 I2S interface

JODY-W3 series modules support an Inter-IC Sound (I2S) interface that shares pins with the PCM interface and supports mono and dual channel modes.

- I2S interface for audio data connection to Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC)
- Master and slave mode for I2S audio interfaces
- Tri-state I2S interface compatibility
- I2S pins shared with PCM pins

In mono-channel mode, by default the left channel is used for data. In dual-channel mode, the two channels are supported on two time slots.

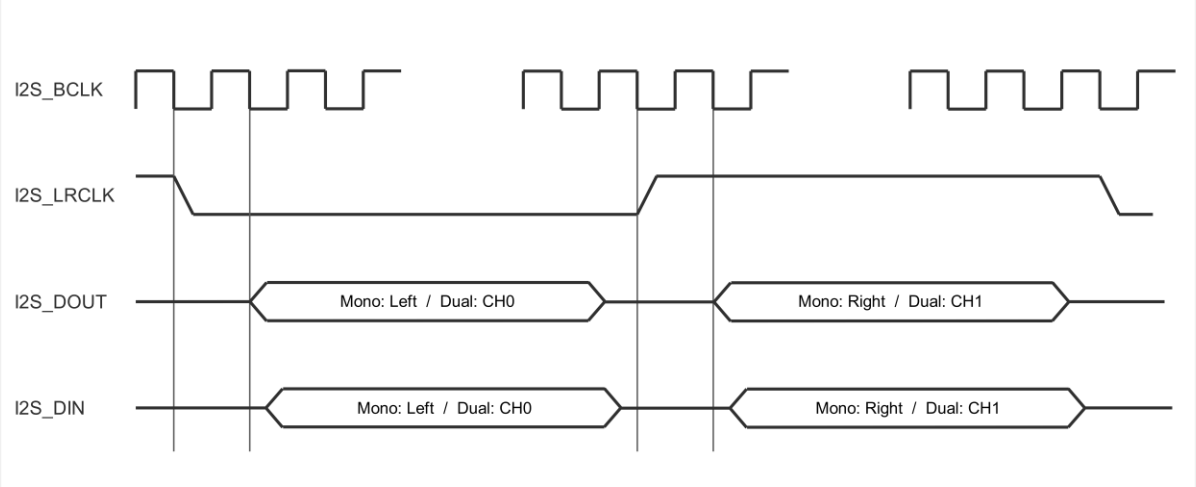

Figure 12: I2S timing specification - mono-/dual-channel mode

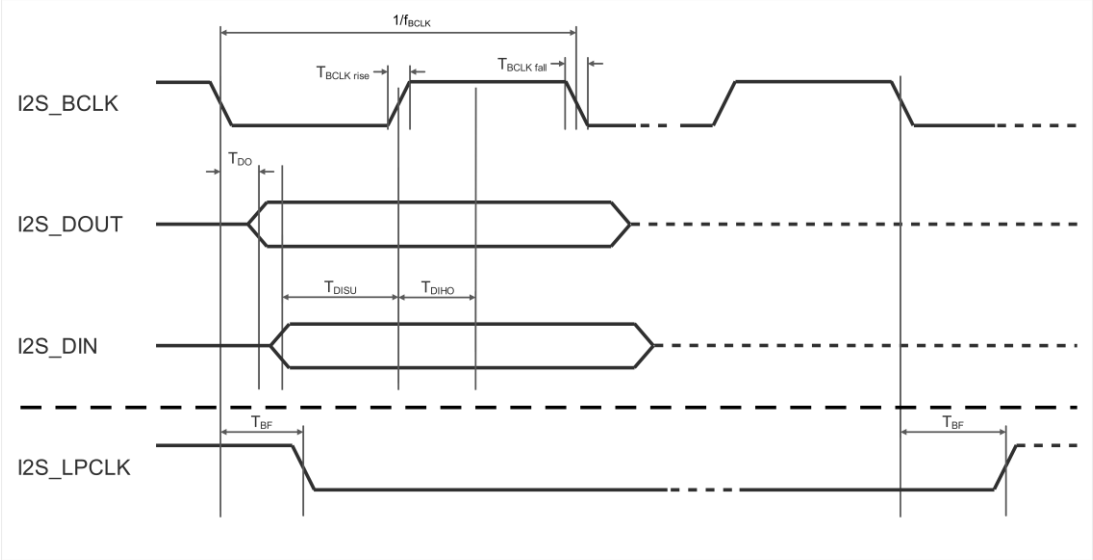

Figure 13: I2S timing specification for data and clock signals - master mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{BCLK}	Bit clock frequency	-	1.024	2/2.048	4.096	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle		45	50	55	%
$T_{BCLK\ rise/fall}$	I2S_BCLK rise/fall time	-	-	3	-	ns
T_{DO}	Delay from I2S_BCLK falling edge to I2S_DOUT rising edge	-	-	-	40	ns
T_{DISU}	Setup time for I2S_DIN before I2S_BCLK rising edge	-	10	-	-	ns
T_{DIHO}	Hold time for I2S_DIN after I2S_BCLK rising edge	-	0	-	-	ns
T_{BF}	Delay from I2S_BCLK falling edge to I2S_LRCLK falling edge	-	-	-	40	ns

Table 17: I2S timing specification - master mode

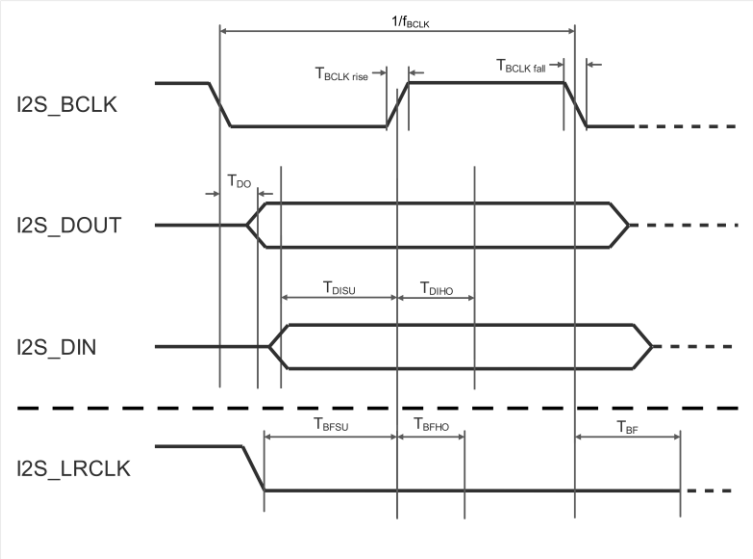

Figure 14: I2S timing specification for data and clock signals - slave mode

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{BCLK}	Bit clock frequency	-	1.024	2/2.048	4.096	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle		45	50	55	%
$T_{BCLK\ rise/fall}$	I2S_BCLK rise/fall time	-	-	3	-	ns
T_{DO}	Delay from I2S_BCLK falling edge to I2S_DOUT rising edge	-	-	-	40	ns
T_{DISU}	Setup time for I2S_DIN before I2S_BCLK rising edge	-	10	-	-	ns
T_{DIHO}	Hold time for I2S_DIN after I2S_BCLK rising edge	-	0	-	-	ns
T_{BFSU}	Setup time for I2S_LRCLK before I2S_BCLK rising edge	-	40	-	-	ns
T_{BFHO}	Hold time for I2S_LRCLK after I2S_BCLK rising edge	-	0	-	-	ns

Table 18: I2S timing specification - slave mode

2.6 Coexistence interfaces

2.6.1 PTA

Pin name	Pin number	Function	Pin type	Description
GPIO_2	34	EXT_STATE	I	External radio state input signal. External radio traffic direction (Tx/Rx): • 1: TX • 0: RX
GPIO_17	88	EXT_GNT	O	External radio grant output signal
GPIO_1	92	EXT_FREQ	I	External radio frequency input signal. Frequency overlap between external radio and Wi-Fi: • 1: overlap • 0: non-overlap This signal is useful when the external radio is a frequency hopping device.
GPIO_19	90	EXT_PRI	I	External radio priority input signal. Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2 bit priority (sample twice). Can also support TX/RX information following the priority information if EXT_STATE is not used.
GPIO_18	89	EXT_REQ	I	Request from the external radio

Table 19: PTA coexistence interface

2.6.2 WCI-2

Pin name	Pin number	Function	Pin type	Description
GPIO_31	13	WCI2_SOUT	0	WCI-2 output signal
GPIO_30	14	WCI2_SIN	I	WCI-2 input signal

3 Pin definition

3.1 Pin assignment

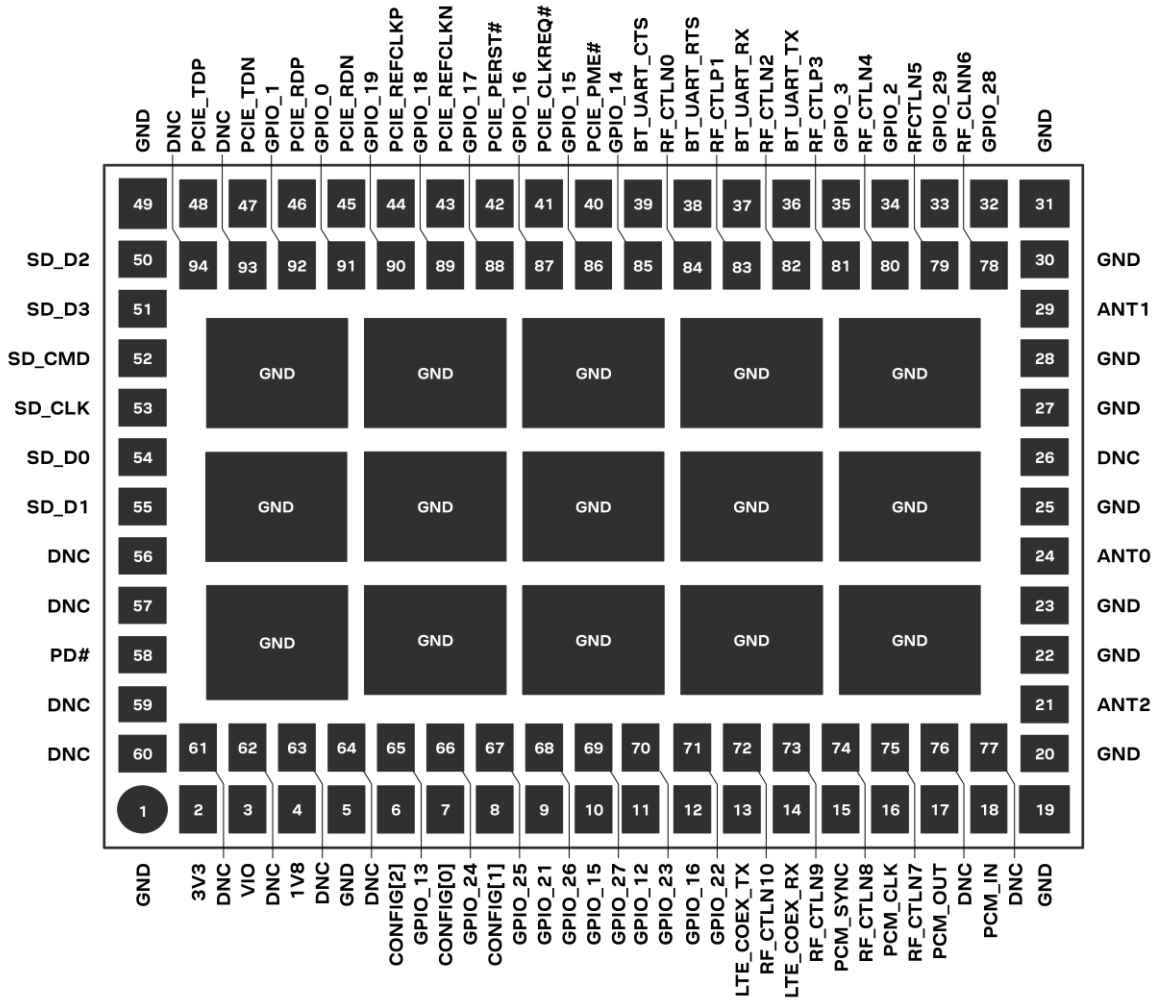

Figure 15: Pin assignment

3.2 Pin description

No.	Name	Pin type[2]	Chipset pin	Description	Power domain
1	GND	GND		Ground	
2	3V3	PWR		3.3 V analog power supply	3V3
3	VIO	PWR		VIO supply (1.8 V or 3.3 V)	VIO
4	1V8	PWR		1.8 V analog power supply	1V8
5	GND	GND		Ground	

[2] I/O notations: I=Input, O=Output, I/O=Input or Output, OD=Open Drain, NC=Not Connected, DNC=Do not connect, PWR=Power, GND=Ground, RF=Radio i/f

No.	Name	Pin type[2]	Chipset pin	Description	Power domain
6	CONFIG[2]	I	CONFIG_HOST[2]	Firmware boot options. See also Table 5, Configuration pins.	1V8
7	CONFIG[0]	I	CONFIG_HOST[0]	Firmware boot options. See also Table 5, Configuration pins.	1V8
8	CONFIG[1]	I	CONFIG_HOST[1]	Firmware boot options. See also Table 5, Configuration pins.	1V8
9	GPIO_21	I/O	GPIO[21] / W_DISABLE1n	Multi-functional pin: • GPIO • Host indication to disable the Wi-Fi function of the device (input).	VIO
10	WL_HOST_WAKE	I/O	GPIO[15] / CON[5]	Multi-functional pin: • GPIO • Host wake Wi-Fi (output) • Configuration pin CON[5] See also Table 5, Configuration pins. This pin has the same functionality as pin 86.	VIO
11	GPIO_12	I/O	GPIO[12] / UART_DSRn / W_DISABLE2n	Multi-functional pin: • GPIO • UART DSR signal (input) • Host indication to disable the Bluetooth function of the device (input) This pin can also be used as: • Device wake Wi-Fi 1 (input).	VIO
12	BT_HOST_WAKE	I/0	GPIO[16] / CON[6]	Multi-functional pin: • GPIO • Host wake Bluetooth (output) • Configuration pin CON[6] See also Table 5, Configuration pins. This pin has the same functionality as pin 87.	VIO
13	GPIO_31	I/O	GPIO[31] / JTAG_TDO / WCI2_SOUT	Multi-functional pin: • GPIO • JTAG test data (output) • WCI-2 signal (output)	VIO
14	GPIO_30	I/O	GPIO[30] / JTAG_TDI / WCI2_SIN	Multi-functional pin: • GPIO • JTAG test data (input) • WCI-2 signal (input)	VIO
15	PCM_SYNC	I/O	GPIO[7] / I2S_LRCLK / PCM_SYNC	Multi-functional pin: • GPIO • I2S word select / left-right clock can be output (master) or input (slave). • PCM sync can be output (master) or input (slave)	VIO
16	PCM_CLK	I/O	GPIO[6] / I2S_BCLK / PCM_CLK / CON[10]	Multi-functional pin: • GPIO • I2S bit clock can be output (master) or input (slave) • PCM clock can be output (master) or input (slave) • Configuration pin CON[10] See also Table 5, Configuration pins.	VIO

No.	Name	Pin type[2]	Chipset pin	Description	Power domain
17	PCM_OUT	I/O	GPIO[5] / I2S_DOUT / PCM_DOUT / CON[9]	Multi-functional pin: • GPIO • I2S data output • PCM data output • Configuration pin CON[9] See also Table 5, Configuration pins.	VIO
18	PCM_IN	I/O	GPIO[4] / I2S_DIN / PCM_DIN / CON[8]	Multi-functional pin: • GPIO • I2S data input • PCM data input • Configuration pin CON[8] See also Table 5, Configuration pins.	VIO
19	GND	GND		Ground	
20	GND	GND		Ground	
21	ANT2	I/O, RF		Antenna pin: • JODY-W374, JODY-W354: NC • JODY-W377: Bluetooth	
22	GND	GND		Ground	
23	GND	GND		Ground	
24	ANT0	I/O, RF		Antenna pin: • JODY-W374, JODY-W354: Bluetooth and 5 GHz (Path B) Wi-Fi • JODY-W377: 2.4 GHz (Path B) and 5 GHz (Path B) Wi-Fi	
25	GND	GND		Ground	
26	DNC	DNC		Do not connect	
27	GND	GND		Ground	
28	GND	GND		Ground	
29	ANT1	I/O, RF		Antenna pin: • 2.4 GHz (Path A) and 5 GHz (Path A) Wi-Fi	
30	GND	GND		Ground	
31	GND	GND		Ground	
32	GPIO_28	I/0	GPIO[28] / JTAG_TCK	Multi-functional pin: • GPIO • JTAG test data clock (input)	VIO
33	GPIO_29	I/0	GPIO[29] / JTAG_TMS	Multi-functional pin: • GPIO • JTAG controller select (input)	VIO
34	GPIO_2	I/0	GPIO[2]	Multi-functional pin: • GPIO This pin can also be used as: • PTA external radio state signal (input)	VIO
35	GPIO_3	I/0	GPIO[3] / I2S_CCLK / PCM_MCLK	Multi-functional pin: • GPIO • I2S CCLK (output) (optional) • PCM master clock (output) (optional)	VIO
36	BT_UART_TX	I/O	GPIO[8] / UART_SOUT	Multi-functional pin: • GPIO • Fast UART serial data output	VIO

No.	Name	Pin type[2]	Chipset pin	Description	Power domain
37	BT_UART_RX	I/O	GPIO[9] / UART_SIN	Multi-functional pin: • GPIO • Fast UART serial data input	VIO
38	BT_UART_RTS	I/O	GPIO[11] / UART_RTSn	Multi-functional pin: • GPIO • Fast UART active-low request-to-send signal (output)	VIO
39	BT_UART_CTS	I/O	GPIO[10] / UART_CTSn	Multi-functional pin: • GPIO • Fast UART active-low clear-to-send signal (input)	VIO
40	PCIE_PME#	I/O	PCIE_WAKEn	PCIe wake signal (active low) NOTE: Pull-up required on host side	VIO
41	PCIE_CLKREQ#	I/O	PCIE_CLKREQn	PCIe clock request (active low) NOTE: Pull-up required on host side	VIO
42	PCIE_PERST#	I/O	GPIO[20] / PCIE_PERSTn	Multi-functional Pin: • GPIO • PCIe host indication to reset the device (input)	VIO
43	PCIE_REFCLKN	I		PCIE negative differential clock input	1V8
44	PCIE_REFCLKP	I		PCIE positive differential clock input	1V8
45	PCIE_RDN	I		PCIE negative differential data input	1V8
46	PCIE_RDP	I		PCIE positive differential data input	1V8
47	PCIE_TDN	O		PCIE negative differential data output	1V8
48	PCIE_TDP	O		PCIE positive differential data output	1V8
49	GND	GND		Ground	
50	SD_D2	I/O	SD_DAT[2]	SDIO data line bit [2]	1V8
51	SD_D3	I/O	SD_DAT[3]	SDIO data line bit [3]	1V8
52	SD_CMD	I/O	SD_CMD	SDIO command line	1V8
53	SD_CLK	I	SD_CLK	SDIO clock input	1V8
54	SD_D0	I/O	SD_DAT[0]	SDIO data line bit [0]	1V8
55	SD_D1	I/O	SD_DAT[1]	SDIO data line bit [1]	1V8
56	DNC	DNC		Do not connect	
57	DNC	DNC		Do not connect	
58	PD#	I	PDn	Power-down interface of the chipset: • 0 = power-down mode • 1 = normal mode Can accept an input of 1.8 V to 4.5 V. Internal 51 kΩ pull-up to 1V8 on this pin.	1V8
59-64	DNC	DNC		Do not connect	
65	GPIO_13	I/O	GPIO[13] / UART_DTRn	Multi-functional pin: • GPIO • UART DTR signal (output) This pin can also be used as: • Device wake Wi-Fi 2 (input)	VIO
66	GPIO_24	I/O	GPIO[24] / SPI_SI	Multi-functional pin: • GPIO • SPI data input	VIO

No.	Name	Pin type[2]	Chipset pin	Description	Power domain
67	GPIO_25	I/O	GPIO[25] / SPI_CSn	Multi-functional pin: • GPIO • SPI chip select (output)	VIO
68	GPIO_26	I/O	GPIO[26] / SPI_SO / I2C_SDA	Multi-functional pin: • GPIO • SPI data output • I2C data signal (input/output)	VIO
69	GPIO_27	I/O	GPIO[27] / SPI_SCL / I2C_SCL	Multi-functional pin: • GPIO • SPI clock signal (input/output) I2C clock signal (input/output)	VIO
70	GPIO_23	I/O	GPIO[23]	GPIO	VIO
71	GPIO_22	I/O	GPIO[22]	GPIO	VIO
72	RF_CNTL10_N	O	RF_CNTL10_N	RF control output low	VIO
73	RF_CNTL9_N	O	RF_CNTL9_N	RF control output high	VIO
74	RF_CNTL8_N	O	RF_CNTL8_N	RF control output low	VIO
75	RF_CNTL7_N	O	RF_CNTL7_N	RF control output high	VIO
76	DNC	DNC		Do not connect	
77	DNC	DNC		Do not connect	
78	RF_CNTL6_N	O	RF_CNTL6_N	RF control output low	VIO
79	RF_CNTL5_N	O	RF_CNTL5_N	RF control output high	VIO
80	RF_CNTL4_N	O	RF_CNTL4_N	RF control output low	VIO
81	RF_CNTL3_P	O	RF_CNTL3_P	RF control output high	VIO
82	RF_CNTL2_N	O	RF_CNTL2_N	RF control output low	VIO
83	RF_CNTL1_P	O	RF_CNTL1_P	RF control output high	VIO
84	RF_CNTL0_N	O	RF_CNTL0_N	RF control output low	VIO
85	GPIO_14	I/O	GPIO[14] / CON[4]	Multi-functional pin: • GPIO • Configuration pin CON[4] See also Table 5, Configuration pins.	VIO
86	WL_HOST_WAKE	I/O	GPIO[15] / CON[5]	Multi-functional pin: • GPIO • Host wake Wi-Fi (output) • Configuration pin CON[5] See also Table 5, Configuration pins. This pin has the same functionality as pin 10.	VIO
87	BT_HOST_WAKE	I/O	GPIO[16] / CON[6]	Multi-functional pin: • GPIO • Host wake Bluetooth (output), • Configuration pin CON[6]. See also Table 5, Configuration pins. This pin has the same functionality as pin 12.	VIO
88	GPIO_17	I/O	GPIO[17] / CON[7]	Multi-functional pin: • GPIO • Configuration pin CON[7] See also Table 5, Configuration pins. This pin can also be used as: • PTA external radio grant signal (output)	VIO

No.	Name	Pin type[2]	Chipset pin	Description	Power domain
89	GPIO_18	I/O	GPIO[18]	Multi-functional pin: • GPIO This pin can also be used as: • Independent software reset for Wi-Fi subsystem (input) • PTA request from the external radio (input)	VIO
90	GPIO_19	I/O	GPIO[19]	Multi-functional pin: • GPIO This pin can also be used as: • Independent software reset for Bluetooth subsystem (input) • PTA external radio priority signal (input)	VIO
91	GPIO_0	I/O	GPIO[0]	GPIO	VIO
92	GPIO_1	I/O	GPIO[1]	Multi-functional pin: • GPIO This pin can also be used as: • Device wake Bluetooth (input) • PTA external radio frequency signal (input)	VIO
93	DNC	DNC		Do not connect	
94	DNC	DNC		Do not connect	
EP	GND	GND	15 exposed ground/thermal pins. Connect to ground.		

Table 20: JODY-W3 pinout table

4 Electrical specification

⚠ Stressing the device above one or more of the Absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating modules at these or any conditions other than those specified Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Units
3V3	3.3 V analog power supply voltage	-	3.96	V
VIO	1.8 V I/O digital supply voltage	-	1.98	V
	3.3 V I/O digital supply voltage	-	3.63	V
1V8	1.8 V analog power supply voltage	-	2.16	V
$T_{STORAGE}$	Storage temperature	-40	+85	°C

Table 21: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification described in Table 21 must be limited to values within the specified boundaries using appropriate protection devices.

4.2 Maximum ESD ratings

Applicability	Min.	Max.	Units
Human Body Model (HBM), according to AEC-Q100-002.	-2000	+2000	V
Charged Device Model (CDM), according to AEC-Q100-011.	-500	+500	V

Table 22: Maximum ESD ratings

4.3 Operating conditions

Symbol	Parameter	Min.	Typ	Max.	Units
3V3	3.3 V analog power supply voltage	3.14	3.3	3.46	V
VIO	1.8 V I/O digital supply voltage	1.71	1.8	1.89	V
	3.3 V I/O digital supply voltage	3.14	3.3	3.46	V
1V8	1.8 V analog power supply voltage	1.71	1.8	1.89	V
T_A	Ambient operating temperature	-40	-	+85	°C
Ripple Noise	Peak-to-peak voltage ripple on all supply lines	-	-	30	mV

Table 23: Operating conditions

4.4 Digital pad ratings

Symbol	Parameter	VIO	Min.	Max.	Units
V_{IH}	Input high voltage	1.8 V – 3.3 V	0.7*VIO	VIO+0.4	V
V_{IL}	Input low voltage	1.8 V – 3.3 V	-0.4	0.3*VIO	V
V_{HYS}	Input hysteresis	1.8 V – 3.3 V	0.1	-	V
V_{OH}	Output high voltage	1.8 V – 3.3 V	VIO-0.4	-	V
V_{OL}	Output low voltage	1.8 V – 3.3 V	-	0.4	V

Table 24: DC characteristics VIO

4.5 Power consumption

☞ The power consumption data is collected with PCIe-UART interface configuration and at 25 °C ambient temperature.

Parameter	3V3 [mA]	1V8 [mA]	VIO (1.8 V) [mA]
Power sleep mode			
Power down	0.005	0.07	0.003
Wi-Fi only in deep sleep mode (PCIe L1)	0.07	2.52	0.45
Wi-Fi and Bluetooth in deep sleep mode (PCIe L1)	0.16	2.52	0.45
Wi-Fi only in deep sleep mode (PCIe L1.2)	0.07	1.39	0.45
Wi-Fi and Bluetooth in deep sleep mode (PCIe L1.2)	0.16	1.39	0.45
Bluetooth current consumption			
Bluetooth idle	0.5	19.5	0.45
Bluetooth peak TX, DH5	0.5	101	0.45
Bluetooth peak RX, DH5	0.5	35	0.45
Bluetooth LE 1.28s inquiry scan	0.11	1.53	0.45
Bluetooth LE peak TX, L1M	0.5	102	0.45
Bluetooth LE peak RX, L1M	0.5	35	0.45
IEEE power save mode 1x1 RX			
IEEE Power Save DTIM 1 and BT deep sleep, 2GHz 1x1 RX	0.07	5.94	0.45
IEEE Power Save DTIM 3 and BT deep sleep, 2GHz 1x1 RX	0.07	2.9	0.45
IEEE Power Save DTIM 5 and BT deep sleep, 2GHz 1x1 RX	0.07	2.24	0.45
IEEE Power Save DTIM 10 and BT deep sleep, 2GHz 1x1 RX	0.07	2.01	0.45
IEEE Power Save DTIM 1 and BT deep sleep, 5GHz 1x1 RX	0.07	5.35	0.45
IEEE Power Save DTIM 3 and BT deep sleep, 5GHz 1x1 RX	0.07	2.68	0.45
IEEE Power Save DTIM 5 and BT deep sleep, 5GHz 1x1 RX	0.07	2.1	0.45
IEEE Power Save DTIM 10 and BT deep sleep, 5GHz 1x1 RX	0.07	1.83	0.45
IEEE power save mode 2x2 RX			
IEEE Power Save DTIM 1 and BT deep sleep, 2GHz 2x2 RX	0.07	6.48	0.45
IEEE Power Save DTIM 3 and BT deep sleep, 2GHz 2x2 RX	0.07	3.06	0.45
IEEE Power Save DTIM 5 and BT deep sleep, 2GHz 2x2 RX	0.07	2.33	0.45
IEEE Power Save DTIM 10 and BT deep sleep, 2GHz 2x2 RX	0.07	2.05	0.45
IEEE Power Save DTIM 1 and BT deep sleep, 5GHz 2x2 RX	0.07	5.86	0.45
IEEE Power Save DTIM 3 and BT deep sleep, 5GHz 2x2 RX	0.07	2.85	0.45
IEEE Power Save DTIM 5 and BT deep sleep, 5GHz 2x2 RX	0.07	2.2	0.45
IEEE Power Save DTIM 10 and BT deep sleep, 5GHz 2x2 RX	0.07	1.95	0.45
Wi-Fi 2.4 GHz 1x1 RX			
802.11b	0.07	282	0.45
802.11g	0.07	301	0.45
802.11n, HT20	0.07	302	0.45
802.11n, HT40	0.07	314	0.45
Wi-Fi 2.4 GHz 2x2 RX			
802.11b	0.07	319	0.45
802.11g	0.07	322	0.45
802.11n, HT20	0.07	315	0.45
802.11n, HT40	0.07	339	0.45

Parameter	3V3 [mA]	1V8 [mA]	VIO (1.8 V) [mA]
802.11ax, HE20	0.07	298	0.45
802.11ax, HE40	0.07	332	0.45
Wi-Fi 5 GHz 1x1 RX			
802.11n, HT20	0.07	304	0.45
802.11n, HT40	0.07	320	0.45
802.11ax, HE20	0.07	383	0.45
802.11ax, HE40	0.07	348	0.45
802.11ax, HE80	0.07	386	0.45
Wi-Fi 5 GHz 2x2 RX			
802.11n, HT20	0.07	317	0.45
802.11n, HT40	0.07	340	0.45
802.11ax, HE20	0.07	391	0.45
802.11ax, HE40	0.07	365	0.45
802.11ax, HE80	0.07	412	0.45
Active modes			
Wi-Fi 2.4 GHz 1x1 TX			
CCK 11 Mbps, BW20, Ch6, 20 dBm	255	275	0.47
OFDM 6 Mbps, BW20, Ch6, 19 dBm	230	295	0.47
OFDM 54 Mbps, BW20, Ch6, 18 dBm	210	295	0.47
MCS0, 11n HT20, Ch6, 18 dBm	210	295	0.47
MSC7, 11n HT20, Ch6,18 dBm	215	295	0.47
MCS0, 11n HT40, Ch6, 17 dBm	195	305	0.47
MSC7, 11n HT40, Ch6,17 dBm	195	305	0.47
MCS0, 11ax HE20, Ch6, 17 dBm	195	295	0.47
MSC11, 11ax HE20, Ch6,17 dBm	200	305	0.47
MCS0, 11ax HE40, Ch6, 17 dBm	200	310	0.47
MSC11, 11ax HE40, Ch6,17 dBm	200	310	0.47
Wi-Fi 2.4 GHz 2x2 TX			
CCK 11 Mbps, BW20, Ch6, 20 dBm	510	355	0.47
OFDM 6 Mbps, BW20, Ch6, 19 dBm	465	390	0.47
OFDM 54 Mbps, BW20, Ch6, 18 dBm	430	390	0.47
MCS0, 11ax HE20, Ch6, 17 dBm	400	390	0.47
MSC11, 11ax HE20, Ch6,17 dBm	400	395	0.47
MCS0, 11ax HE40, Ch6, 17 dBm	400	410	0.47
MSC11, 11ax HE40, Ch6,17 dBm	400	405	0.47
Wi-Fi 5 GHz 1x1 TX			
MCS0, 11n HT20, Ch100, 17 dBm	220	375	0.47
MCS7, 11n HT20, Ch100, 17 dBm	220	380	0.47
MCS0, 11n HT40, Ch100, 16 dBm	205	385	0.47
MCS7, 11n HT40, Ch100, 16 dBm	200	380	0.47
MCS0, 11ax HE20, Ch100, 15 dBm	195	375	0.47
MCS11, 11ax HE20, Ch100, 15 dBm	195	385	0.47
MCS0, 11ax HE40, Ch100, 15 dBm	195	385	0.47
MCS11, 11ax HE40, Ch100, 15 dBm	195	385	0.47

Parameter	3V3 [mA]	1V8 [mA]	VIO (1.8 V) [mA]
MCS0, 11ax HE80, Ch100, 15 dBm	195	400	0.47
MCS11, 11ax HE80, Ch100, 15 dBm	195	395	0.47
Wi-Fi 5 GHz 2x2 TX			
MCS8, 11n HT20, Ch100, 17 dBm	420	520	0.46
MCS15, 11n HT20, Ch100, 17 dBm	420	615	0.46
MCS8, 11n HT40, Ch100, 16 dBm	390	535	0.45
MCS15, 11n HT40, Ch100, 16 dBm	390	530	0.46
MCS0, 11ac VHT80, Ch100, 16 dBm	390	580	0.45
MCS8, 11ac VHT80, Ch100, 16 dBm	380	575	0.46
MCS0, 11ax HE20, Ch100, 15 dBm	370	515	0.45
MCS11, 11ax HE20, Ch100, 15 dBm	370	520	0.45
MCS0, 11ax HE40, Ch100, 15 dBm	370	535	0.45
MCS11, 11ax HE40, Ch100, 15 dBm	370	530	0.45
MCS0, 11ax HE80, Ch100, 15 dBm	370	590	0.45
MCS11, 11ax HE80, Ch100, 15 dBm	370	580	0.45
Wi-Fi concurrent dual-band mode 1x1 TX			
2.4 GHz, 11n HT20, MCS7, 16 dBm 5 GHz, 11ax HE80, MCS11, 12 dBm	320	510	0.46
2.4 GHz, 11ax HE20, MCS11, 14 dBm 5 GHz, 11ac VHT40, MCS9, 14 dBm	310	510	0.46
2.4 GHz, 11n HT40, MCS7, 16 dBm 5 GHz, 11ac VHT80, MCS9, 12 dBm	345	510	0.46
2.4 GHz, 11n HT20, MCS7, 16 dBm 5 GHz, 11ac VHT20, MCS8, 14 dBm	360	500	0.46
Wi-Fi concurrent dual-band mode 2x2 TX			
2.4 GHz, 11n HT20, MCS15, 16 dBm 5 GHz, 11ax HE80, MCS11, 12 dBm	620	735	0.47
2.4 GHz, 11ax HE20, MCS11, 14 dBm 5 GHz, 11ac VHT40, MCS9, 14 dBm	635	750	0.47
2.4 GHz, 11n HT40, MCS15, 16 dBm 5 GHz, 11ac VHT80, MCS9, 12 dBm	625	735	0.47
2.4 GHz, 11n HT20, MCS15, 16 dBm 5 GHz, 11ac VHT20, MCS8, 14 dBm	640	730	0.47
Maximum current consumption @ 85°C			
Maximum current during 1x1 CDW operation	400	660	0.55
Maximum current during 2x2 CDW operation	800	1300	0.55

Table 25: Wi-Fi + Bluetooth power consumption

4.6 Radio specifications

4.6.1 Bluetooth

Parameter	Specification
RF Frequency Range	2.4 – 2.5 GHz
Supported Modes	Bluetooth 5.3 Bluetooth Low Energy (LE) - LE long range - Shared RF with BR/EDR - 2 Mbps LE
Modulation	1 Mbit/s: GFSK (BR) 2 Mbit/s: π/4 DQPSK (EDR) 3 Mbit/s: 8DQPSK (EDR)
Transmit Power	BDR: +10 dBm ± 2 dB
	EDR: +7 dBm ± 2 dB
	Bluetooth LE: +8 dBm ± 2 dB
Sensitivity	DH5: -94 dBm (De-sense of 5.5 dB at 2440 MHz, 2 dB at 2480 MHz)
	3DH5: -87 dBm (De-sense of 6 dB at 2440 MHz, 2 dB at 2480 MHz)
	LR8: -106 dBm (De-sense of 11dB at 2440 MHz, 5 dB at 2480 MHz)
	LR2: -105 dBm (De-sense of 11dB at 2440 MHz, 5 dB at 2480 MHz)
	LE1M: -101 dBm (De-sense of 10 dB at 2440 MHz, 4 dB at 2480 MHz)
	LE2M: -98 dBm (De-sense of 5 dB at 2440 MHz, 1 dB at 2480 MHz)

Table 26: Bluetooth radio parameters

4.6.2 Wi-Fi

JODY-W3 series modules support concurrent dual-band Wi-Fi with 802.11a/b/g/n/ac/ax operation in the 2.4 GHz and 5 GHz radio bands.

Parameter	Operation Mode	Specification
RF Frequency range	802.11b/g/n/ax	2.400 – 2.500 GHz
	802.11a/n/ac/ax	4.900 – 5.925 GHz
Modulation	802.11b	CCK and DSSS
	802.11a/g/n/ac/ax	OFDM
Supported data rates	802.11b	1, 2, 5.5, 11 Mbit/s
	802.11a/g	6, 9, 12, 18, 24, 36, 48, 54 Mbit/s
	802.11n SISO and MIMO	MCS0 – MCS15 and MCS 32 (duplicate 6 Mbps)
	802.11ac SISO and MIMO	MCS0 – MCS9
	802.11ax SISO and MIMO	MCS0 – MCS11
Supported channel bandwidth	802.11ac/ax	20, 40, 80 MHz
Supported guard interval (GI)	802.11n/ac	400, 800 ns
	802.11ax	800, 1600 ns
	802.11ac	Short guard interval supported

Table 27: Wi-Fi radio parameters

Parameter		Operation Mode	802.11 EVM limit	Specification (typ. Output power tolerance ± 2 dB)
Maximum transmit power	2.4 GHz	DSSS/CCK	-9.1 dB	19 dBm
		OFDM, BPSK	-8 dB	17 dBm
		OFDM, QPSK	-13 dB	17 dBm
		OFDM, 16-QAM	-19 dB	17 dBm
		OFDM, 64-QAM, 3/4	-25 dB	16 dBm
		OFDM, 64-QAM, 5/6	-27 dB	16 dBm
		OFDM, 256-QAM, 3/4	-30 dB	16 dBm
		OFDM, 256-QAM, 5/6	-32 dB	16 dBm
	5 GHz	OFDM, BPSK	-5 dB	16 dBm
		OFDM, QPSK	-13 dB	16 dBm
		OFDM, 16-QAM	-19 dB	16 dBm
		OFDM, 64-QAM, 3/4	-25 dB	16 dBm
		OFDM, 64-QAM, 5/6	-27 dB	15 dBm
		OFDM, 256-QAM, 3/4	-30 dB	15 dBm
		OFDM, 256-QAM, 5/6	-32 dB	14 dBm
		OFDMA, 1024-QAM, 3/4	-35 dB	13 dBm
		OFDMA, 1024-QAM, 5/6	-35 dB	13 dBm

Table 28: Wi-Fi radio maximum transmit power parameter

Parameter	Band	Operating mode	Data rate	Bandwidth	Specification
Sensitivity	2.4 GHz[3]	802.11b	1 Mbps / 2 Mbps	20 MHz	-97 dBm / -94 dBm
			5.5 Mbps / 11 Mbps		-92 dBm / -89 dBm
		802.11g	6 Mbps / 9 Mbps	20 MHz	-91 dBm / -90 dBm
			12 Mbps / 18 Mbps		-89 dBm / -87 dBm
			24 Mbps / 36 Mbps		-84 dBm / -80 dBm
			48 Mbps / 54 Mbps		-76 dBm / -75 dBm
		802.11n	MCS0 / MCS1	20 MHz	-91 dBm / -88 dBm
			MCS2 / MCS3		-86 dBm / -84 dBm
			MCS4 / MCS5		-80 dBm / -76 dBm
			MCS6 / MCS7		-74 dBm / -73 dBm
			MCS0 / MCS1	40 MHz	-89 dBm / -86 dBm
			MCS2 / MCS3		-84 dBm / -81 dBm
			MCS4 / MCS5		-77 dBm / -73 dBm
			MCS6 / MCS7		-72 dBm / -70 dBm
		802.11ax	MCS0 / MCS1	20 MHz	-91 dBm / -89 dBm
			MCS2 / MCS3		-87 dBm / -84 dBm
			MCS4 / MCS5		-81 dBm / -77 dBm
			MCS6 / MCS7		-76 dBm / -75 dBm
			MCS8 / MCS9		-70 dBm / -69 dBm
			MCS10 / MCS11		-63 dBm / -62 dBm
			MCS0 / MCS1	40 MHz	-89 dBm / -86 dBm
			MCS2 / MCS3		-85 dBm / -81 dBm

[3] The LTE coexistence variants JODY-W354-20A and JODY-W374-20A have up to 2 dB less sensitivity in the 2.4 GHz band.

Parameter	Band	Operating mode	Data rate	Bandwidth	Specification
			MCS4 / MCS5		-79 dBm / -75 dBm
			MCS6 / MCS7		-73 dBm / -72 dBm
			MCS8 / MCS9		-68 dBm / -66 dBm
			MCS10 / MCS11		-63 dBm / -62 dBm
	5 GHz	802.11a	6 Mbps / 9 Mbps	20 MHz	-90 dBm / -89 dBm
			12 Mbps / 18 Mbps		-88 dBm / -86 dBm
			24 Mbps / 36 Mbps		-83 dBm / -80 dBm
			48 Mbps / 54 Mbps		-75 dBm / -74 dBm
		802.11n	MCS0 / MCS1	20 MHz	-90 dBm / -88 dBm
			MCS2 / MCS3		-85 dBm / -82 dBm
			MCS4 / MCS5		-79 dBm / -75 dBm
			MCS6 / MCS7		-73 dBm / -72 dBm
			MCS0 / MCS1	40 MHz	-88 dBm / -85 dBm
			MCS2 / MCS3		-83 dBm / -80 dBm
			MCS4 / MCS5		-77 dBm / -72 dBm
			MCS6 / MCS7		-71 dBm / -70 dBm
		802.11ac	MCS0 / MCS1	20 MHz	-90 dBm / -88 dBm
			MCS2 / MCS3		-85 dBm / -83 dBm
			MCS4 / MCS5		-79 dBm / -75 dBm
			MCS6 / MCS7		-73 dBm / -72 dBm
			MCS8		-68 dBm
			MCS0 / MCS1	40 MHz	-88 dBm / -85 dBm
			MCS2 / MCS3		-83 dBm / -80 dBm
			MCS4 / MCS5		-76 dBm / -72 dBm
			MCS6 / MCS7		-71 dBm / -70 dBm
			MCS8 / MCS9		-65 dBm / -64 dBm
			MCS0 / MCS1	80 MHz	-85 dBm / -82 dBm
			MCS2 / MCS3		-80 dBm / -77 dBm
			MCS4 / MCS5		-73 dBm / -69 dBm
			MCS6 / MCS7		-68 dBm / -66 dBm
			MCS8 / MCS9		-62 dBm / -61 dBm
		802.11ax	MCS0 / MCS1	20 MHz	-90 dBm / -88 dBm
			MCS2 / MCS3		-87 dBm / -83 dBm
			MCS4 / MCS5		-81 dBm / -76 dBm
			MCS6 / MCS7		-75 dBm / -74 dBm
			MCS8 / MCS9		-69 dBm / -68 dBm
			MCS10 / MCS11		-63 dBm / -62 dBm
			MCS0 / MCS1	40 MHz	-88 dBm / -86 dBm
			MCS2 / MCS3		-84 dBm / -81 dBm
			MCS4 / MCS5		-78 dBm / -74 dBm
			MCS6 / MCS7		-73 dBm / -72 dBm
			MCS8 / MCS9		-67 dBm / -66 dBm
			MCS10 / MCS11		-62 dBm / -59 dBm
			MCS0 / MCS1	80 MHz	-85 dBm / -83 dBm
			MCS2 / MCS3		-81 dBm / -77 dBm

Parameter	Band	Operating mode	Data rate	Bandwidth	Specification
			MCS4 / MCS5		-76 dBm / -71 dBm
			MCS6 / MCS7		-70 dBm / -69 dBm
			MCS8 / MCS9		-65 dBm / -63 dBm
			MCS10 / MCS11		-59 dBm / -57 dBm

Table 29: Wi-Fi radio sensitivity

4.7 LTE Coexistence performance

4.7.1 Wi-Fi receiver performance with LTE coexistence filter

Figure 16 shows the Wi-Fi sensitivity of JODY-W3 modules including dedicated high performance coexistence filter in the presence of an LTE interferer allocated in any of the bands 7, 38, 40 or 41. The modules are specified according to Table 1.

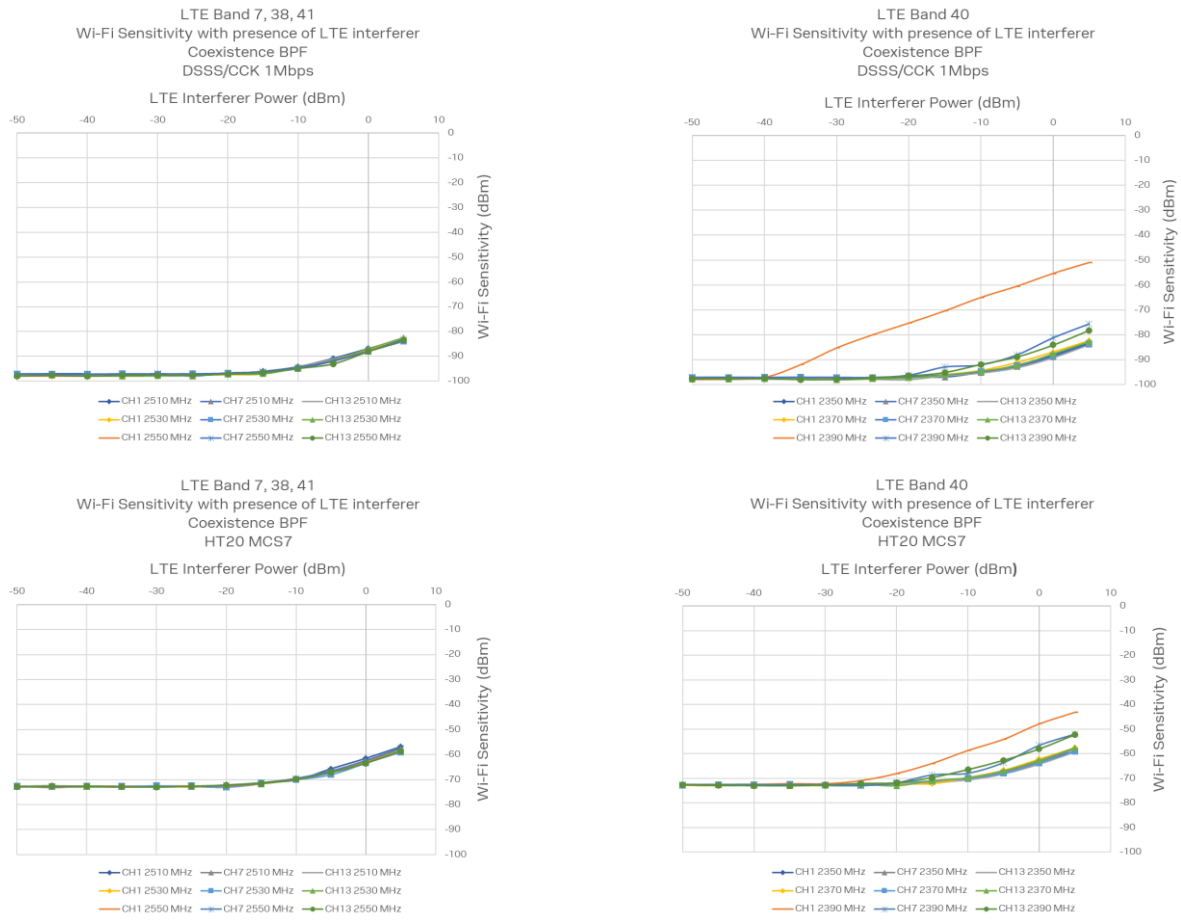

Figure 16: Wi-Fi sensitivity of JODY-W3 modules with dedicated coexistence filter

4.7.2 Wi-Fi receiver performance without LTE coexistence filter

Figure 17 shows the Wi-Fi sensitivity of JODY-W3 modules, including data without a coexistence filter in the presence of an LTE interferer allocated in bands 7, 38, 40, and 41. JODY-W3 modules are specified in accordance with Table 1.

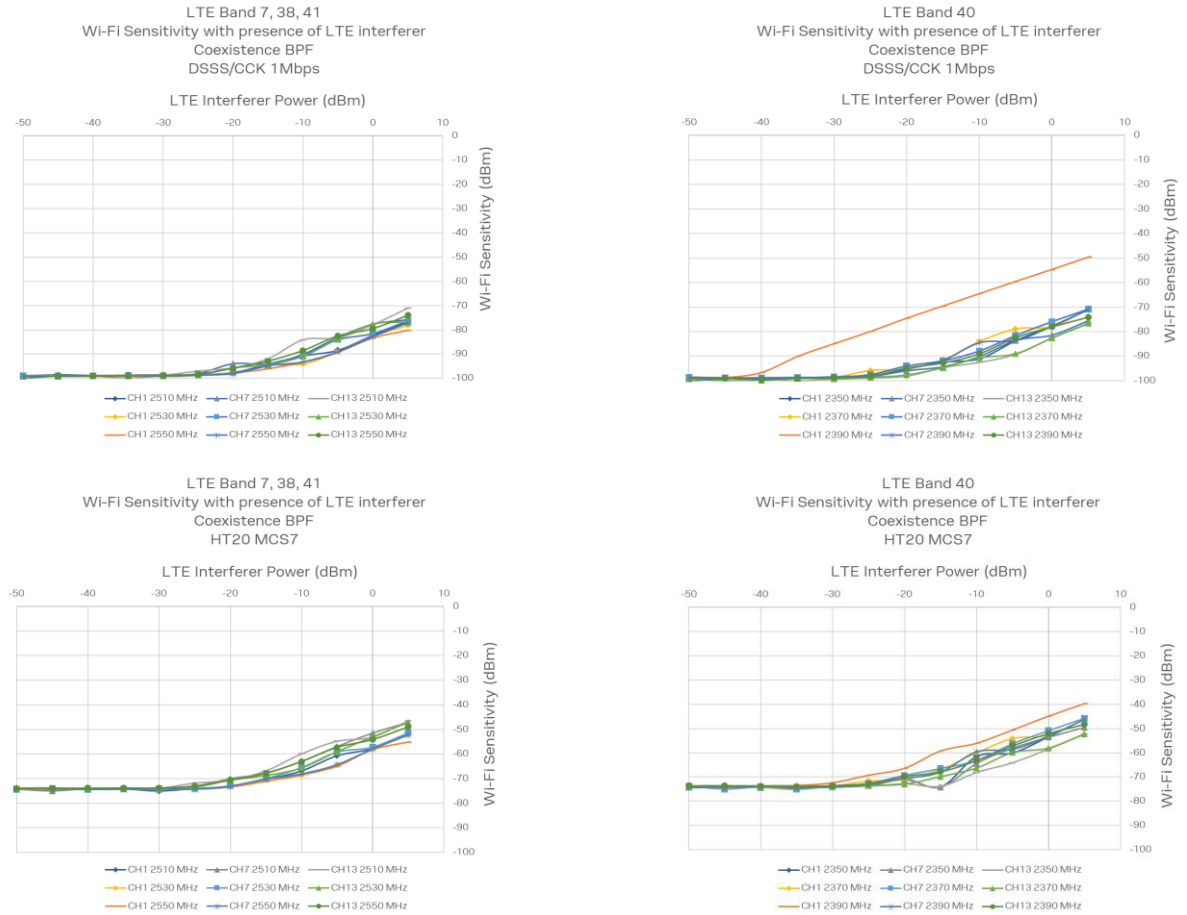

Figure 17: Wi-Fi sensitivity of JODY-W3 modules without dedicated coexistence filter

5 Software

JODY-W3 series modules are based on the NXP AW690/88Q9098/88W9098 chipsets, and the drivers and firmware required to operate JODY-W3 series modules are developed by NXP. A firmware binary is downloaded by the host operating system driver at start-up.

The following software options are available for the JODY-W3 module:

- Open-source Linux/Android driver (`mxm_mwifiex`) for mainstream use is available free of charge and already integrated into the Linux BSP for NXP i.MX application processors
- Proprietary Linux/Android drivers providing different feature packs

The proprietary drivers are distributed by u-blox to customers that have signed a limited use license agreement (LULA-M) with u-blox. It can be signed electronically. The driver package is also available directly from NXP. Contact your local support team for further information.

The software packages typically include:

- Dedicated Linux kernel drivers for Wi-Fi and Bluetooth in source code
- Dedicated firmware images, which will be uploaded to the device during initialization
- Various configuration tools
- Laboratory and manufacturing tools for RF testing

6 Mechanical specifications

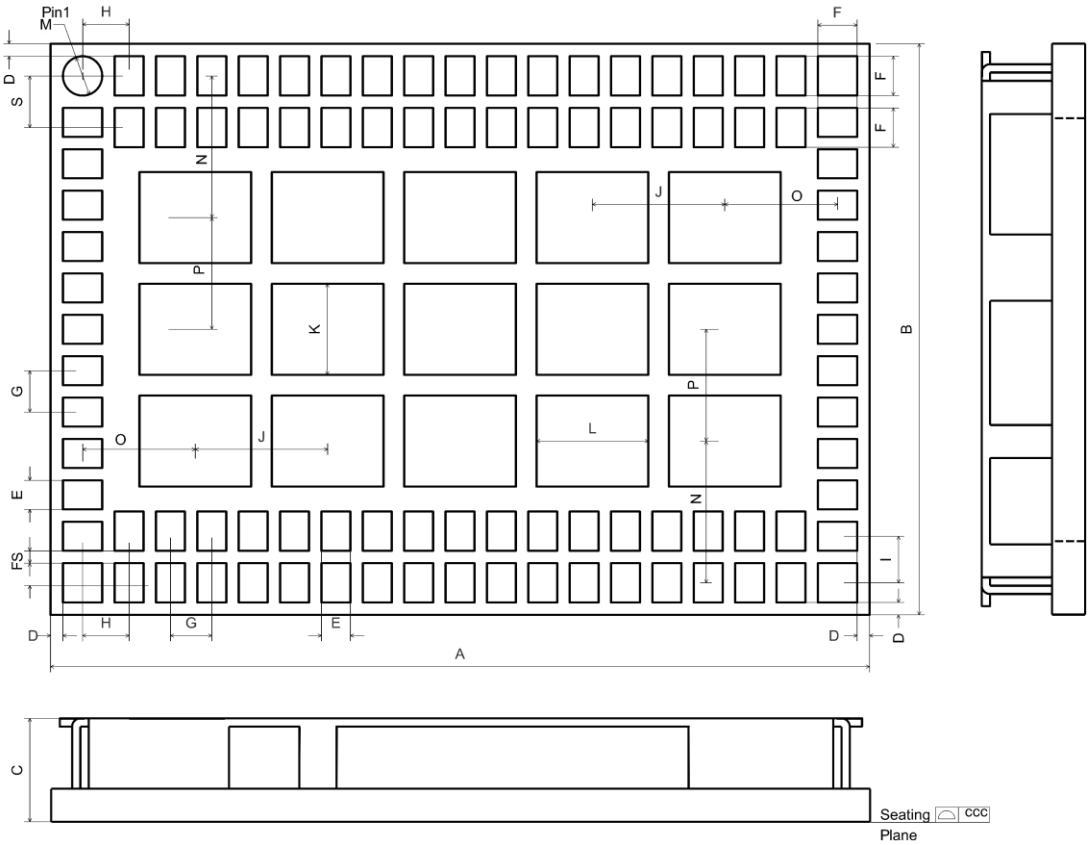

Figure 18: JODY-W3 series dimensions (bottom view)

Parameter	Description	Typical		Tolerance	
A	Module Length [mm]	19.8	(779.5 mil)	+0.35/-0.10	(+13.8/-3.9 mil)
B	Module Width [mm]	13.8	(543.3 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
C	Module Thickness [mm]	2.5	(98.4 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
ccc	Seating Plane Coplanarity [mm]	<0.1	(3.94 mil)		
D	PCB Edge to Pin Edge [mm]	0.3	(11.8 mil)	+0.20/-0.20	(+7.9/-7.9 mil)
E	Pin Width [mm]	0.7	(27.6 mil)	+0.05/-0.05	(+2.0/-2.0 mil)
F	Pin Length [mm]	0.95	(37.4 mil)	+0.05/-0.05	(+2.0/-2.0 mil)
G	Pin to Pin Pitch [mm]	1.0	(39.4 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
H	Horizontal Corner Pin to Pin Pitch [mm]	1.125	(44.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
I	Lateral Corner Pin to Pin Pitch [mm]	1.125	(44.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
J	Horizontal Thermal Pads Pitch [mm]	3.2	(126.0 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
K	Thermal Pad Height [mm]	2.2	(86 6 mil)	+0.10/-0.10	(+3.9/-3.9 mil)
L	Thermal Pad Length [mm]	2.7	(106.3 mil)	+0.10/-0.10	(+3.9/-3.9 mil)
M	Pin 1 Diameter [mm]	0.95	(37.4 mil)	+0.05/-0.05	(+2.0/-2.0 mil)
N	Horizontal Pin to Thermal Pad Pitch [mm]	3.425	(134.8 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
O	Lateral Pin to Thermal Pad Distance [mm]	2.725	(107.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
P	Lateral Thermal Pads Pitch [mm]	2.7	(106.3 mil)	+0.02/-0.02	(+0.8/-0.8 mil)
S	Horizontal Pins Row Pitch [mm]	1.25	(49.2 mil)	+0.02/-0.02	(+0.8/-0.8 mil)

Table 30: Description of dimensions parameters

7 Qualification and approvals

7.1 Country approvals

Table 31 describes the status of JODY-W3 module certification in each country/region.

Country/region	JODY-W354 / JODY-W374	JODY-W377
Europe	Approved	Approved
Great Britain	Approved	Approved
USA	Approved	Approved
Canada	Approved	Approved

Table 31: Country approval status

Additional country certifications can be progressed upon request. Contact your local support team for further information.

☞ For detailed information about the regulatory requirements that must be met when using JODY-W3 modules in an end product, see the system integration manual [2].

7.2 Approved antennas

JODY-W3 has been tested and approved for Bluetooth and Wi-Fi operation in the 2.4 GHz band and Wi-Fi operation in the 5 GHz band using the approved antennas described in the JODY-W3 system integration manual [2].

For information about the specifications that must be fulfilled in an end product utilizing the JODY-W3 radio type approval, see the JODY-W3 antenna reference design application note [8]. The JODY-W3 antenna reference design application note provides PCB layout details and electrical specifications.

7.3 Bluetooth qualification

JODY-W3 series is qualified for Bluetooth 5.3 "Controller Subsystem" operation and is listed as a qualified design (QD ID: 196269) with the Bluetooth Special Interest Group (SIG). This means that there is no need to do any further qualification if the module is combined with a host stack that is qualified for Bluetooth as a "Host Subsystem".

8 Product handling

8.1 Packaging

For efficient production, production lot set-up and tear-down, JODY-W3 series modules are delivered as hermetically sealed devices on tape and reel. For more information about the packaging, shipment, storage, and handling see the Packaging information reference guide [1].

8.1.1 Reels

JODY-W3 series modules are deliverable in quantities of 500 pieces on a reel. The modules are shipped on Type A4 reels, as described in the Packaging information reference guide [1].

8.1.2 Tapes

The orientation of the module and the dimensions of the tapes are shown in Figure 19.

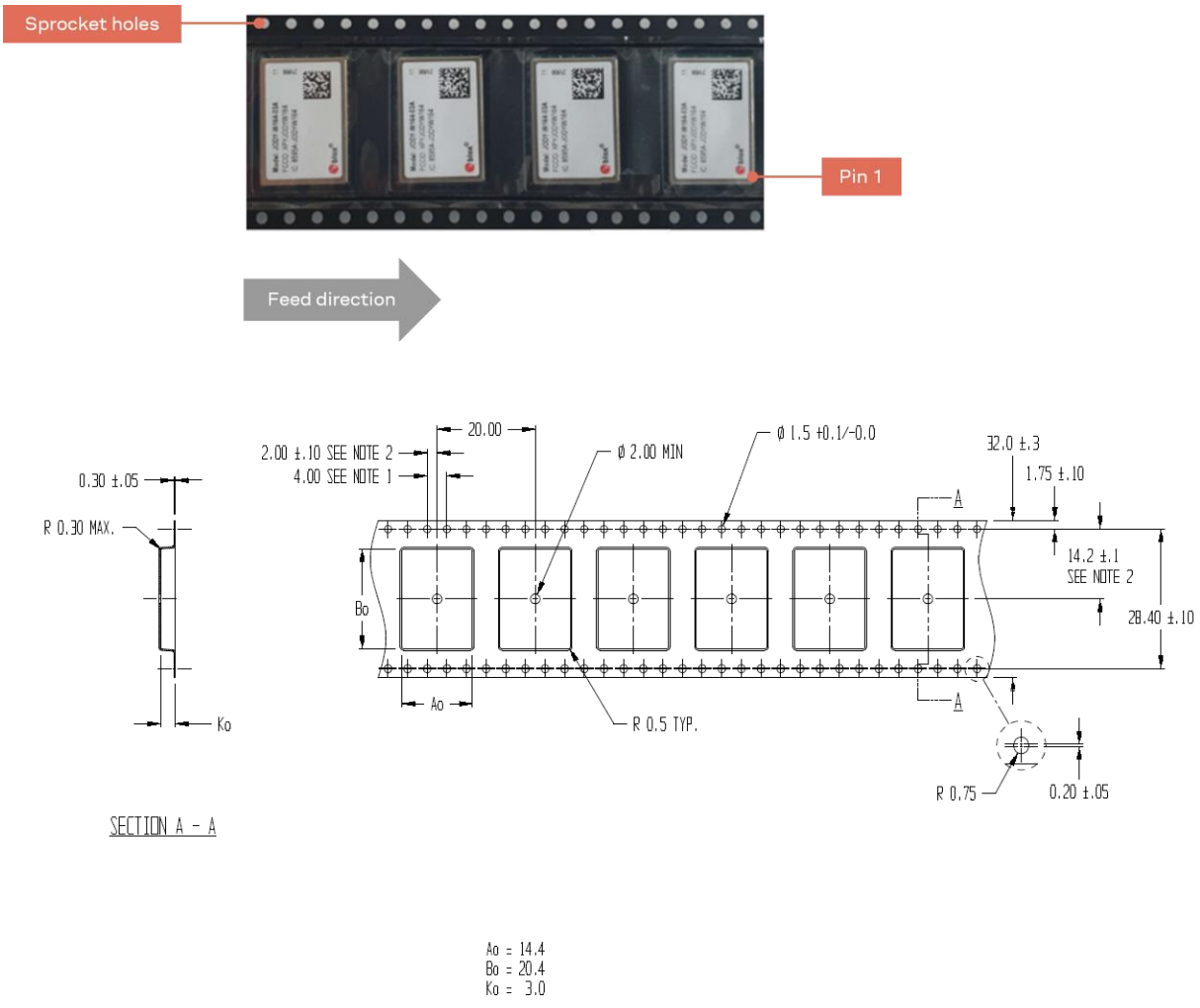

Figure 19: JODY-W3 tape dimensions

8.2 Moisture sensitivity levels

⚠ JODY-W3 series automotive-grade modules are rated at moisture sensitivity level 3. JODY-W3 series professional-grade are rated at moisture sensitivity level 4. A warning to highlight the moisture and static sensitivity risk is carried on each Moisture Barrier Bag (MBB) that protects the modules during shipping.

⚠ In factory conditions with maximum temperature and relative humidity of 30 °C/60%RH, modules rated at MSL3 must be mounted within 168 hours after opening the dry pack. Otherwise, the modules must be stored at less than 10%RH. In the same conditions, MSL4 modules must be mounted within 72 hours after opening the dry pack. Modules require baking if the humidity indicator card shows more than 10% when read at 23±5°C, or if any of the conditions cannot be met. Refer to J-STD-033B standards for further information about the bake procedure.

For more information about MSL (Moisture Sensitivity Level), labeling, and storage, see also the Product packaging reference guide [1].

8.3 Reflow soldering

JODY-W3 series modules are approved for two-time reflow processes.

⚠ Reflow soldering profiles must be chosen in accordance with u-blox soldering recommendations described in the system integration manual [2]. Failure to observe these recommendations can result in severe damage to the product.

8.4 ESD handling precautions

⚠ JODY-W3 series modules are electrostatic sensitive devices (ESD) that demand adherence to special ESD precautions. Failure to observe these precautions can result in severe damage to the product.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates JODY-W3 series modules. ESD precautions should be implemented on the application board where the module is mounted.

For further information about the handling of JODY-W3 series modules, see also the JODY-W3 system integration manual [2].

9 Labeling and ordering information

9.1 Product labeling

The labels applied to JODY-W3 series modules include important product information.

Figure 20 shows the label applied to JODY-W3 series modules. Each of the given label references are described in Table 32.

Figure 20: JODY-W3 series sample label

The various label components are shown in Table 32.

Reference	Description
1	Text in bold font: “Model:” type number with the product version
2	Minor product version (xx)
3	Date of production encoded YY/WW (year/week)
4	Certification IDs for FCC and IC
5	Data Matrix with unique serial number comprising 19 alphanumeric symbols: - The first 3 symbols are used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant. - The following 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF, and The last 4 symbols represent the hardware and firmware version encoded HHFF.
6	u-blox logo – with red dot showing the position of pin 1

Table 32: JODY-W3 series label description

9.2 Product identifiers

Table 33 describes the three product identifiers: specifically, the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Model name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products.	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade.	PPPP-TGVV-TTQ
Type number	Comprises the model name and ordering code – with additional identifiers to describe minor product versions.	PPPP-TGVV-TTQ-XX

Table 33: Product code formats

Table 34 describes each part of the product code.

Code	Meaning	Example
PPPP	Form factor	JODY
TG	Platform T – Dominant technology, For example, W: Wi-Fi, B: Bluetooth G – Generation	W3
VV	Variant based on the same platform; range [00...99]	74
TT	Major Product Version	00
Q	Quality grade A: Automotive B: Professional C: Standard	A
XX	Minor product version (not relevant for certification)	00

Table 34: Part identification code

9.3 Ordering codes

Ordering Code	Product name	Product
JODY-W354-00A	JODY-W354-A	Automotive grade module with two antenna pins and concurrent dual-band 1x1 2.4 GHz and 1x1 5 GHz 802.11ax, Bluetooth/Bluetooth LE 5.3. Operational temperature -40 ^{0}C to +85 ^{0}C, NXP chipset AW690.
JODY-W354-20A	JODY-W354-A	Automotive grade module with two antenna pins and concurrent dual-band 1x1 2.4 GHz and 1x1 5 GHz 802.11ax, Bluetooth/Bluetooth LE 5.3. Operational temperature -40 ^{0}C to +85 ^{0}C, NXP chipset AW690, LTE filter for 2.4 GHz Wi-Fi.
JODY-W374-00A	JODY-W374-A	Automotive grade module with two antenna pins and concurrent dual-band 1x1 2.4 GHz and 2x2 5 GHz 802.11ax, Bluetooth/Bluetooth LE 5.3. Operational temperature -40 ^{0}C to +85 ^{0}C, NXP chipset 88Q9098.
JODY-W374-20A	JODY-W374-A	Automotive grade module with two antenna pins and concurrent dual-band 1x1 2.4 GHz and 2x2 5 GHz 802.11ax, Bluetooth/Bluetooth LE 5.3. Operational temperature -40 ^{0}C to +85 ^{0}C, NXP chipset 88Q9098, LTE filter for 2.4 GHz Wi-Fi.
JODY-W374-00B	JODY-W374	Professional grade module with two antenna pins and concurrent dual-band 1x1 2.4 GHz and 2x2 5 GHz 802.11ax, Bluetooth/Bluetooth LE 5.3. Operational temperature -40 ^{0}C to +85 ^{0}C, NXP chipset 88W9098.
JODY-W377-00A	JODY-W377-A	Automotive grade module with three antenna pins and concurrent dual-band 2x2 2.4 GHz and 2x2 5 GHz 802.11ax, Bluetooth/Bluetooth LE 5.3. Operational temperature -40 ^{0}C to +85 ^{0}C, NXP chipset 88Q9098.
JODY-W377-00B	JODY-W377	Professional grade module with three antenna pins and concurrent dual-band 2x2 2.4 GHz and 2x2 5 GHz 802.11ax, Bluetooth/Bluetooth LE 5.3. Operational temperature -40 ^{0}C to +85 ^{0}C, NXP chipset 88W9098.

Table 35: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
AC	Alternating Current
BT	Bluetooth
CMD	Command
DC	Direct Current
DNC	Do not connect
FCC	Federal Communications Commission
FIFO	First In, First Out
GI	Guard interval
GND	Ground
GPIO	General-purpose input/output
ISED	Innovation, Science and Economic Development Canada
ISM	Industrial, scientific and medical
LTE	Long Term Evolution
LULA	Limited Use License Agreement
MIMO	Multiple Input Multiple Output
MSL	Moisture sensitivity level
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCN	Product Change Notification
PCM	Pulse-code modulation
RED	Radio Equipment Directive
RF	Radio Frequency
RH	Relative humidity
RoHS	Restriction of Hazardous Substances
SAR	Specific Absorption Rate
SCO	Synchronous Connection-Oriented
SDIO	Secure Digital Input Output
SISO	Single-input single-output
SMD	Surface-mount Device
STA	Station
TBD	To be defined
UART	Universal Asynchronous Receiver/Transmitter
WLAN	Wireless Local Area Network

Table 36: Explanation of the abbreviations and terms used

Related documents

[1] Packaging information reference guide, UBX-14001652
[2] JODY-W3 series system integration manual, UBX-19011209
[3] JODY-W3 Declaration of Conformity, UBX- 22018374
[4] 2195630-1, TE connectivity, Data Sheet
[5] 001-0009, TE connectivity, Data Sheet
[6] 001-0012, TE connectivity, Data Sheet
[7] JODY-W3 UKCA Declaration of Conformity, UBX-22036490
[8] JODY-W3 antenna reference design application note, UBX-22022630

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	11-Jul-2019	mhei	Initial release.
R02	16-Dec-2019	mhei	Added JODY-W377 variant
R03	20-May-2020	mhei	Product status “Prototype”
R04	10-May-2021	vbak, mzes	Updated the mechanical specifications in section 6. Added reserved MAC addresses in section 1.7. Added power consumption and RX-sensitivity data. Corrected configuration pins in Table 5.
R05	21-Jan-2022	mhei, mzes	Updated Software section. Updated SDIO timing diagrams. Updated mechanical drawing and PCIe specification. Updated timing in PCM interface. Removed ambiguous description of operating condition ranges in Electrical specifications and information describing ESD handling precautions duplicated in the system integration manual [2]. Updated information describing Moisture sensitivity levels, Reflow soldering, and ESD handling precautions.
R06	27-Jan-2022	mzes	Bluetooth specification updated to 5.3, as described in previous document release. Corrected previously incorrect statement in Wi-Fi features describing SDIO support for recently released JODY-W354-A module. Added data for peak current during concurrent dual band, 1x1 TX operation in Table 25: Wi-Fi + Bluetooth power consumption.
R07	21-Apr-2022	mzes	Updated product status to Engineering Samples for JODY-W374 and JODY-W377 variants.
R08	28-Sep-2022	mzes	Added new LTE coexistence variants W354-20A and W374-20A. Revised pinout table. Added coexistence interfaces and power consumption values. Updated module width tolerance in Table 30: Description of dimensions parameters. Updated contact information.
R09	9-Dec-2022	mhei	Added Great Britain regulatory compliance, Certification in other countries, and Bluetooth qualification. Included minor revisions to product descriptions in Ordering codes.
R10	26-May-2023	mzes	Updated module orientation in Packaging. Removed 2.4G 11ac sensitivity values in Wi-Fi radio sensitivity table data, Table 29. Updated contact information. Removed regulatory requirements (now described in the SIM) with summary Qualification and approvals information.
R11	22-May-2024	frca	Status for all variants changed from “Initial Production” to “Mass Production”

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