M2-MAYA-W1

M.2 card for the MAYA-W1 Wi-Fi 4 and Bluetooth 5.2 module

Data sheet

Abstract

This technical data sheet describes the M2-MAYA-W1 card module which offers 1x1 802.11a/b/g/n and dual-mode Bluetooth 5.2 in an M.2 Key E form factor. The M2-MAYA-W1 card provides all the features and functionality supported in the MAYA-W1 module, with the added benefits associated with easy installation and replacement. The card can be inserted in a standard M.2 Key E slot without the need to solder the module on a host or carrier PCB.

Document information

Title	**M2-MAYA-W1**	
Subtitle	M.2 card for the MAYA-W1 Wi-Fi 4 and Bluetooth 5.2 module	
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Product status	Corresponding content status	
Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Chipset	Type number	IN/PCN reference	Product status
M2-MAYA-W161	NXP IW416	M2-MAYA-W161-00C-00	N/A	Initial production

Contents

1   Functional description

1.1   Overview

The M2-MAYA-W1 card features the MAYA-W1 multi-radio module, based on the NXP IW416 chipset. This Type 2230 Key E M.2 card supports all features and functionality of the module on a convenient expansion card that plugs directly to the host platform.

MAYA-W1 modules can be operated in the following modes:

- Wi-Fi 1x1 802.11a/b/g/n in 2.4 GHz or 5 GHz bands
- Dual-mode Bluetooth 5.2 (BR/EDR and BLE), can be operated simultaneously with Wi-Fi

Even though the M2-MAYA-W1 card is of standard grade, the module variant used on the card is MAYA-W161-professional grade module.

1.2   Product features

As the M2-MAYA-W1 card supports all of the features that the integrated MAYA-W1 module supports, this document aims to describe the extended features of the M2-MAYA-W1 card specifically. For more information about the MAYA-W1 module, see the MAYA-W1 series data sheet [1]. Table 1 describes the features of the card.

	M2-MAYA-W161
Grade	
Automotive	
Professional	
Standard	•
Radio	
Chip inside	NXP IW416
Bluetooth qualification	v5.2
Bluetooth profiles	HCI
Bluetooth BR/EDR	•
Bluetooth Low Energy	•
Wi-Fi 4 IEEE 802.11 standards	a/b/g/n
Wi-Fi frequency band [GHz]	2.4 and 5
Bluetooth output power conducted [dBm]	10
Wi-Fi output power conducted [dBm]	18
Antenna type	2 U-FL connectors
OS support	
Android / Linux drivers (from u-blox)	•
RTOS (via NXP i.MX RT MCUs)	•
Interfaces	
High-speed UART (Bluetooth)	1
PCM, I2S (Bluetooth audio)	1
SDIO (Wi-Fi) [version]	3.0
Features	
Micro Access Point [max connects]	8
Wi-Fi direct	•
WPA3	•
RF calibration in OTP	•
Programmed MAC address	•

Table 1: Key features of the M2-MAYA-W1 module

1.3   Product description

Product name	Description
M2-MAYA-W161	Standard grade M.2 card module equipped with two separate antenna connectors: one for 2.4 GHz and 5 GHz 802.11 a/b/g/n and another for Bluetooth/Bluetooth Low Energy (LE) 5.2). The module integrates the NXP IW416 chipset.

Table 2: Product description

1.4   Block diagram

Figure 1 shows the block diagram of the M2-MAYA-W161 card that integrates the MAYA-W161 module and includes two antenna connectors for attaching two external antennas: one for Wi-Fi and another for Bluetooth.
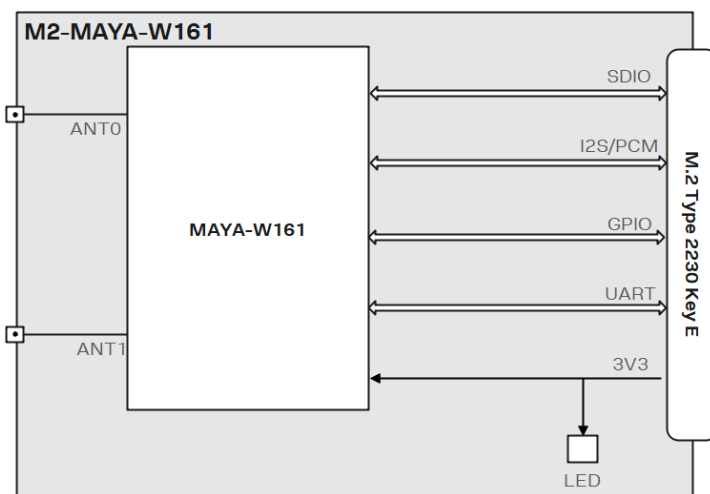
Figure 1: Block diagram of the M2-MAYA-W161 card module

2   Interfaces

The M2-MAYA-W1 card supports all MAYA-W1 module interfaces. For more information about these interfaces, see the MAYA-W1 series data sheet [1].

2.1   Boot configuration pins

By default, the M2-MAYA-W1 card is configured for using the SDIO interface for Wi-Fi and the UART interface for Bluetooth.

Host interface selection and firmware boot options are selected using the MAYA-W1 module configuration pin **CONFIG[1:0]**. The configuration settings for the available boot options are shown in Table 3.

CONFIG[1]	CONFIG[0]	Wi-Fi	Bluetooth	Number of SDIO functions
1	0	SDIO	UART	1 (Wi-Fi)

Table 3: Firmware boot options of the MAYA-W1 module

The M2-MAYA-W1 card supports the same boot options as the MAYA-W1 module. To set the **CONFIG[1:0]** configuration pin to logic-low level ("0"), it must be pulled down with a 51 kΩ resistor to GND. MAYA-W1 has an internal pull-up resistor connected to this pin and as a result, no external pull-up resistor is required to set the configuration pin to logic-high level ("1").

Figure 2 shows the "10" default configuration used to select the SDIO interface for Wi-Fi and UART interface for Bluetooth.
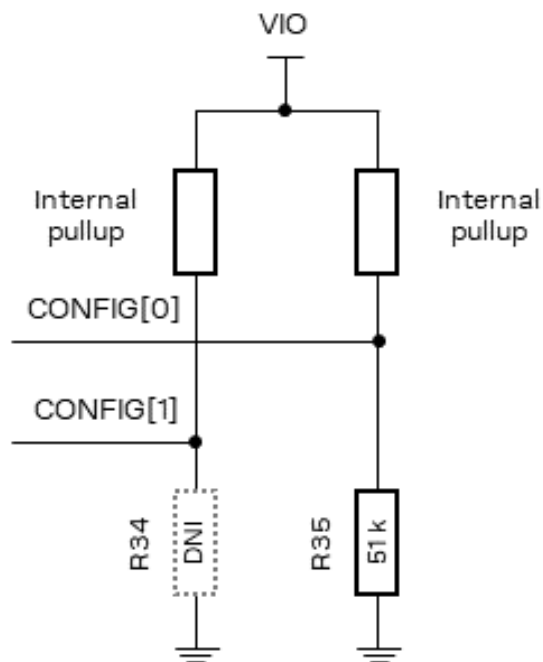
Figure 2: Default configuration of the M2-MAYA-W1 boot pins

Figure 3 shows the physical locations of pulldown resistor positions, R34 and R35.
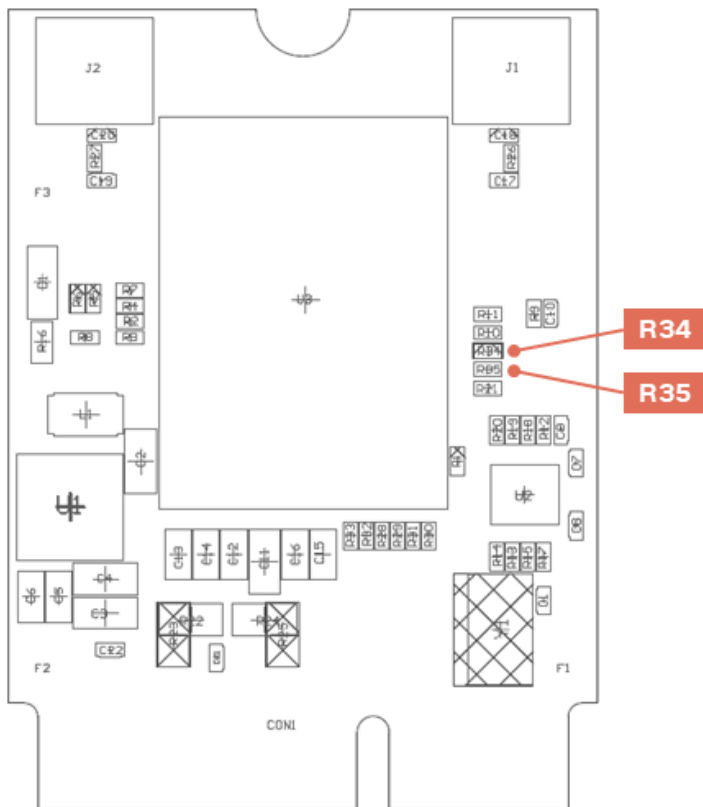
Figure 3: Position of resistors R34 and R35 on M2-MAYA-W1

2.2 SDIO

The SDIO device interface is conformant with the industry standard SDIO 3.0 specification (UHS-I up to 50 MB/s) and allows a host controller to access MAYA-W1 Wi-Fi functionality using the SDIO bus protocol. The interface supports 4-bit SDIO transfer mode over the full clock range up to 100 MHz. All bus speed modes are supplied from the SDIO I/O power supply (by default set to 1.8 V).

2.3 UART

MAYA-W1 series modules support a high-speed UART interface that is conformant with the industry-standard 16550 specification. For information about the features and baud rates supported in the MAYA-W1 series high-speed UART, see the MAYA-W1 data sheet [1].

2.4 PCM/I2S

M2-MAYA-W1 supports the full functionality of the MAYA-W1 series PCM and I2S interfaces for audio. The pins of the PCM and I2S interfaces are shared. See also, the MAYA-W1 data sheet [1].

3 Pin definition

The M2-MAYA-W1 card module implements the standard pinout of M.2 mechanical Type E sockets, as defined by the PCI Express M.2 Specification [5]. In co-operation with NXP, the card fully supports the optional sideband and debug signals defined by the NXP Wi-Fi/Bluetooth M.2 Key E Pinout Definition [6].

3.1 Pin assignment

Figure 4: M2-MAYA-W1 pin assignment

3.2 Pin description

Table 4 and Table 5 describe the M2-MAYA-W1 pins located at the top and bottom side of the M.2 card, respectively. The signal direction of the pins (inputs or outputs) is shown from the M2-MAYA-W1 card perspective.

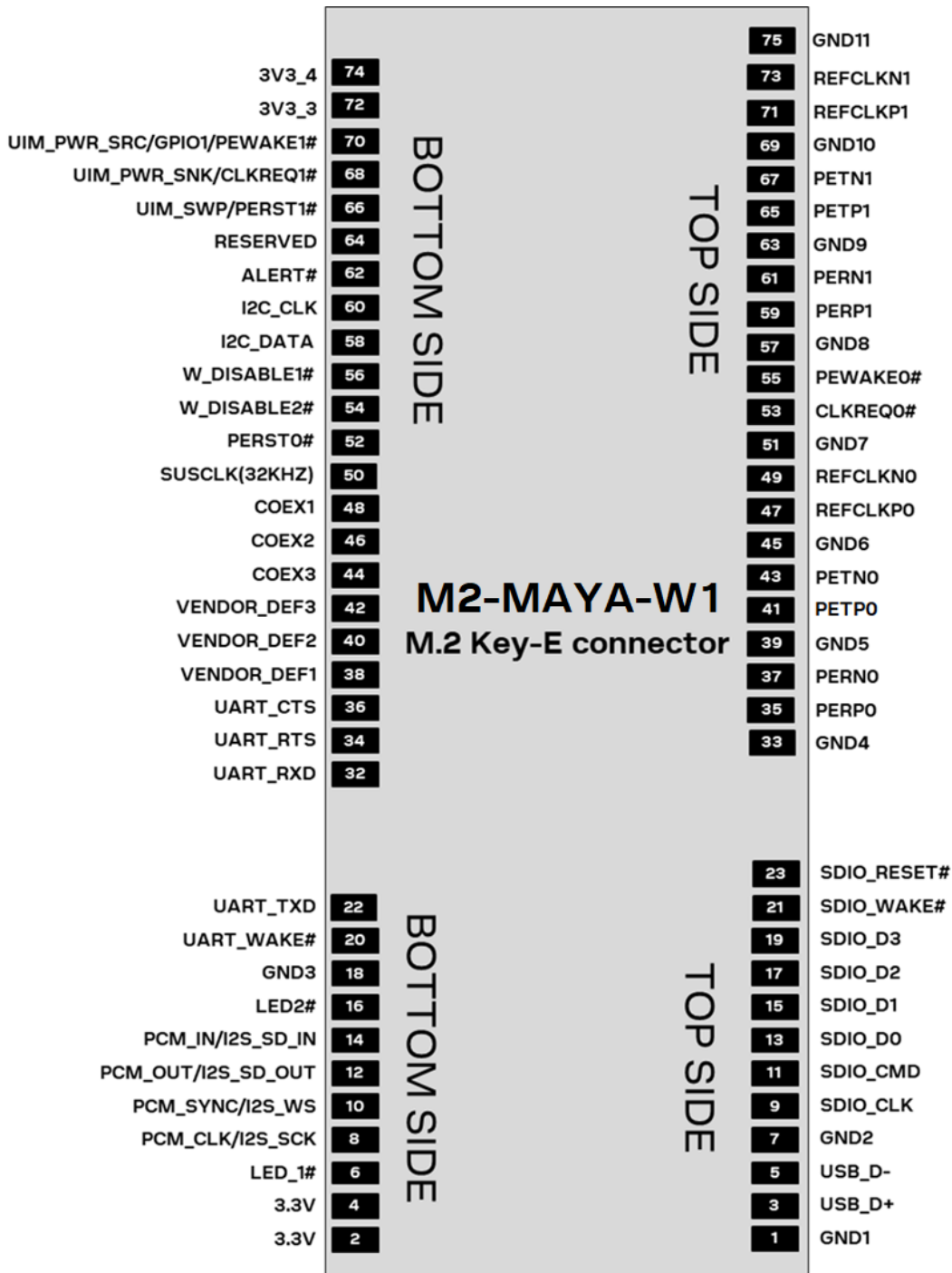| Pin no.	Pin name	Pin type	Voltage	Description
1	GND1	GND		Ground
3	USB_D+	NC		USB data + serial data interface. Not connected
5	USB_D-	NC		USB data - serial data interface. Not connected
7	GND2	GND		Ground
9	SDIO_CLK	I	VIO_SD	SDIO Clock
11	SDIO_CMD	I/O	VIO_SD	SDIO Command
13	SDIO_D0	I/O	VIO_SD	SDIO Data 1
15	SDIO_D1	I/O	VIO_SD	SDIO Data 2
17	SDIO_D2	I/O	VIO_SD	SDIO Data 3
19	SDIO_D3	I/O	VIO_SD	SDIO Data 4
21	SDIO_WAKE#	O	VIO	NXP usage: **WLAN_WAKE_HOST**. Sideband signal used by the Wi-Fi radio to wake up the platform. Active Low by default. Connect to Host GPIO Open drain. Pullup required on platform
23	SDIO_RESET#	NC	VIO	NXP usage: **WLAN_INDEPENDENT_RESET**. Sideband signal to independently reset the Wi-Fi radio. Active Low by default. Connect to Host GPIO
				M.2 Key E connector notch
33	GND4	GND		Ground
35	PERP0	NC		PCIe RX. Not connected
37	PERN0	NC		PCIe RX. Not connected
39	GND5	GND		Ground
41	PETP0	NC		PCIe TX. Not connected
43	PETN0	NC		PCIe TX. Not connected
45	GND6	GND		Ground
47	REFCLKP0	NC		PCIe Reference Clock. Not connected
49	REFCLKN0	NC		PCIe Reference Clock. Not connected
51	GND7	GND		Ground
53	CLKREQ0#	NC		PCIe Clock Request. Not connected
55	PEWAKE0#	NC		PCIe PME Wake. Not connected
57	GND8	GND		Ground
59	PERP1	NC		PCIe RX. Not connected
61	PERN1	NC		PCIe RX. Not connected
63	GND9	GND		Ground
65	PETP1	NC		PCIe TX. Not connected
67	PETN1	NC		PCIe TX. Not connected
69	GND10	GND		Ground

Pin no.	Pin name	Pin type	Voltage	Description
71	REFCLKP1	NC		PCIe Reference Clock. Not connected
73	REFCLKN1	NC		PCIe Reference Clock. Not connected
75	GND11	GND		Ground

Table 4: M2-MAYA-W1 pinout – top side

Table 5 describes the M2-MAYA-W1 pins located on the bottom side of the M.2 card. The signal direction of the pins (inputs or outputs) is shown from the M2-MAYA-W1 card perspective.

Pin no.	Pin name	Pin type	Voltage	Description
2	3.3V	P	3.3 V	Supply voltage pin
4	3.3V	P	3.3 V	Supply voltage pin
6	LED_1#	NC		Not connected
8	PCM_CLK/I2S_SCK	I/O	VIO	PCM data clock
10	PCM_SYNC/I2S_WS	I/O	VIO	PCM frame sync
12	PCM_OUT/I2S_SD_OUT	O	VIO	PCM data output
14	PCM_IN/I2S_SD_IN	I	VIO	PCM data input
16	LED2#	NC		Not connected
18	GND3	GND		Ground
20	UART_WAKE#	O	3.3 V	NXP usage: BT_WAKE_HOST. Sideband signal used by the Bluetooth radio to wake up the platform. Active Low by default. Connect to Host GPIO Open drain. Pullup required on platform. See note [1] for details
22	UART_TXD	O	VIO	UART transmit. Connected to host platform UART receive (UART_RXD)
		M.2 Key E connector notch		
32	UART_RXD	I	VIO	UART receive. Connected to host platform UART transmit (UART_TXD)
34	UART_RTS	O	VIO	UART Request-To-Send. Connected to host platform UART Clear-To-Send (UART_CTS)
36	UART_CTS	I	VIO	UART Clear-To-Send. Connected to host platform UART Request-To-Send (UART_RTS)
38	VENDOR_DEF1	I/O	VIO	NXP usage: **JTAG_TDO**. Used for debug.
40	VENDOR_DEF2	I	VIO	NXP usage: **DEV_WLAN_WAKE**. Sideband signal used by the platform to wake up the Wi-Fi radio. Active Low. Connect to Host GPIO
42	VENDOR_DEF3	I	VIO	NXP usage: **DEV_BT_WAKE**. Sideband signal used by the platform to wake up the Bluetooth radio. Active Low. Connect to Host GPIO
44	COEX3	I/O	VIO	NXP usage: **JTAG_TDI** Used for debug.
46	COEX2	I/O	VIO	NXP usage: **JTAG_TCK**. Used for debug.
48	COEX1	I/O	VIO	NXP usage: **JTAG_TMS**. Used for debug.
50	SUSCLK(32KHZ)	NC		Not connected
52	PERST0#	NC		PCIe host indication to reset the device. Not connected
54	W_DISABLE2#	I	3.3 V	NXP usage: **BT_INDEPENDENT_RESET**. Sideband signal to independently reset the Bluetooth radio. Active Low by default. Connected to Host GPIO. See note [1] for details

Pin no.	Pin name	Pin type	Voltage	Description
56	W_DISABLE1#	I	3.3 V	NXP usage: **PDn**. Full Power-down for the Wi-Fi/BT radio: High = normal mode, Low = full power-down mode. Connect to host GPIO. See note [1] for details
58	I2C_DATA	NC		I2C data. Not connected
60	I2C_CLK	NC		I2C clock. Not connected
62	ALERT#	NC		Not connected
64	RESERVED	NC		Not connected
66	UIM_SWP/PERST1#	NC		Not connected
68	UIM_PWR_SNK/CLKREQ1#	NC		Not connected
70	UIM_PWR_SRC/GPIO1/PEWAKE1#	NC		Not connected
72	3V3_3	P	3.3 V	Supply voltage pin
74	3V3_4	P	3.3 V	Supply voltage pin

[1] It is recommended that a 3V3 CMOS buffer is inserted along each one of the sideband signal lines – between the host platform and the M.2 card socket. Signals **W_DISABLE1#** and **W_DISABLE2#** are outputs from the host platform and inputs to the M.2 card. Therefore, the buffer outputs must be connected to those signals. The **UART_WAKE#** signal is output from the M.2 card and input to the host platform. Therefore, the buffer input must be connected to that signal.

Table 5: M2-MAYA-W1 pin-out (bottom side)

4 Electrical specifications

⚠ Stressing the device above one or more of the ratings of the Absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these ratings or in conditions other than those specified in the Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Units
3V3	Power supply voltage	-0.3	4.0	V
$T_{STORAGE}$	Storage temperature	-40	+85	ºC

Table 6: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification given in Table 6 must be limited to values within the specified boundaries by using appropriate protection devices.

4.2 Maximum ESD ratings

Applicability	Min.	Max.	Units
Human Body Model (HBM), according to ANSA/ESDA/JEDEC JS-001-2014.	-2000	+2000	V
Charged Device Model (CDM), according to JESD22-C101.	-500	+2000	V

Table 7: Maximum ESD ratings

4.3 Operating conditions

Symbol	Parameter	Min.	Typ	Max.	Units
3V3	Power supply voltage	3.135	3.3	3.465	V
T_A	Ambient operating temperature	-40	-	+85	ºC
Ripple Noise	Peak-to-peak voltage ripple on all supply lines.	-	-	30	mV

Table 8: Operating conditions

4.4 Digital pad ratings

Symbol	Parameter	VIO	Min.	Max.	Units
V_{IH}	Input high voltage	1.8 V or 3.3 V	0.7*VIO	VIO+0.4	V
V_{IL}	Input low voltage	1.8 V or 3.3 V	-0.4	0.3*VIO	V
V_{HYS}	Input hysteresis	1.8 V or 3.3 V	100	-	mV
V_{OH}	Output high voltage	1.8 V or 3.3V	VIO-0.4	-	V
V_{OH}	Output low voltage	1.8 V or 3.3 V	-	0.4	V

Table 9: DC characteristics VIO

4.5   Power consumption

Peak current condition	Temperature	Supply current	Units
Active transmission at max. rated output power (WiFi)	Room temperature	0.400	A
Active transmission at max. rated output power (Bluetooth)	Room temperature	0.120	A
Firmware initialization	Room temperature	0.145	A

Table 19: Peak current consumption

4.6   Radio specification

4.6.1   Bluetooth

Parameter	Specification
RF Frequency Range	2.402 – 2.480 GHz
Supported Modes	Bluetooth 5.2 Bluetooth Low Energy (LE) • LE long range • Shared RF with BR/EDR • 2 Mbps LE
Modulation	1 Mbit/s: GFSK (BR) 2 Mbit/s: π/4 DQPSK (EDR) 3 Mbit/s: 8DQPSK (EDR)
Transmit Power	Class 1 BR: +8 dBm ± 2 dB
	Class 1 EDR: +7 dBm ± 2 dB
	Bluetooth LE: +7 dBm ± 2 dB
Receiver sensitivity (typical values)	Bluetooth BR: -94 dBm ± 1.5 dB
	Bluetooth EDR: -88 dBm ± 1.5 dB
	Bluetooth LE: -95 dBm ± 1.5 dB Bluetooth LE Coded PHY: -100 dBm ± 1.5 dB

Table 10: Bluetooth radio parameters

4.6.2   Wi-Fi

M2-MAYA-W1 modules support dual-band Wi-Fi with 802.11a/b/g/n operation in the 2.4 GHz and 5 GHz radio bands. The module is designed to operate in only one frequency band at a time.

Parameter	Operating mode	Specification
RF Frequency range	802.11b/g/n	2.400 – 2.500 GHz
	802.11a/n	4.900 – 5.825 GHz
Modulation	802.11b	CCK and DSSS
	802.11a/g/n	OFDM
Supported data rates	802.11b	1, 2, 5.5, 11 Mbps
	802.11a/g	6, 9, 12, 18, 24, 36, 48, 54 Mbps
	802.11n SISO	MCS0 – MCS7 (150 Mbps)
Supported channel bandwidth	802.11n	20, 40 MHz
Supported guard interval (GI)	802.11n	400, 800 ns

Table 11: Wi-Fi radio parameters

Parameter		Operating mode	802.11 EVM limit	Specification (typ. output power tolerance ± 2 dB)
Maximum transmit power	2.4 GHz	DSSS/CCK	-9 dB	18 dBm
		OFDM, BPSK	-8 dB	18 dBm
		OFDM, QPSK	-13 dB	18 dBm
		OFDM, 16-QAM	-19 dB	18 dBm
		OFDM, 64-QAM, 3/4	-25 dB	16 dBm
		OFDM, 64-QAM, 5/6	-27 dB	16 dBm
	5 GHz	OFDM, BPSK	-5 dB	18 dBm
		OFDM, QPSK	-13 dB	18 dBm
		OFDM, 16-QAM	-19 dB	18 dBm
		OFDM, 64-QAM, 3/4	-25 dB	16 dBm
		OFDM, 64-QAM, 5/6	-27 dB	16 dBm

Table 12: Wi-Fi radio maximum transmit power parameters

Band	Operating mode	Data rate	Bandwidth	Specification
2.4 GHz	802.11b	1 Mbps / 2 Mbps	20 MHz	-98 dBm / -94 dBm
		5.5 Mbps / 11 Mbps		-94 dBm / -90 dBm
	802.11g	6 Mbps / 9 Mbps	20 MHz	-91 dBm / -91 dBm
		12 Mbps / 18 Mbps		-91 dBm / -89 dBm
		24 Mbps / 36 Mbps		-86 dBm / -82 dBm
		48 Mbps / 54 Mbps		-78 dBm / -77 dBm
	802.11n	MCS0 / MCS1	20 MHz	-91 dBm / -90 dBm
		MCS2 / MCS3		-87 dBm / -84 dBm
		MCS4 / MCS5		-81 dBm / -76 dBm
		MCS6 / MCS7		-75 dBm / -73 dBm
		MCS0 / MCS1	40 MHz	-87 dBm / -87 dBm
		MCS2 / MCS3		-84 dBm / -82 dBm
		MCS4 / MCS5		-77 dBm / -74 dBm
		MCS6 / MCS7		-72 dBm / -71 dBm
5 GHz	802.11a	6Mbps/9Mbps	20 MHz	-90 dBm / -90 dBm

| Band	Operating mode	Data rate	Bandwidth	Specification
		12 Mbps/18 Mbps		-89 dBm / -87 dBm
		24 Mbps/36 Mbps		-84 dBm / -80 dBm
		48 Mbps/54 Mbps		-76 dBm / -75 dBm
	802.11n	MCS0 / MCS1	20 MHz	-90 dBm / -87 dBm
		MCS2 / MCS3		-85 dBm / -82 dBm
		MCS4 / MCS5		-79 dBm / -75 dBm
		MCS6 / MCS7		-72 dBm / -70 dBm
		MCS0 / MCS1	40 MHz	-86 dBm / -85 dBm
		MCS2 / MCS3		-82 dBm / -79 dBm
		MCS4 / MCS5		-76 dBm / -72 dBm
		MCS6 / MCS7		-70 dBm / -69 dBm

Table 13: Wi-Fi receiver characteristics

5 Antenna connectors

The M2-MAYA-W161 card features two U.FL connectors: one for each of the two antenna pins.

- Connector J1 is connected to MAYA-W161 pin K1 (**RF_ANT0**) for Wi-Fi operation.
- Connector J2 is connected to MAYA-W161 pin K9 (**RF_ANT1**) for Bluetooth.

The location of the U.FL connectors on the M.2 card is shown in Figure 5.
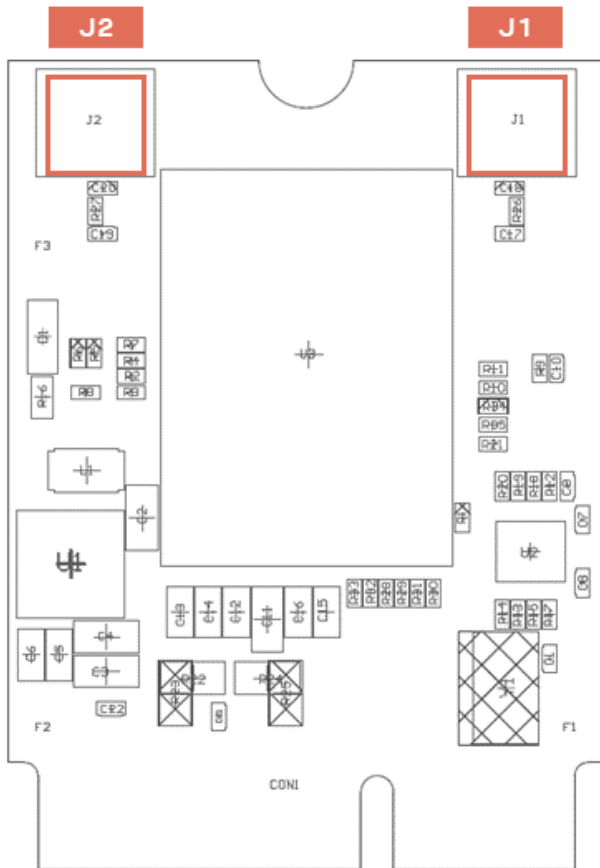
Figure 5: Location of M2-MAYA-W161 antenna U.FL connectors

☞ Given the small size and low profile of the U.FL connector, be sure to follow the manufacturer's instructions to avoid any damage when mating and un-mating the connector. See also the U.FL series guideline [7] and U.FL series data sheet [8].

6   Voltages

The M2-MAYA-W1 card requires a 3.3 V power supply. The card takes the 3.3 V supply from the **3V3** pins on the M.2 connector, while the 1.8 V supply is generated by the on-card DC-DC converter.

The default setting for **VIO** is 1.8 V but this can be changed to 3.3 V by moving the 0 Ω resistor in position R22 to R23 (default = DNI), as shown in Figure 6 (a). Note that R22 and R23 share a common pad. Only one of the two resistors R22 and should be present at any time.

The default setting for **VIO_SD** is 1.8 V, but this can be changed to 3.3 V by moving the 0 Ω resistor in position R24 to R25 (default = DNI), as shown in Figure 6 (b). Note that R24 and R25 share a common pad. Only one of the two resistors R24 and R25 should be present at any time.
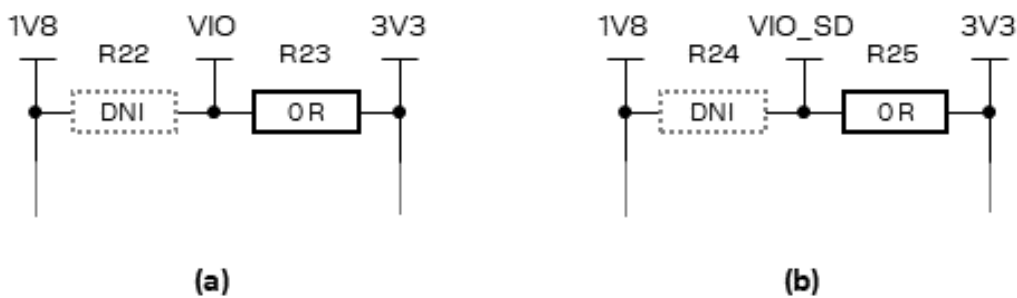

Figure 6: Placement of 0 Ω resistor to change (a) VIO from 1V8 V to 3V3, (b) VIO_SD from 1V8 to 3V3

Figure 7 shows the resistor positions used for changing the voltage supply levels for **VIO** and **VIO_SD.**
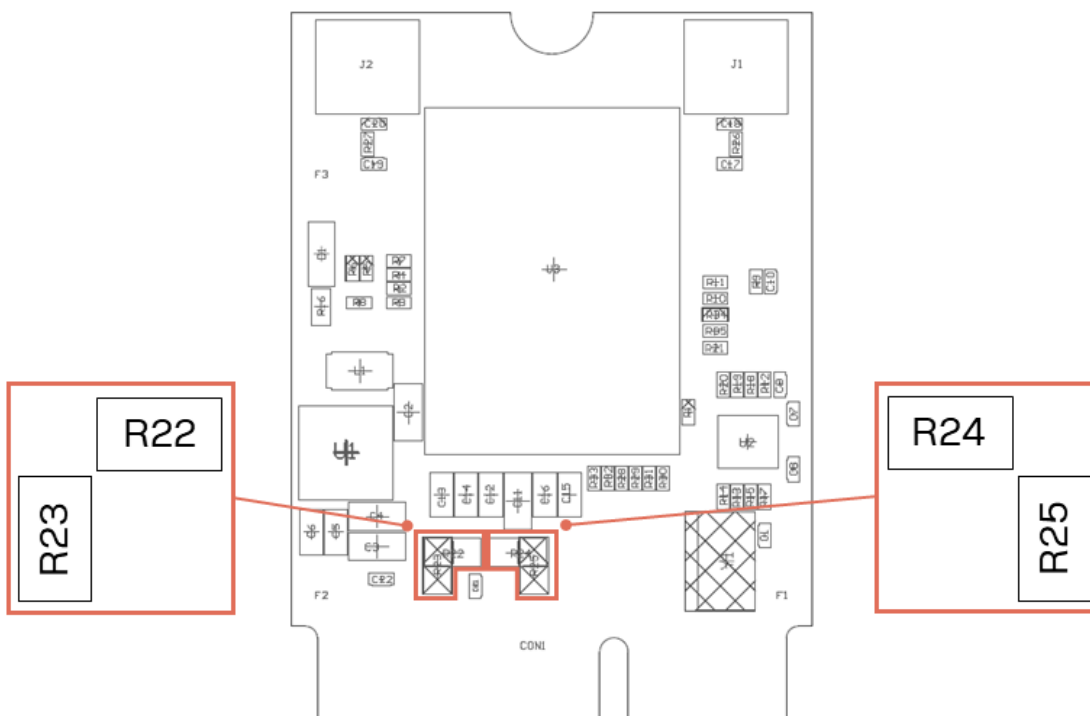

Figure 7: R22 and R23 positions for selecting VIO, and R24 and R25 positions for selecting VIO_SD

Figure 8 shows the on-card level-shifter that translates the M.2 signals, **UART_WAKE#** and **W_DISABLE1#,** from 3.3 V to VIO.
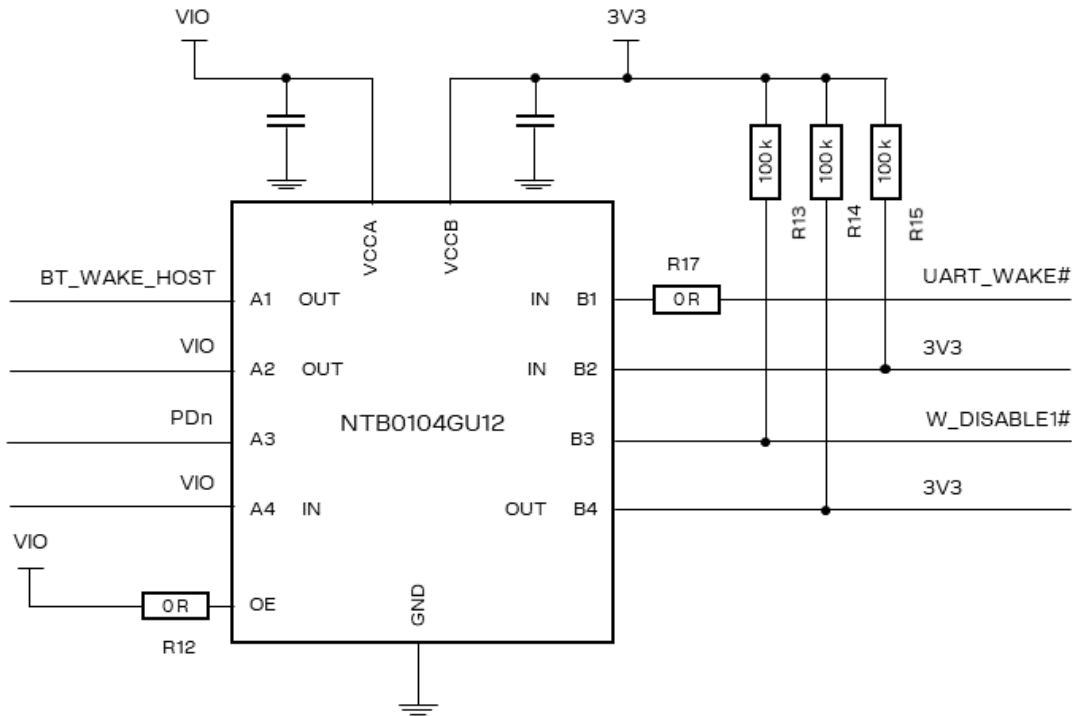

Figure 8: VIO-to-3.3 V level shifter

Figure 9 shows the position of the level-shifter (U5) on the card.
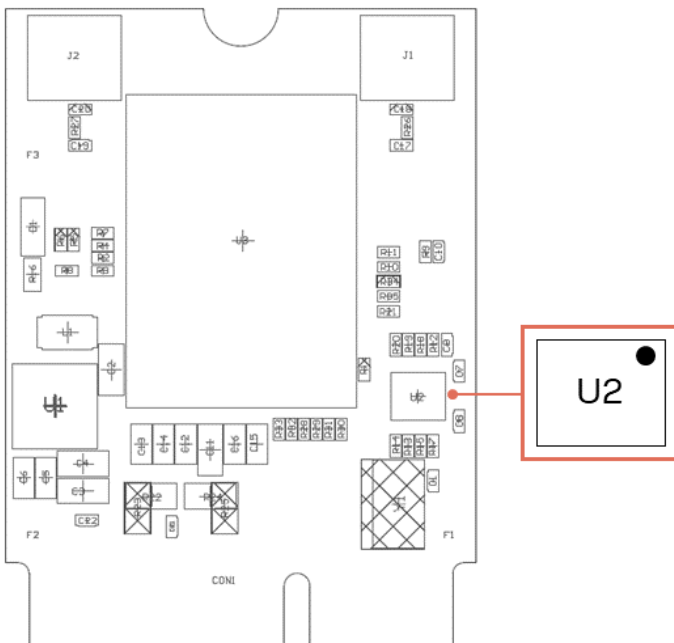

Figure 9: Position of VIO-to-3.3 V level shifter on M2-MAYA-W1

7   Test points

On-card test points TP1, TP2, TP3 and TP4 allow NXP sideband signals to be probed, as shown in Table 14. For information that describes how these signals are used in NXP platforms, see the Pin description. See also the NXP M.2 Key E Pinout Definition [6].

Test point #	M.2 pin#	NXP usage
TP1	44	JTAG_TDI
TP2	38	JTAG_TDO
TP3	48	JTAG_TMS
TP4	46	JTAG_TCK

Table 14: M.2 pin number and functionality of the M2-MAYA-W2 cards test points
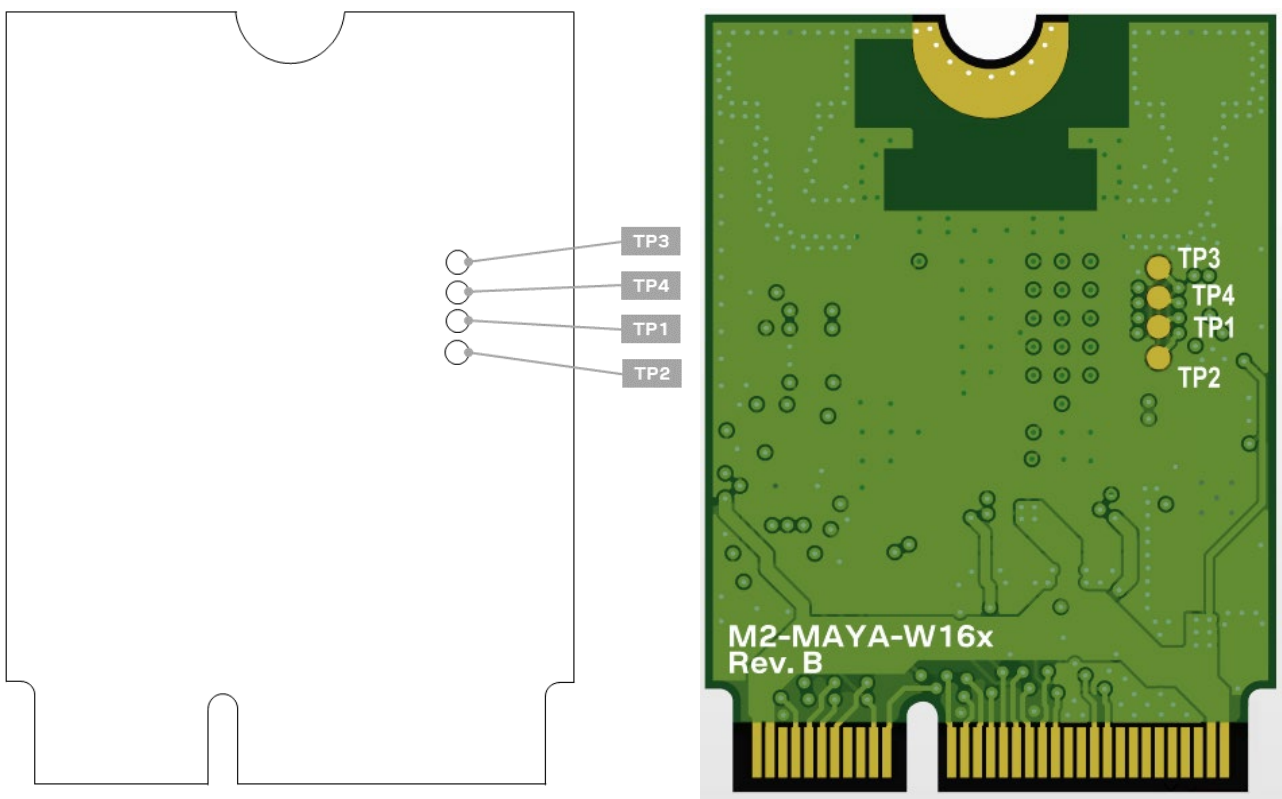
Figure 10: Position of test points on the bottom side of the M2-MAYA-W161 card

8   Mechanical specification

8.1   Physical dimensions

Figure 11 shows the critical physical dimensions of the card.
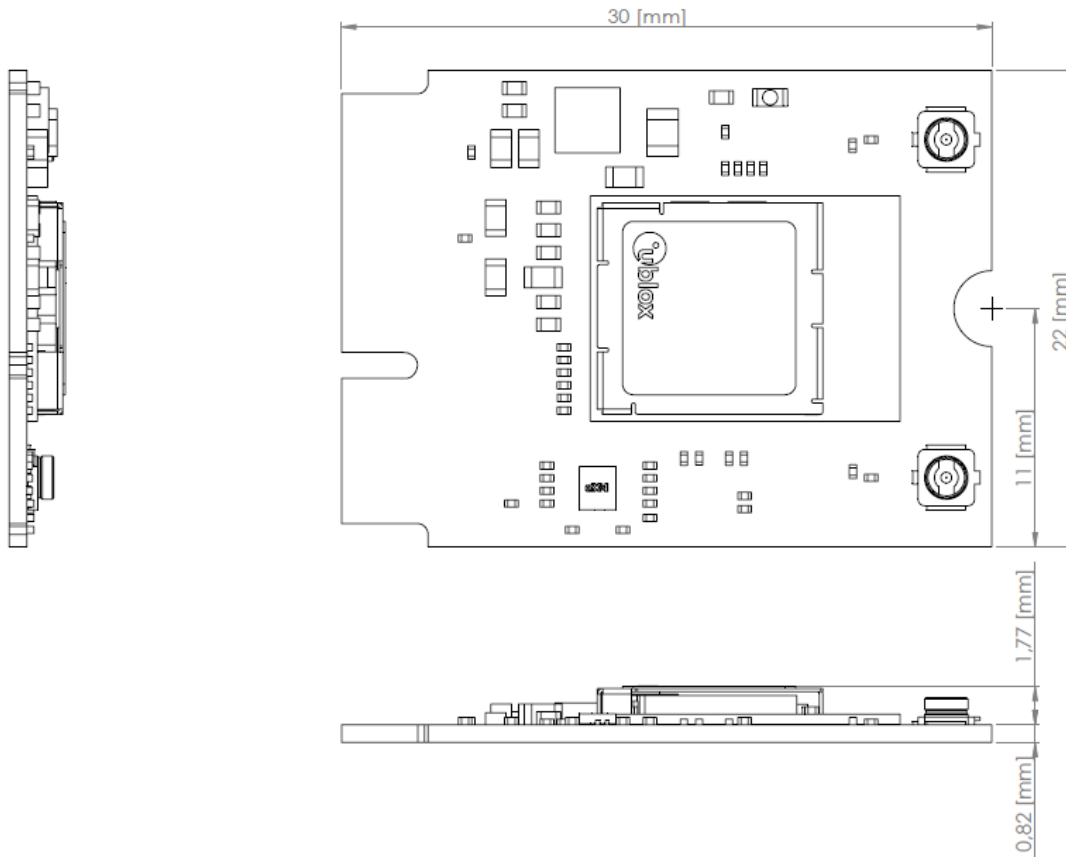

Figure 11: Physical dimensions of the M2-MAYA-W1 card

9   Software

M2-MAYA-W1 cards are based on the NXP IW416 chipset and the drivers and firmware required to operate MAYA-W1 series modules are also developed by NXP. A firmware binary is downloaded by the host operating system driver at start-up.

The following software options are available for the card:

- Open-source Linux/Android driver (`mxm_mwifiex`) for mainstream use is available free of charge and already integrated into the Linux BSP for NXP i.MX application processors
- MCUXpresso Wi-Fi/Bluetooth support for supported NXP MCUs

The software packages typically include:

- Dedicated kernel driver that binds the Wi-Fi device to the kernel. Driver sources are provided.
- Dedicated Wi-Fi/Bluetooth firmware image that is uploaded during initialization of the device.
- Laboratory and manufacturing tools.

10 Approvals

M2-MAYA-W1 cards are designed to comply with the regulatory demands of the Federal Communications Commission (FCC), Industry Canada (IC), UK standards for Conformity Assessed (UKCA) marking, and European standards for CE marking.

For detailed information about regulatory compliance requirements of end products that use M2-MAYA-W1 modules, see the MAYA-W1 system integration manual [2].

10.1 Configuration of Wi-Fi transmit power limits

The Wi-Fi TX power table defines the transmit power levels for the Wi-Fi radio. The power levels are based on regulatory compliance, IEEE 802.11 requirements, and product design constraints. The TX power table can be adjusted to achieve the highest transmit power level for each Wi-Fi channel, bandwidth, and modulation within the constraints defined by the certification.

⚠ The correct TX power limits must be applied to the module after startup of the host system and adjusted after some change of the regulatory domain or country specific requirements during runtime.

The Wi-Fi TX power levels are configured with the `txpwrlimit_2g_cfg_set` and `txpwrlimit_5g_cfg_set` data structures defined in the `txpwrlimit_cfg.conf` configuration file. The configuration file allows integrators to fine tune specific transmit power levels for the Wi-Fi radio, including:

- Band (2.4, 5 GHz)
- Channel
- Modulation rate (CCK, OFDM, HT20, HT40)
- Channel bandwidth (20, 40 MHz)

☞ Transmit power limit configuration files are provided by u-blox for the certified regulatory domains accommodated in the available reference designs and Pre-approved antennas. The configuration files for completed certifications are included in the Yocto meta layer.

For the exact power limits used for the various certifications, see the Appendix: Wi-Fi Tx output power limits. The MAYA-W1 system integration manual [2] contains details about configuring Wi-Fi Tx output power limits along with examples.

11 Product handling

11.1 Packaging

Packaged and shipped in trays containing multiple M.2 cards.

11.2 Shipment, storage, and handling

☞ For more information regarding shipment, storage and handling see the u-blox package information guide. [3]

11.2.1 ESD handling precautions

⚠ M2-MAYA-W1 cards are Electrostatic Sensitive Devices (ESD) that demand the observance of special handling precautions against electrostatic damage. Failure to observe the precautions can result in severe damage to the card.

M2-MAYA-W1 cards are manufactured through a highly automated process, which complies with IEC61340-5-1 (STM5.2-1999 Class M1 devices) standard. In compliance with the following European regulations, proper measures must be taken to protect M2-MAYA-W1 from ESD events on any pin that might be exposed to the end user:

- ESD testing standard CENELEC EN 61000-4-2
- Radio equipment standard ETSI EN 301 489-1

The minimum requirements that must be met to satisfy European regulations are described in Table 15.

Application	Category	Immunity level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration of the end product.	Contact discharge	4 kV
	Air discharge	8 kV

Table 15: ESD immunity ratings based on EN 61000-4-2

Compliance with standard protection level specified in EN 61000-4-2 is achieved by including proper ESD protection in the production line and close to all areas that are accessible to the end user.

12 Labeling and ordering

The labels applied to M2-MAYA-W1 cards include important product information. Table 16 describes each of the features on the product label for each product variant.

Reference	Description
1	Text in bold font: "Model:" type number with the product version
2	DataMatrix (product identifier, serial number, datacode) • Product identifier: 3 digits defined by EMS • Serial number Datacode: 4 digits
3	Company logo and trademark
4	Placeholder for CE marking (when certified)
5	Panel position number
6	Production date YY/WW (year/week)

Table 16. M2-MAYA-W1 card label description

12.1 M2-MAYA-W161 cards

Figure 12 shows the label applied to M2-MAYA-W161 cards. Each of the given label references are described in Table 16.
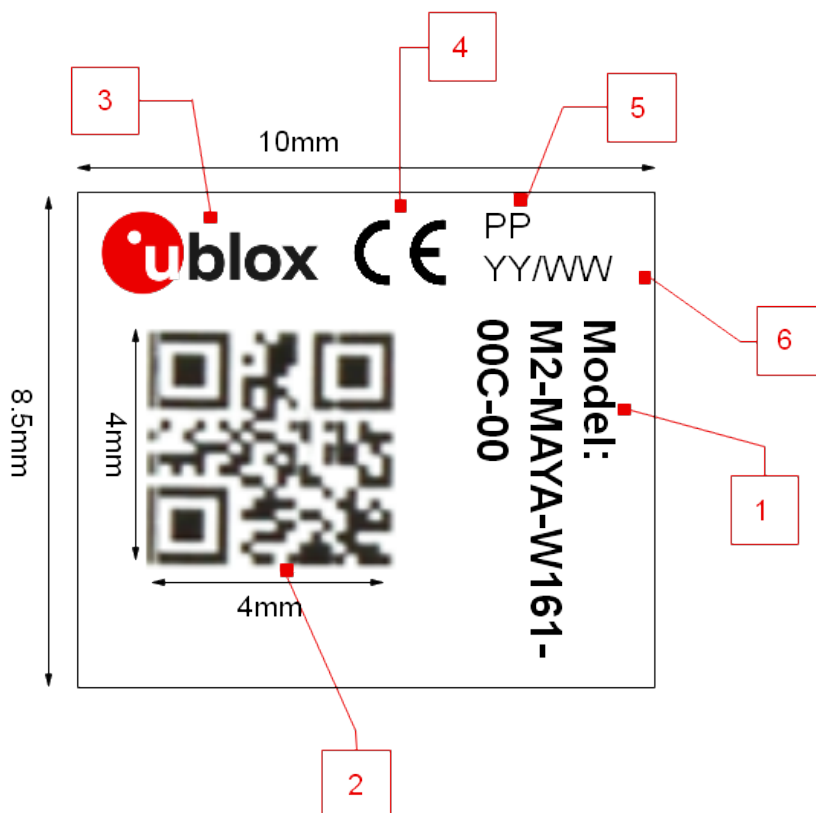
Figure 12: Product label format with dimensions for M2-MAYA-W161

12.2 Ordering codes

Ordering Code	Product name	Product
M2-MAYA-W161-00C	M2-MAYA-W161	M.2 key E card (2230) with two antenna U.FL connectors (one for 2.4 GHz and 5 GHz 802.11a/b/g/n and another for Bluetooth/Bluetooth Low Energy (LE) 5.2). Operational temperature -40 ^{0}C to +85 ^{0}C, standard grade module with NXP chipset IW416. Packaged in tray containing multiple M.2 cards.

Table 17: Product ordering codes

☞ Product changes affecting form, fit or function are documented by u-blox. Visit our website for a list of Product Change Notifications (PCNs).

Appendix

A   Appendix A: Wi-Fi Tx output power limits

A.1. FCC/ISED regulatory domain

A.1.1. Bluetooth Output power

Channel	Channel bandwidth	Data rates	Maximum power setting
0 - 78	1 MHz	BR/EDR	7 dBm
0 - 39	2 MHz	BLE	8 dBm

A.1.2. Wi-Fi Output power for 2.4 GHz band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
1 - 2	CCK and DSSS	20 MHz	1, 2, 5.5, 11 Mbps	14 dBm
3	CCK and DSSS	20 MHz	1, 2, 5.5, 11 Mbps	15 dBm
4	CCK and DSSS	20 MHz	1, 2, 5.5, 11 Mbps	16 dBm
5	CCK and DSSS	20 MHz	1, 2, 5.5, 11 Mbps	17 dBm
6 - 11	CCK and DSSS	20 MHz	1, 2, 5.5, 11 Mbps	18 dBm
1	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	16 dBm
2 – 9	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	18 dBm
10	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	17 dBm
11	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	16 dBm
1	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
2 - 10	OFDM	20 MHz	HT20 MCS0-MCS7	16 dBm
11	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
3, 4	OFDM	40 MHz	HT40 MCS0-MCS7	14 dBm
5	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm
6	OFDM	40 MHz	HT40 MCS0-MCS7	16 dBm
7 - 9	OFDM	40 MHz	HT40 MCS0-MCS7	15 dBm

Table 18: FCC Wi-Fi power table for operation in the 2.4 GHz band

A.1.3. Wi-Fi output power for 5 GHz band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
36 - 60	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	17 dBm
64	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	16 dBm
36 - 60	OFDM	20 MHz	HT20 MCS0-MCS7	16 dBm
64	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
38	OFDM	40 MHz	HT40 MCS0-MCS7	14 dBm
46, 54	OFDM	40 MHz	HT40 MCS0-MCS7	16 dBm
62	OFDM	40 MHz	HT40 MCS0-MCS7	14 dBm

Table 19: FCC Wi-Fi power table for operation in the 5 GHz U-NII-1 and U-NII-2A bands

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
100	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	16 dBm
104 - 132	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	18 dBm
136	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	16 dBm
140	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	14 dBm
100	OFDM	20 MHz	HT20 MCS0-MCS7	15 dBm
104 - 136	OFDM	20 MHz	HT20 MCS0-MCS7	16 dBm
140	OFDM	20 MHz	HT20 MCS0-MCS7	14 dBm
102	OFDM	40 MHz	HT40 MCS0-MCS7	13 dBm
110	OFDM	40 MHz	HT40 MCS0-MCS7	16 dBm
134	OFDM	40 MHz	HT40 MCS0-MCS7	13 dBm

Table 20: FCC Wi-Fi power table for operation in the 5 GHz U-NII-2e band

Channel	Modulation	Channel bandwidth	Data rates	Maximum power setting
149 - 153	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	16 dBm
157	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	17 dBm
161 - 165	OFDM	20 MHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	18 dBm
149 - 165	OFDM	20 MHz	HT20 MCS0-MCS7	16 dBm
151 - 159	OFDM	40 MHz	HT40 MCS0-MCS7	16 dBm

Table 21: FCC Wi-Fi power table for operation in the 5 GHz U-NII-3 band

Appendix B: Glossary

Abbreviation	Definition
BLE	Bluetooth Low Energy
BR/EDR	Bluetooth Basic Rate / Enhanced Data Rate
BSP	Board Support Package
BT	Bluetooth
DNI	Do Not Insert
I2S	Inter-IC-Sound
IC	Integrated Circuit
PCM	Pulse Code Modulation
SDIO	Secure Digital Input Output
TBD	To be defined / determined
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VIO	Input /Output Voltage
U.FL	Low-profile SMT coaxial connector

Table 22: Explanation of the abbreviations and terms used

Related documentation

[1]   MAYA-W1 series data sheet, UBX-21006380
[2]   MAYA-W1 series system integration manual, UBX-21010495
[3]   Product packaging reference guide, UBX-14001652
[4]   NXP IW416 preliminary data sheet, Rev. 3, 16 February 16, 2021
[5]   PCI Express M.2 Specification Revision 4.0, Version 1.0, November 5, 2020
[6]   Wi-Fi/Bluetooth M.2 Key E Pinout Definition – NXP Application Note AN13049, Rev.1,
      November 12, 2020
[7]   Hirose Electric Co. LTD - U.FL Series Catalog, August 2021
[8]   Hirose Electric Co. LTD - U.FL Series Specification Sheet, June 19, 2020
[9]   u-blox Limited Use License Agreement (LULA-M)

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	04-Mar-2022	gmet	Initial release
R02	03-Jan-2023	gmet	Revised content; added Appendix A and Electrical Specifications chapter
R03	08-Feb-2023	gmet	Revised and updated Interfaces, Electrical specifications, Approvals, and Wi-Fi TX output power limits.
R04	20-Apr-2023	gmet	Updated product status. Revised absolute maximum ratings and operating conditions for 3V3 supply in Electrical specifications.
R05	23-Feb-2024	gmet	Updated Approvals Voltages, Pin Description, and Test points

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AIW-166K4 AIW-355 DQ-N01 AIW-355 DQ-C01 EWM-W159M201E EWM-W192K1 EWM-W192K2 W106C