Dual Bidirectional I²C-Bus and SMBus Voltage-Level Translator

UM3212M8 ***MSOP8***
UM3212DA ***DFN8 2.1×1.6***
UM3212V8 VSSOP8

General Description

The UM3212 is a dual bidirectional I²C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0V to 3.6V ($V_{ref(1)}$) and 1.8V to 5.5V($V_{bias(ref)(2)}$).
The UM3212 allows bidirectional voltage translations between 1.0V and 5V without the use of a direction pin. The low ON-state resistance (R_{on}) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.
The UM3212 is not a bus buffer which provides both level translation and physically isolates the capacitance to either side of the bus when both sides are connected. The UM3212 only isolates both sides when the device is disabled and provides voltage level translation when active.
The UM3212 can also be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.
As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The UM3212 has a standard open-collector configuration of the I²C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast-mode Plus I²C-bus devices in addition to SMBus devices. The maximum frequency is dependent on the RC time constant, but generally supports > 2MHz.
When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage ($V_{pu(D)}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.
All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical.
The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

Applications

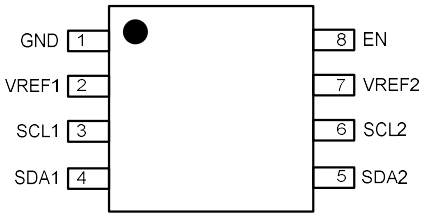
- I²C, SMBus and SPI Level Translation
- Low-Voltage ASIC Level Translation
- Smart Card Readers
- Cell-Phone Cradles
- Portable POS Systems
- Portable Communication Devices
- Low-Cost Serial Interfaces
- Cell-Phones
- GPS
- Telecommunications Equipment

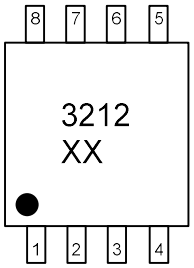
Features

- 2-Bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I^2C-Bus Applications
- Standard-Mode, Fast-Mode, Fast-Mode Plus and HS-Mode I^2C-Bus and SMBus Compatible
- Less than 3.5ns Maximum Propagation Delay to Accommodate Standard-Mode and Fast-Mode I^2C-Bus Devices and Multiple Masters
- Allows Voltage Level Translation between:
  1) 1.0V VREF1 and 1.8V, 2.5V, 3.3V or 5V VREF2
  2) 1.2V VREF1 and 1.8V, 2.5V, 3.3V or 5V VREF2
  3) 1.8V VREF1 and 3.3V or 5V VREF2
  4) 2.5V VREF1 and 5V VREF2
  5) 3.3V VREF1 and 5V VREF2
- Open-Drain I^2C-Bus I/O Ports (SCL1, SDA1, SCL2 and SDA2)
- Provides Bidirectional Voltage Translation with no Direction Pin
- Low 3.0Ω ON-State Connection between Input and Output Ports Provides Less Signal Distortion
- 5V Tolerant I^2C-Bus I/O Ports to Support Mixed-Mode Signal Operation
- High-Impedance SCL1, SDA1, SCL2 and SDA2 Pins for EN=LOW
- Lock-up Free Operation
- Flow through Pinout for Ease of Printed-Circuit Board Trace Routing
- ESD Protection Exceeds 2000V HBM per JESD22-A114, 200V MM per JESD22-A115, and 1000V CDM per JESD22-C101
- Packages Offered: MSOP8, DFN8, VSSOP8

Pin Configurations

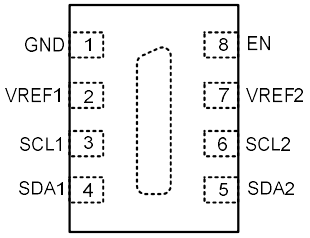
Top View

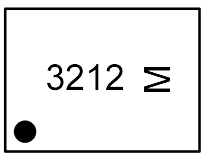




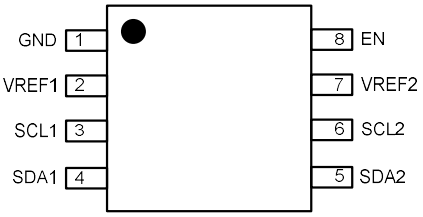
XX: Week Code
UM3212M8
MSOP8

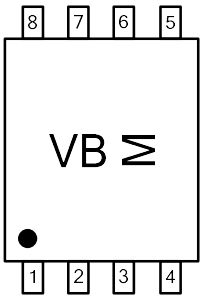
(Top View)





M: Month Code
UM3212DA
DFN8 2.1×1.6





M: Month Code
UM3212V8
VSSOP8

Pin Description

Pin Number	Symbol	Function
1	GND	Ground (0V).
2	VREF1	Low-voltage side reference supply voltage for SCL1 and SDA1.
3	SCL1	Serial clock, low-voltage side; connect to VREF1 through a pull-up resistor.
4	SDA1	Serial data, low-voltage side; connect to VREF1 through a pull-up resistor.
5	SDA2	Serial data, high-voltage side; connect to VREF2 through a pull-up resistor.
6	SCL2	Serial clock, high-voltage side; connect to VREF2 through a pull-up resistor.
7	VREF2	High-voltage side reference supply voltage for SCL2 and SDA2.
8	EN	Switch enable input; connect to VREF2 and pull-up through a high resistor.

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM3212M8	MSOP8	3212	4000pcs/13Inch Tape & Reel
UM3212DA	DFN8 2.1×1.6	3212	3000pcs/7Inch Tape & Reel
UM3212V8	VSSOP8	VB	3000pcs/7Inch Tape & Reel

Absolute Maximum Ratings (Note 1)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Value	Unit
$V_{ref(1)}$	Reference Voltage (1)		-0.5 to +6	V
$V_{bias(ref)(2)}$	Reference Bias Voltage (2)		-0.5 to +6	V
V_I	Input Voltage		-0.5 (Note 2) to +6	V
$V_{I/O}$	Voltage on an Input/Output Pin		-0.5 (Note 2) to +6	V
I_{ch}	Channel Current (DC)		+128	mA
I_{IK}	Input Clamp Current	V_I＜0V	-50	mA
T_{stg}	Storage Temperature Range		-65 to +150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I/O}$	Voltage on an Input/ Output Pin	SCL1, SDA1, SCL2, SDA2	0	5	V
$V_{ref(1)}$ (Note 3)	Reference Voltage (1)	VREF1	0	5	V
$V_{bias(ref)(2)}$ (Note 3)	Reference Bias Voltage (2)	VREF2	0	5	V
$V_{I(EN)}$	Input Voltage on Pin EN		0	5	V
$I_{sw(pass)}$	Pass Switch Current			64	mA
T_{amb}	Ambient Temperature	Operating in Free-Air	-40	+85	°C

Note 3：$V_{ref(1)} \leq V_{bias(ref)(2)} - 1$ V for best results in level shifting applications.

Electrical Characteristics

T_{amb}=−40°C to +85°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Unit
V_{IK}	Input Clamping Voltage	I_I=−18mA; $V_{I(EN)}$=0V				-1.2	V
I_{IH}	HIGH-Level Input Current	V_I=5V; $V_{I(EN)}$=0V				5	μA
$C_{i(EN)}$	Input Capacitance on Pin EN	V_I=0V or 3V			13		pF
$C_{io(off)}$	Off-State Input/Output Capacitance	SCLn, SDAn; V_O=0V or 3V; $V_{I(EN)}$=0V			10	12.2	pF
$C_{io(on)}$	On-State Input/Output Capacitance	SCLn, SDAn; V_O=0V or 3V; $V_{I(EN)}$=3V			8	12	pF
R_{on}	ON-State Resistance (Note 5)	SCLn, SDAn; (Note 6) V_I=0; I_O=64mA	EN=4.5V		2.0	5.0	Ω
			EN=3V		2.4	6.0	
			EN=2.3V		3.1	8.0	
			EN=1.5V		11	32	
		SCLn, SDAn; V_I=2.4V; I_O=15mA	EN=4.5V		4.6	7.5	
			EN=3V		50	80	
		SCLn, SDAn; V_I=1.7V; I_O=15mA	EN=2.3V		50	80	

Note 4：All typical values are at T_{amb}=25°C.

Note 5：Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch.
ON-state resistance is determined by the lowest voltage of the two terminals.

Note 6：Guaranteed by design.

Switching Characteristics (Translating Down)

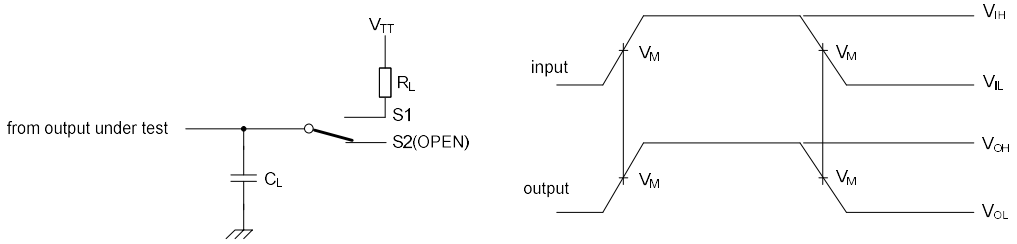
Over recommended operating free-air temperature range (unless otherwise noted). Values guaranteed by design.

Symbol	Parameter	Test Conditions	C_L=50pF		C_L=30pF		C_L=15pF		Unit
			Min	Max	Min	Max	Min	Max	
$V_{I(EN)}$=3.3V; V_{IH}=3.3V; V_{IL}=0V; V_M=1.15V (see Figure 1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL2 or SDA2 to (Output) SCL1 or SDA1.	0	2.5	0	1.7	0	1.2	ns
t_{PHL}	HIGH to LOW Propagation Delay		0	2.5	0	2.0	0	1.3	ns
$V_{I(EN)}$=2.5V; V_{IH}=2.5V; V_{IL}=0V; V_M=0.75V (see Figure 1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL2 or SDA2 to (Output) SCL1 or SDA1.	0	2.5	0	1.7	0	1.2	ns
t_{PHL}	HIGH to LOW Propagation Delay		0	3.0	0	2.0	0	1.3	ns

Switching Characteristics (Translating Up)

Over recommended operating free-air temperature range (unless otherwise noted). Values guaranteed by design.

Symbol	Parameter	Test Conditions	C_L=50pF		C_L=30pF		C_L=15pF		Unit
			Min	Max	Min	Max	Min	Max	
$V_{I(EN)}$=3.3V; V_{IH}=2.3V; V_{IL}=0V; V_{TT}=3.3V; V_M=1.15V; R_L=300Ω (see Figure 1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL1 or SDA1 to (Output) SCL2 or SDA2.	0	2.35	0	1.5	0	1.0	ns
t_{PHL}	HIGH to LOW Propagation Delay		0	3.35	0	2.25	0	1.4	ns
$V_{I(EN)}$=2.5V; V_{IH}=1.5V; V_{IL}=0V; V_{TT}=2.5V; V_M=0.75V; R_L=300Ω (see Figure 1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL1 or SDA1 to (Output) SCL2 or SDA2.	0	2.35	0	1.5	0	1.0	ns
t_{PHL}	HIGH to LOW Propagation Delay		0	3.5	0	2.5	0	1.5	ns

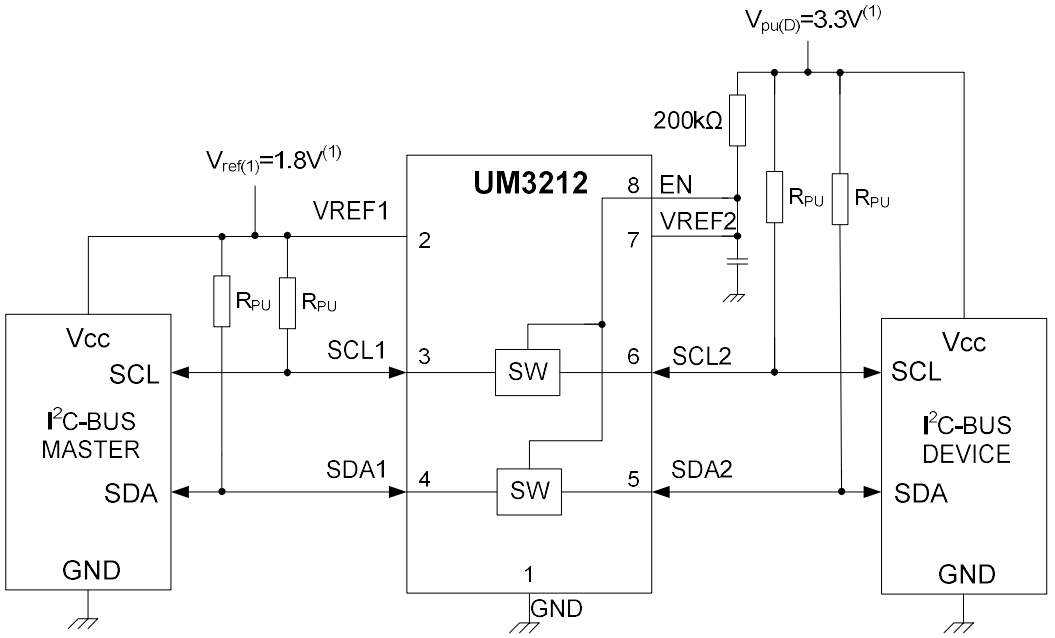


a. Load circuit **b. Timing diagram; high-impedance scope probe used**

$S1$ = translating up; $S2$ = translating down.
C_L includes probe and jig capacitance.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 5 ns; t_f ≤ 5 ns.
The outputs are measured one at a time, with one transition per measurement.

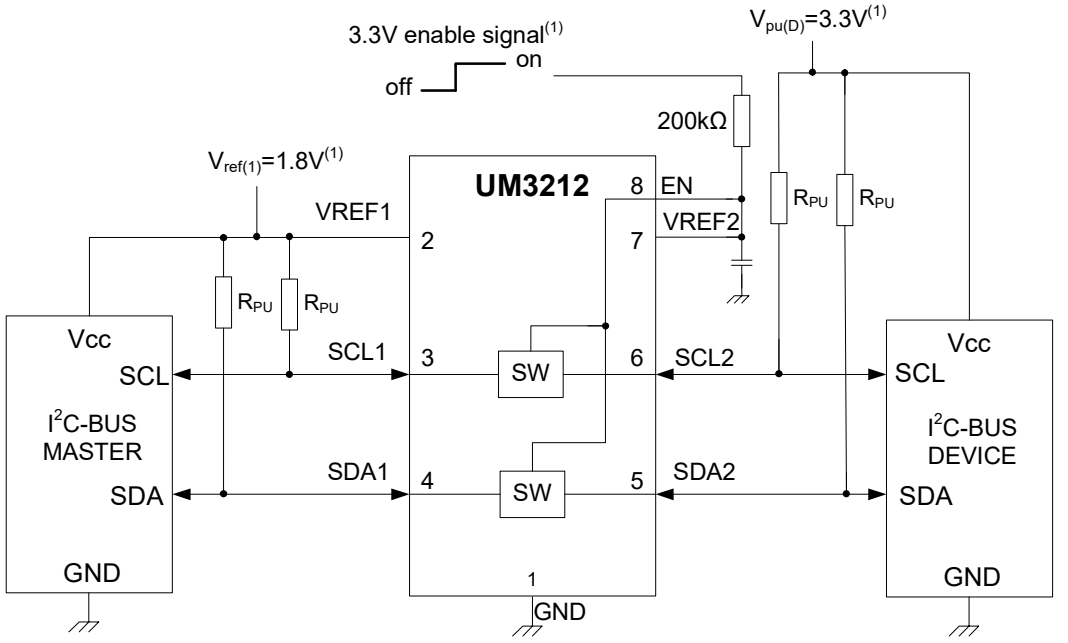
Fig 1. Load circuit for outputs

Typical Application Circuit



(1) The applied voltages at $V_{ref(1)}$ and $V_{pu(D)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Fig 2. Typical application circuit (switch always enabled)



(1) In the Enabled mode, the applied enable voltage $V_{I(EN)}$ and the applied voltage at $V_{ref(1)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Fig 3. Typical application circuit (switch enable control)

Applications Information

Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to HIGH side $V_{pu(D)}$ through a pull-up resistor (typically 200kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended. The I^2C-bus master output can be totem pole or open-drain (pull-up resistors may be required) and the I^2C-bus device output can be totem pole or open-drain (pull-up resistors are required to pull the SCL2 and SDA2 outputs to $V_{pu(D)}$). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ($V_{ref(1)}$) is connected to the processor core power supply voltage. When VREF2 is connected through a 200kΩ resistor to a 3.3V to 5.5V $V_{pu(D)}$ power supply, and $V_{ref(1)}$ is set between 1.0 V and ($V_{pu(D)}$ −1V), the output of each SCL1 and SDA1 has a maximum output voltage equal to VREF1, and the output of each SCL2 and SDA2 has a maximum output voltage equal to $V_{pu(D)}$.

Application Operating Conditions

Refer to Figure 2

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Unit
$V_{bias(ref)(2)}$	Reference Bias Voltage (2)		$V_{ref(1)}$+0.6	2.1	5	V
$V_{I(EN)}$	Input Voltage on Pin EN		$V_{ref(1)}$+0.6	2.1	5	V
$V_{ref(1)}$	Reference Voltage (1)		0	1.5	4.4	V
$I_{sw(pass)}$	Pass Switch Current		-	14	-	mA
I_{ref}	Reference Current	Transistor	-	5	-	μA
T_{amb}	Ambient Temperature	Operating in Free-Air	-40	-	+85	°C

Note 7: All typical values are at T_{amb}=25°C.

Sizing Pull-Up Resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15mA, the pull-up resistor value is calculated as:

$$R_{PU} = \frac{V_{pu(D)} - 0.35V}{0.015\ A}$$

The table below summarizes resistor reference voltages and currents at 15mA, 10mA, and 3mA. The resistor values shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the UM3212 device at 0.175V, although the 15mA only applies to current flowing through the UM3212 device

Pull-Up Resistor Values

Calculated for V_{OL}=0.35V; assumes output driver V_{OL}=0.175V at stated current.

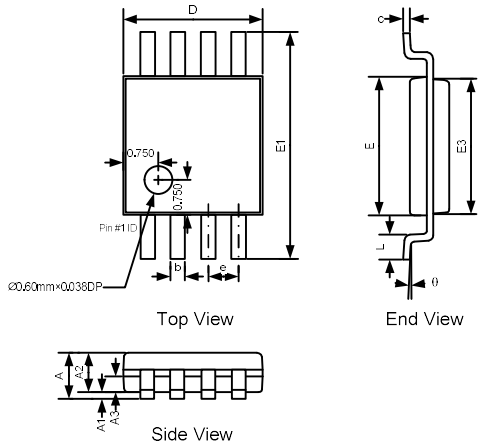
$V_{pu(D)}$	Pull-Up Resistor Value (Ω)					
	15mA		10mA		3mA	
	Nominal	+10% (Note 8)	Nominal	+10% (Note 8)	Nominal	+10% (Note 8)
5V	310	341	465	512	1550	1705
3.3V	197	217	295	325	983	1082
2.5V	143	158	215	237	717	788
1.8V	97	106	145	160	483	532
1.5V	77	85	115	127	383	422
1.2V	57	63	85	94	283	312

Note 8: +10% to compensate for V_{CC} range and resistor tolerance.

Package Information

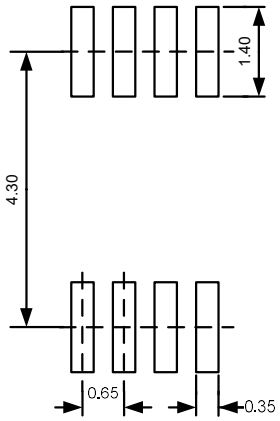
UM3212M8: MSOP8

Outline Drawing



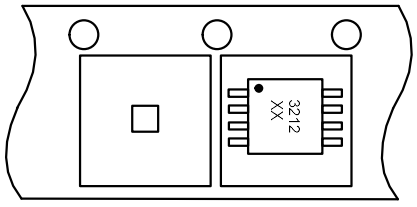
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.10	-	-	0.043
A1	0.02	-	0.15	0.0008	-	0.006
A2	0.75	0.86	0.95	0.030	0.034	0.037
A3	0.29	0.39	0.49	0.011	0.015	0.019
b	0.22	-	0.38	0.009	-	0.015
c	0.08	0.15	0.23	0.003	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	4.70	4.90	5.10	0.185	0.193	0.201
E3	2.85	2.95	3.05	0.112	0.116	0.120
e	0.65BSC			0.026BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
θ	0°	-	8°	0°	-	8°

Land Pattern



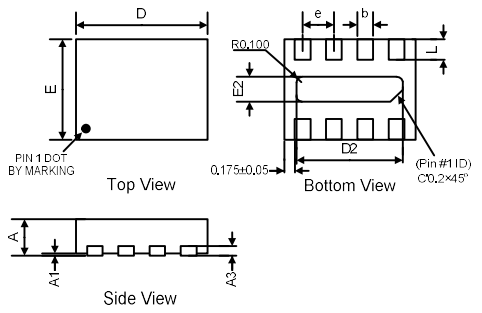
NOTES:
1. Compound dimension: 3.00×3.00;
2. Unit: mm;
3.General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



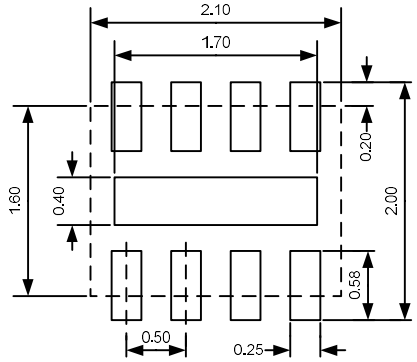
UM3212DA: DFN8 2.1×1.6

Outline Drawing



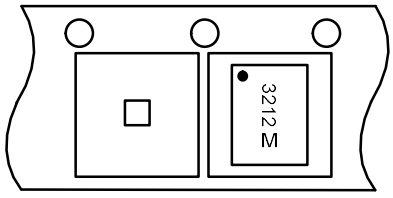
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.575	0.605	0.020	0.023	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.15TYP			0.006TYP		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	2.05	2.10	2.175	0.081	0.083	0.086
D2	1.60	1.70	1.80	0.063	0.067	0.071
E	1.55	1.60	1.675	0.061	0.063	0.066
E2	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50TYP			0.020TYP		
L	0.275	-	0.38	0.011	-	0.015

Land Pattern



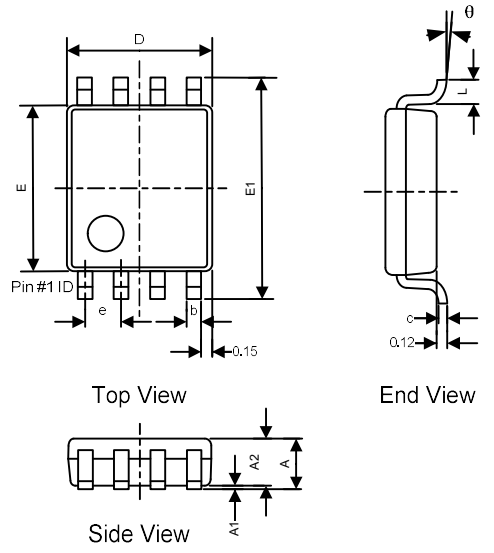
NOTES:
1. Compound dimension: 2.10×1.60;
2. Unit: mm;
3.General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



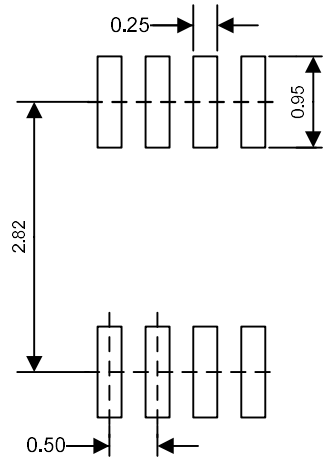
UM3212V8: VSSOP8

Outline Drawing



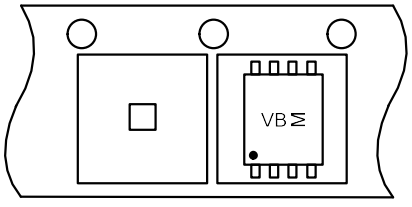
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.60	0.75	0.90	0.023	0.029	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.60	0.70	0.80	0.023	0.027	0.031
b	0.17	-	0.27	0.007	-	0.011
c	0.08	-	0.23	0.003	-	0.009
D	1.90	2.00	2.10	0.075	0.079	0.083
E	2.20	2.30	2.40	0.086	0.090	0.094
E1	3.00	3.10	3.20	0.118	0.122	0.126
e	0.50BSC			0.020BSC		
L	0.20	0.28	0.35	0.008	0.011	0.014
θ	0°	3°	6°	0°	3°	6°

Land Pattern



NOTES:
1. Compound dimension: 2.00×2.30;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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