UNI-SEMICONDUCTOR CO . , LTD
宇 力 半 导 体 有 限 公 司

U6119 Data Sheet

DC-DC CONVERTER CONTROL CIRCUITS

■VIN 200V/100V MOS
■OUTPUT SWITCH ADJ
■2% REFERENCE ACCURACY
■LOW QUIESCENT CURRENT: 15UA (TYP.)
■OUT MOSFET
■FREQUENCY OPERATION TO 200KHz
■ACTIVE CURRENT LIMITING

DESCRIPTION

The U6119 series is a monolithic control circuit delivering the main functions for DC-DC voltage converting.

The device contains an internal temperature compensated reference, comparator, duty cycle controlled oscillator with an active current limit circuit, driver and high current output switch.

Output voltage is ADJ Vol ,NO-integrated two external resistors with a 2% reference accuracy.

Employing a minimum number of external components the U6119 devices series is designed for Step-Down applications.

■ Features

Support Flyback and Buck Topology:

QR-Buck CC Control (SEL= GND)

- Low Standby Power <70mW
- Programmable Cable Drop Compensation: (CDC) in PSR CV Mode
- Built-in AC Line & Load CC Compensation
- Build in Protections:
  - Short Load Protection (SLP)
  - On-Chip Thermal Shutdown (OTP)
  - Cycle-by-Cycle Current Limiting
  - Leading Edge Blanking (LEB)
  - Pin Floating Protection
- VDD UVLO OVP & Clamp
- Package (SOP7)

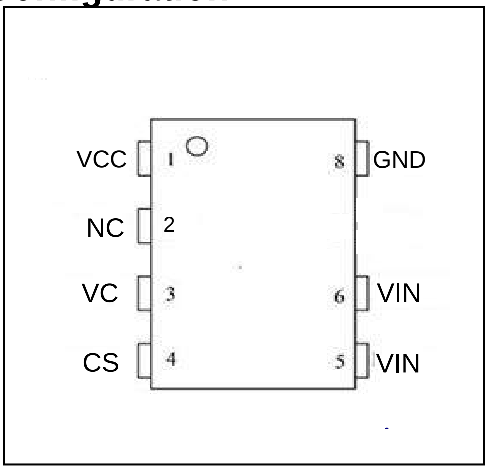
APPLICATIONS

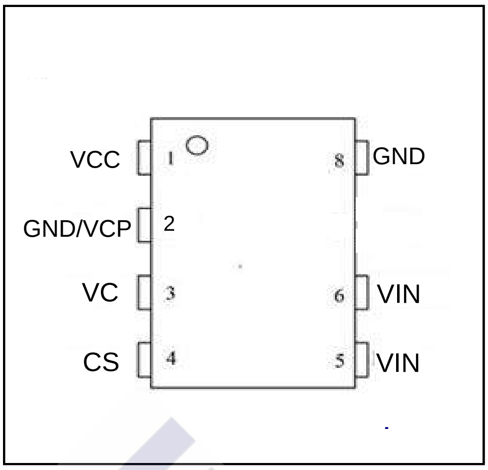
- **Electric-Vehicle, Electric-Bicycle Apliance**
- **Industry Controls**

Base Part Number	Package Type	Rsdon		VOFFSET
		min(ohm)	max(ohm)	
U6119S	SOP7	0.75	0.85	200V
U6119SA	SOP7	0.1	0.15	100V
U6119SC	SOP7	0.1	0.15	100V

Number	DESCRIPTION
U6119SC	SOP-7，无卤、编带盘装，3000 颗/卷
U6119S/SA	SOP-7，无卤、编带盘装，3000 颗/卷

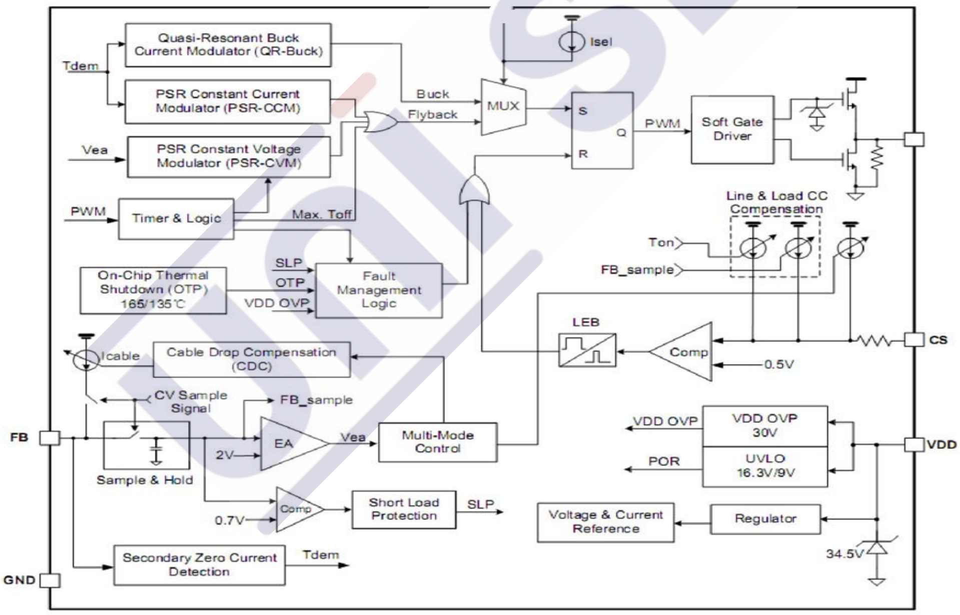
Pin Configuration





U6119S TOP VIEW U6119SA/SC

Block Diagram

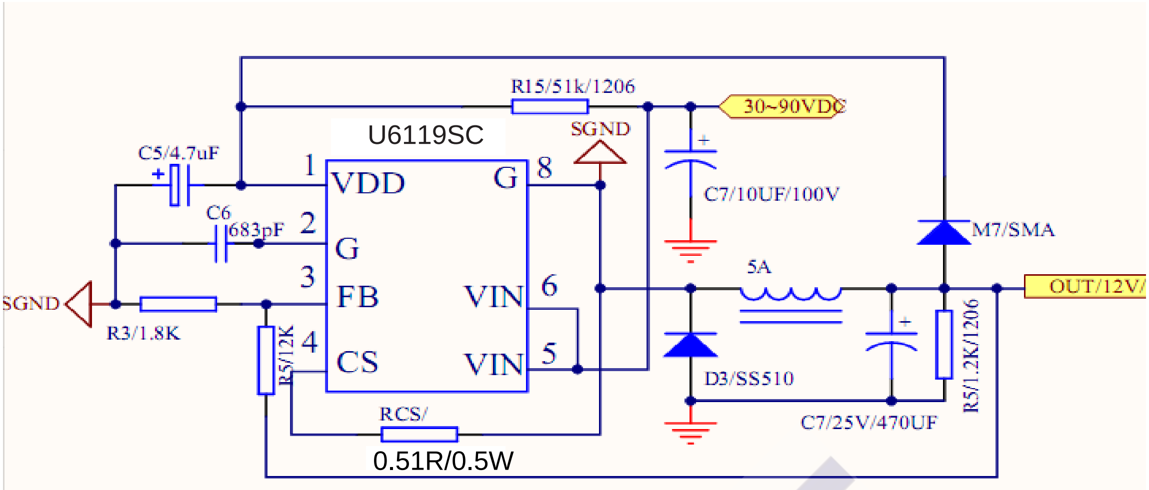


Pin Description

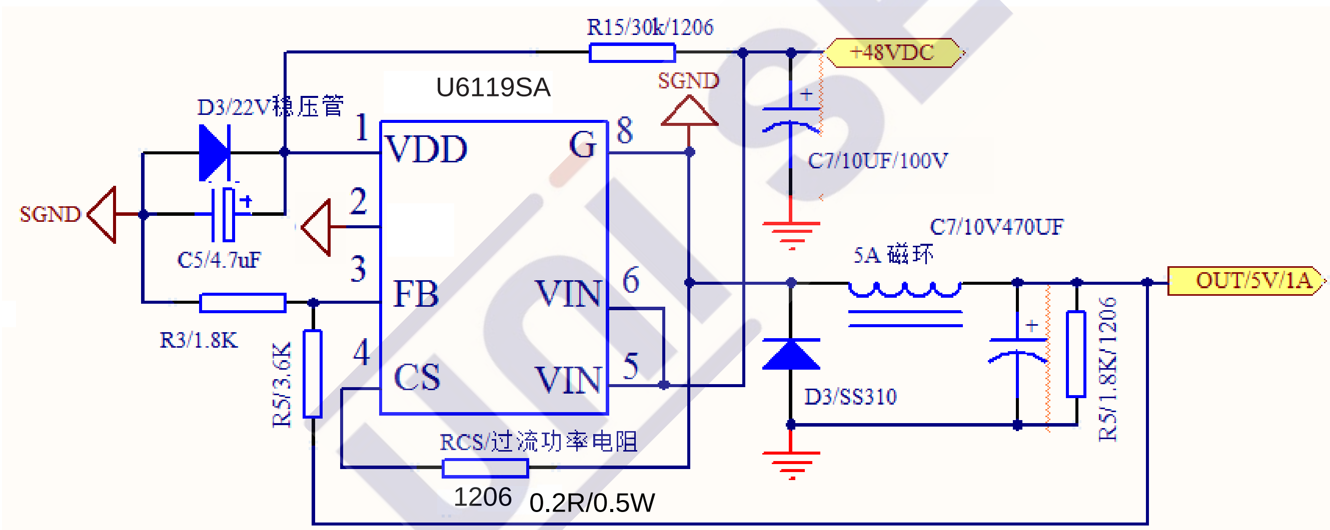
Pin Num	Pin Name	I/O	Description
1	VDD	P	Power Supply
3	VC	I	The voltage feedback
4	CS	I	Current sense input
5,6	VIN	O	HV VIN Pin.
8	GND	P	Ground
2		P	U6119S:NC U6119SA/SC:GND/VCP

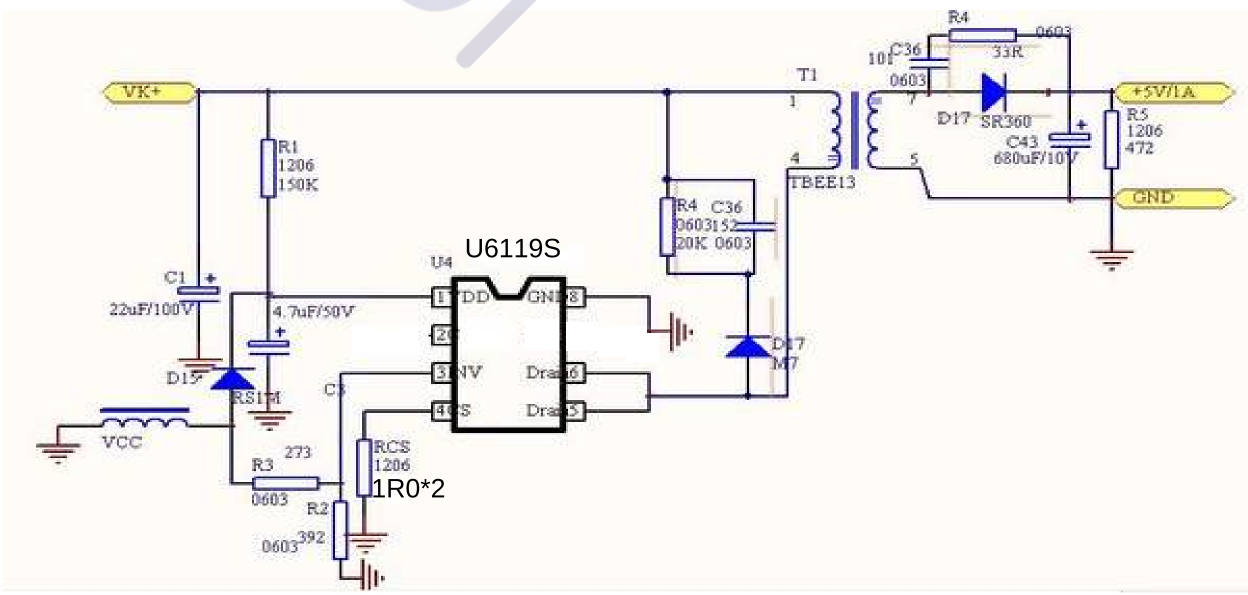
■ Typical Application Circuit

l Test Condition (V_{OUT} = 12V)



l Test Condition (V_{OUT} = 5V)





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{dd}	Power Supply Voltage	26	V
V_{ir}	Comparator Input Voltage Range	-0.3 to 20	V
I_{ds}	Driver Drain Current	1/ 1.5	A
I_{SW}	Switch Current	3/5	A
P_{tot}	Power Dissipation at T_{amb} = 25 °C (for **ESOIC Package**)	1.0	W
	(for **SOIC Package**)	0.625	W
T_{op}	Operating Ambient Temperature Range (for **AC SERIES**)	- 40 to 1 4 5	°C
	(for **AB SERIES**)	- 40 to 1 4 5	°C
T_{stg}	Storage Temperature Range	- 40 to 150	°C

Absolute Maximum Rating are those values beyond which damage to the device may occur.
Functional operation under these condition is not implied.

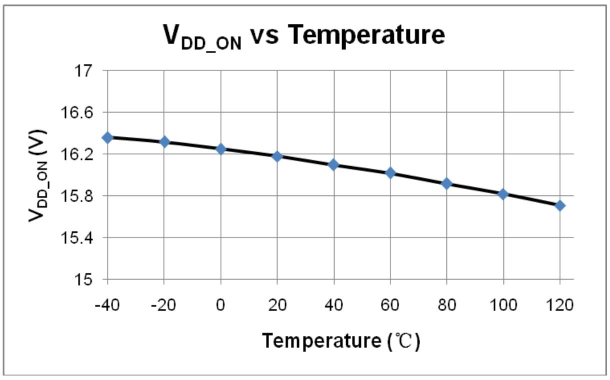
ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_{CC} = 60V, T = T_{LOW} to T_{HIGH}, unless otherwise specified, see note 2)

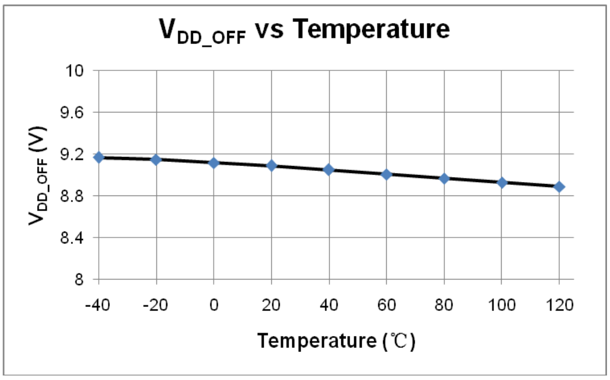
Control Function Section						
T_{LEB}	Current Sense Leading Edge Blanking Time	(Note 2)		200		ns
T_{on_min}	Minimum On Time	(Note 2)		300		ns
T_{on_max}	Maximum On Time		10	12	14	us
T_{ss}	Internal Soft Start Time	(Note 2)		5		ms
F_{clk}	Internal Frequency Clock			ADJ	200	kHz
ΔF_{clk}	Peak to Peak Frequency Jitter			10		kHz
BV_{DSS}	MOSFET Break Down Voltage			200/100		V
Over Temperature						
T_{SD}	Thermal Shut Down	(Note 2)		140		°C
T_{RC}	Thermal Recovery	(Note 2)		130		°C

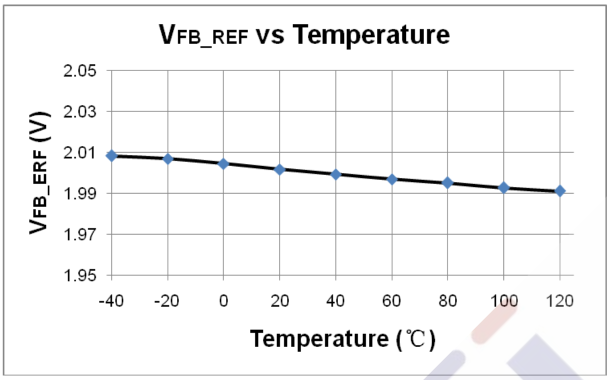
Note1. Stresses listed as the above **"**Maximum Ratings**"** may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

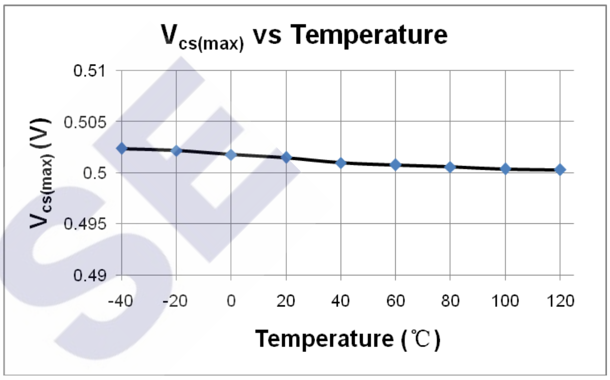
Note2. It's guaranteed by design and functionally tested during production manufacture.

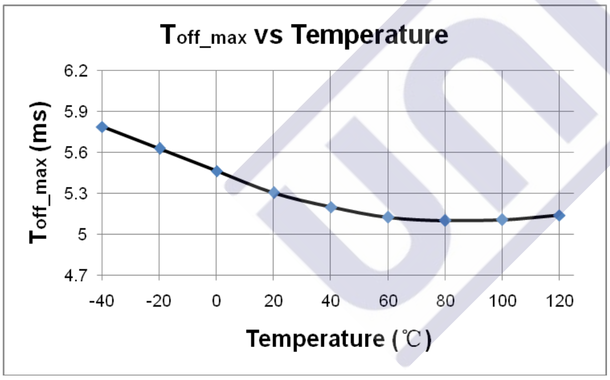
n Characterization Plots

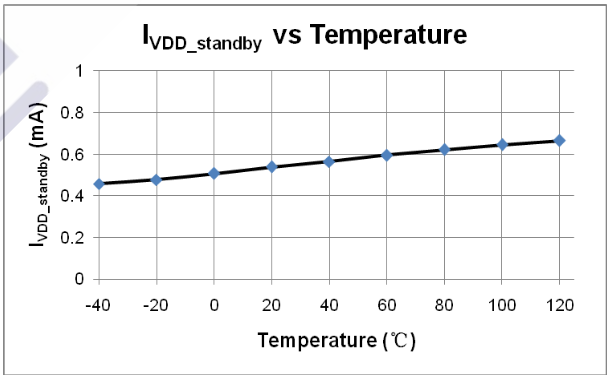












PERATION DESCRIPTION

Over Temperature Protection

When the IC temperature is over 140 °C, the IC shuts down. Only when the IC temperature drops to 80 °C, the IC restarts to work.

Light Load Mode Operation

To save more power loss in no load condition, U6119 family adopts a light load mode operation. When the switching period is longer than 300us, the peak current limit will be decreased to 100mA. With this feature, ultra no load power loss consumed by the pre-load can be <5mW.

The Selection of the DC Output Stage

The output power rage determines the selection of the CS and LX design. For Pout<4W, it's recommended to use CV rectification; for Pout>4W, it's recommended to use CC rectification.

COMPONENTS SELECTION

Start-Up Resistor (R_{ST}) and Hold-up Capacitor (C_{VIN})

To keep proper start-up operation and meet the start-up time requirement, the value of the VIN capacitor C_{VIN} and start-up resistor R_{ST} need well designed.

Firstly make sure the current flowing through the RST is larger than the IC start-up current I_VIN_ST (3uA typically) and lower than the IC operation current I_VIN_op (800uA typically).

$$\frac{V_{in\_max}}{I_{\_VIN\_op}} < R_{ST} < \frac{V_{in\_min}}{I_{\_VIN\_ST}}$$

V_{in_min}: The minimum peak value of DC input voltage.

V_{in_max}: The maximum peak value of DC input voltage. For universal input, V_{in_max} is 180V.

Secondly the VIN capacitor is recommended to be selected by the following equation:

$$C_{VIN} < \frac{\left(\frac{V_{in\_min}}{R_{ST}} - I_{\_VIN\_ST}\right) \cdot T_{ST}}{V_{IN\_ON}}$$

For better line and load regulation, the value of C_{VIN} is recommended to be as small as possible. Typically 1uF is recommended. If the VIN capacitance is not big enough to cause the start-up failed; increase the value of C_{VIN} and decrease the RST, re-do the calculation of above equation until ideal start-up performance is got.

For better noise immunity, it's recommended that the VIN capacitor be placed as close as possible to the VIN Pin.

- **Quasi Resonant Buck (QR-Buck) Constant Current Control for LED Lighting**

If SEL pin is short to GND, U6119 will works in Quasi-Resonant Buck mode. In QR-Buck mode, the IC keeps CS peak current constant and starts new PWM cycle with valley switching. Therefore, high precision CC and high conversion efficiency can be achieved simultaneously. The average output current is given by:.

$$I_{Buck\_CC\_OUT}(mA) \cong \frac{1}{2} \times \frac{500mV}{Rcs(\Omega)}$$

Freewheeling Diode (D_1)

Diode D1 should be an ultra-fast type. Slow diode is not acceptable, because the inductor is always working in continuous conduction mode during start-up period. Slow diode will cause high current spike which will falsely make the Power MOESFET turned off and prevent the output voltage reach regulation. Slow diode will also cause extra power loss and make the efficiency lower down. A 100V/1A diode with recovery time <50ns is recommended for Buck converter and 200V/A diode with recovery time <50ns is recommended for Buck/Boost converter, such as ES1D and ES2D.

Feedback Diode (D_F)

The information of the output voltage is sent the IC through the diode DF which can be a slow diode, such as 1N400X series. To minimize the output voltage error, the forward voltage of D1 and D_F should match. At the same time, the power supply of the IC will be taken place by the output voltage through DF after the soft-start.

Inductor (L)

For Buck converter, the selection of L can be calculated by the following equation:

$$L = \frac{2 \cdot (V_{in\max} - V_{DS} - V_o) \cdot V_o \cdot I_o}{h \cdot [I_{\lim it}^2 - (2 \cdot I_o - I_{\lim it})^2] \cdot (V_{in\_\min} - V_{DS}) \cdot f_{sw}} \quad \text{for CCM}$$

$$L = \frac{2 \cdot (V_{in\max} - V_{DS} - V_o) \cdot V_o \cdot I_o}{h \cdot I_{\lim it}^2 \cdot (V_{in\_\min} - V_{DS}) \cdot f_{sw}} \quad \text{for DCM}$$

For Buck/Boost converter, the selection of L can be calculated by the following equation:

$$L = 2 \cdot \frac{P_o}{h \cdot [I_{\lim it}^2 - (2 \cdot I_o - I_{\lim it})^2] \cdot f_{sw}} \quad \text{for CCM}$$

$$L = 2 \cdot \frac{P_o}{h \cdot I_{\lim it}^2 \cdot f_{sw}} \quad \text{for DCM}$$

Where:

When $I_o > I_{limit}/2$, it's working in CCM operation mode; when $I_o < I_{limit}/2$, it's working in DCM operation mode.

V_{in_min}: The minimum DC input voltage after the rectified diode bridge. It's recommended to keep V_{in_min} higher than 70V always.

η : The overall estimated efficiency, the typical value of 0.8 is recommended for DCM and 0.7 for CCM.

V_o: The averaged output voltage.

Io: The averaged output current.

V_F: The forward conduction voltage of the freewheeling diode D1.

V_{DS}: The MOSFET conduction voltage during it's turned on. The typical value of 5V is recommended

F_{sw}: The switching frequency and 56 kHz is recommended.

I_{limit}: The minimum peak inductor current limit.

Any standard off-the-shelf inductor that meets the design requirement can be selected. The value of the inductor L determines the averaged switching frequency according to the rule of power balance. Typically a 0.68mH-22uH inductor is recommended to be used with Isat>0.6A

Output Capacitor (C_{OUT})

The selection of output capacitor is determined by the requirement of the output voltage ripple. To make the output ripple small enough, a large value of C_{OUT} is needed. But large value of C_{OUT} will increase the cost and need longer time for soft-start. Typically a capacitor with 220uF/25V is recommended.

Pre-Load Resistor (R_L)

At no load condition, the switching frequency is determined by the value of C_{VIN} and the operation current of the IC not by the output voltage information. Combined with the value of the selection of inductor L1, there's a minimum input power for this circuit. To keep the regulation of the output voltage at no load condition, a minimum load current is needed. For 15V application, a resistor with value around of 30k ohm is recommended.

Table 1 shows the relationship between these circuit parameters and the key operation performance.

Table 1

	Start-up Time	Output Ripple	No Load
R_{ST} ↑	↑	→	↓
C_{VIN} ↑	↑	↑	↓
L ↑	↓	↑	↑
C_{OUT} ↑	↑	↓	→

- **Programmable Cable Drop Compensation (CDC) in CV Mode**

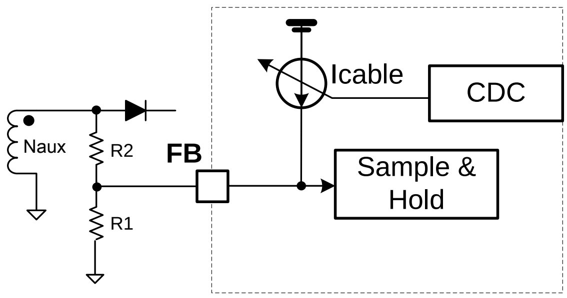
In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In U6119, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.5) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in Fig.), the cable loss compensation can be programmed. The percentage of maximum

compensation is given by

$$\frac{\Delta V(cable)}{Vout} \approx \frac{Icable\_max \times (R1//R2)}{V_{FB\_REF}} \times 100\%$$

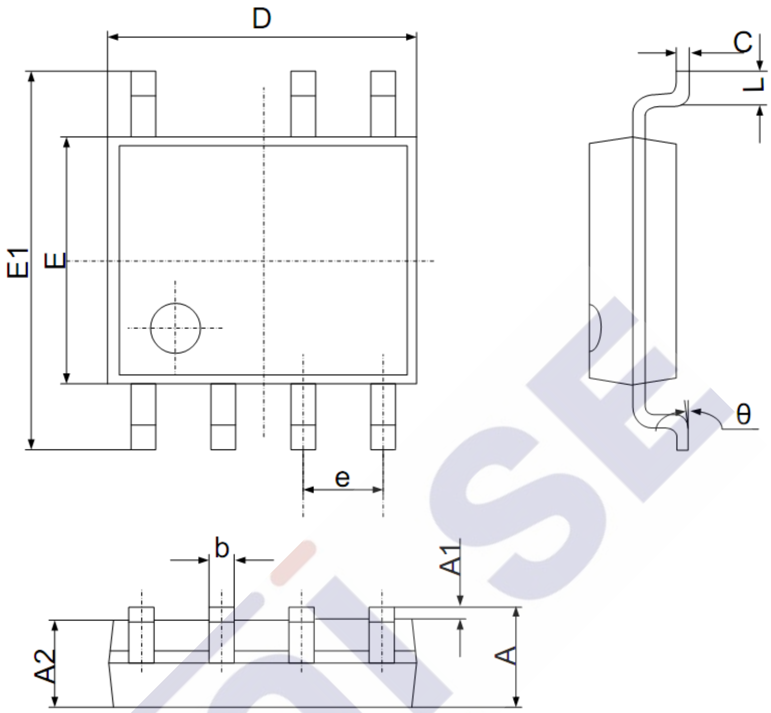
For example, R1=3 K Ω , R2=18K Ω , The percentage of maximum compensation is given by

$$\frac{\Delta V(cable)}{Vout} = \frac{63uA \times (3K//18K)}{2V} \times 100\% = 8.1\%$$



■ 封装尺寸

SOP-7



符号	尺寸（毫米）		尺寸（英寸）	
	最小	最大	最小	最大
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.002	0.010
A2	1.350	1.550	0.049	0.065
b	0.330	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.203
e	1.270（中心到中心）		0.050（中心到中心）	
E1	5.800	6.200	0.228	0.244
E	3.800	4.000	0.15	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

IMPORTANT NOTICE

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