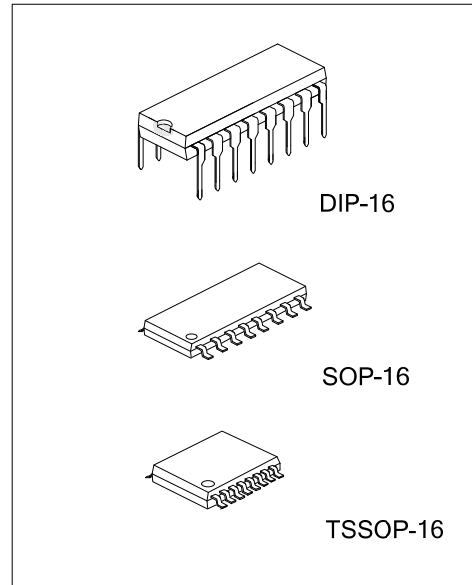




4052

CMOS IC

DIFFERENTIAL 4-CHANNEL ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



DESCRIPTION

The UTC **4052** is differential 4-channel analog multiplexers/demultiplexers for application as digitally-controlled analog switches.

The device has two binary control inputs and an inhibit input. It feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

FEATURES

- * Wide Analog Voltage Range: $V_{DD}-V_{EE} = 3V\sim 18V$.
(Note: V_{EE} must be $\leq V_{SS}$)
- * Break-Before-Make Switching Eliminates Channel Overlap.
- * Linearized Transfer Characteristics
- * Implement an DP4T Switch Effectively.
- * Pin to Pin Replacement for CD4052

ORDERING INFORMATION

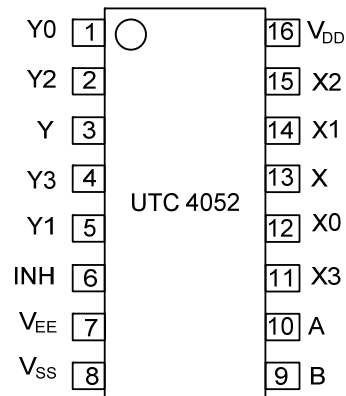
Ordering Number		Package	Packing
Lead Free	Halogen Free		
4052L-D16-T	4052G-D16-T	DIP-16	Tube
-	4052G-S16-R	SOP-16	Tape Reel
-	4052G-P16-R	TSSOP-16	Tape Reel

<p>4052L-D16-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D16: DIP-16, S16: SOP-16, P16: TSSOP-16 (3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING

DIP-16	SOP-16 / TSSOP-16

■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN No.	SYMBOL	NAME AND FUNCTION
13, 3	X, Y	Commons Input/Output
6	INH	Inhibit Input
7	V_{EE}	Supply Voltage
8	V_{SS}	Ground
10, 9	A, B	Binary Control Inputs
12, 14, 15, 11	X0~X3	X Channel Inputs/Outputs
1, 5, 2, 4	Y0~Y3	Y Channel Inputs/Outputs
16	V_{DD}	Positive Supply Voltage

Note: Control Inputs referenced to V_{SS} . Analog Inputs and Outputs reference to V_{EE} . V_{EE} must be $< V_{SS}$.

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V_{EE} , $V_{SS} \geq V_{EE}$)	V_{DD}	-0.5 ~ +18	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	V_{IN} , V_{OUT}	-0.5 ~ $V_{DD} + 0.5$	V
Input Current (DC or Transient), per Control Pin	I_{IN}	±10	mA
Switch Through Current	I_{SW}	±25	mA
Power Dissipation	P_D	700	mW
Derating above 65°C		7	mW/°C
Junction Temperature	T_J	125	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})						
Power Supply Voltage Range	V_{DD}	$V_{DD} - 3 \geq V_{SS} \geq V_{EE}$	3		18	V
Quiescent Current per Package	I_Q	Control Inputs: $V_{IN} = V_{SS}$ or V_{DD} Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{SW} \leq 500\text{mV}$ (Note 2)		0.005	5	μA
				0.010	10	μA
				0.015	20	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	$T_A=25^\circ\text{C}$ only (The channel component, $(V_{IN}-V_{OUT})/R_{ON}$, is excluded.)		$(0.07 \mu\text{A}/\text{kHz}) f + I_Q$		μA
				$(0.20 \mu\text{A}/\text{kHz}) f + I_Q$		μA
				$(0.36 \mu\text{A}/\text{kHz}) f + I_Q$		μA
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V_{EE})						
Recommended Peak to Peak Voltage Into or Out of the Switch	$V_{I/O}$	Channel On or Off	0		V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (Note2)	ΔV_{SW}	Channel On	0		600	mV
Output Offset Voltage	$V_{O(OFF)}$	$V_{IN} = 0\text{V}$, No Load		10		μV
ON Resistance	R_{ON}	$\Delta V_{SW} \leq 500\text{mV}$ (Note2) $V_{IN} = V_{IL}$ or V_{IH} (Control), and $V_{IN} = 0$ to V_{DD} (Switch)		250	1050	Ω
				120	500	Ω
				80	280	Ω
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR_{ON}			25	70	Ω
				10	50	Ω
				10	45	Ω
Off Channel Leakage Current	I_{OFF}	$V_{IN} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel, $V_{DD}=15\text{V}$		±0.05	±100	nA
Capacitance, Switch I/O	$C_{I/O}$	Inhibit = V_{DD}		10		pF
Capacitance, Common O/I	$C_{O/I}$	Inhibit = V_{DD}		17		pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	Pins Not Adjacent		0.15		pF
		Pins Adjacent		0.47		
CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V_{SS})						
Low Level Input Voltage	V_{IL}	$R_{ON} = \text{per spec}$, $I_{OFF} = \text{per spec}$		2.25	1.5	V
				4.50	3.0	V
				6.75	4.0	V
High Level Input Voltage	V_{IH}	$R_{ON} = \text{per spec}$, $I_{OFF} = \text{per spec}$	3.5	2.75		V
			7.0	5.50		V
			11	8.25		V
Input Leakage Current	I_{LEAK}	$V_{IN} = 0$ or V_{DD} , $V_{DD}=15\text{V}$		±0.00001	±0.1	μA
Input Capacitance	C_{IN}			5.0	7.5	pF

■ DYNAMIC ELECTRICAL CHARACTERISTICS

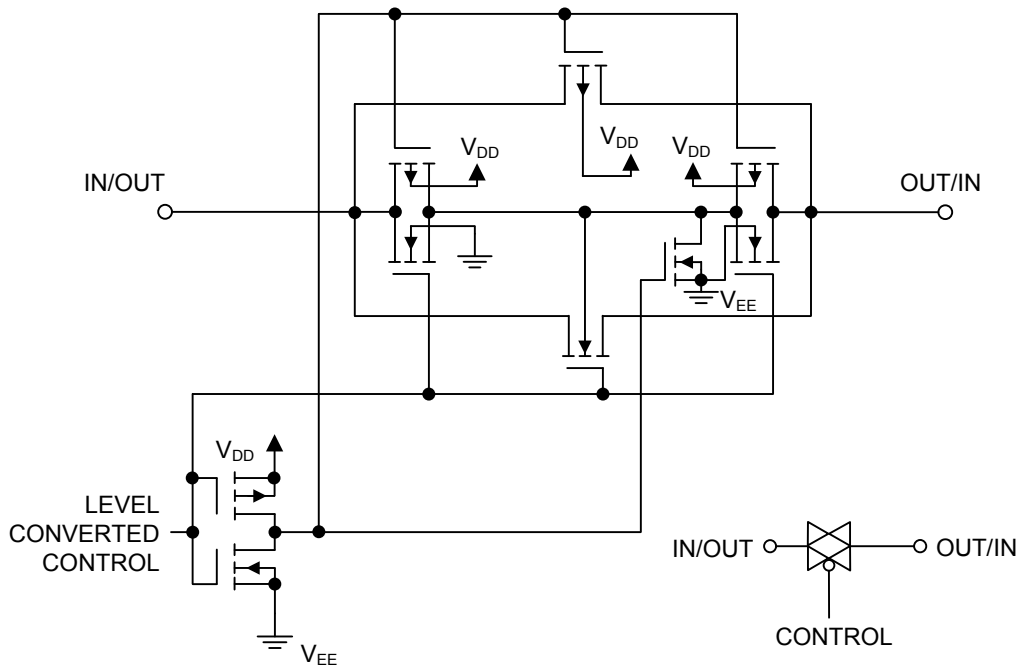
($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$, $V_{EE} \leq V_{SS}$, unless otherwise specified)

PARAMETER	SYMBOL	$V_{DD}-V_{EE}$ V_{DC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Times Switch Input to Switch Output ($R_L = 10\text{ k}\Omega$)	t_{PLH} , t_{PHL}	5	t_{PLH} , $t_{PHL} = (0.17\text{ ns/pF})C_L + 21.5\text{ns}$		30	75	ns
		10	t_{PLH} , $t_{PHL} = (0.08\text{ ns/pF})C_L + 8.0\text{ns}$		12	30	ns
		15	t_{PLH} , $t_{PHL} = (0.06\text{ ns/pF})C_L + 7.0\text{ns}$		10	25	ns
Inhibit to Output	t_{PHZ} , t_{PLZ} t_{PZH} , t_{PZL}	5	($R_L = 10\text{k}\Omega$, $V_{EE} = V_{SS}$)		300	600	ns
		10	Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level		155	310	ns
		15			125	250	ns
Control Input to Output	t_{PLH} , t_{PHL}	5	$R_L = 10\text{ k}\Omega$, $V_{EE} = V_{SS}$		325	650	ns
		10			130	260	ns
		15			90	180	ns
Total Harmonic Distortion	THD	10	$R_L = 10\text{k}\Omega$, $f = 1\text{ kHz}$, $V_{IN} = 5\text{ V}_{PP}$		0.07		%
Bandwidth	BW	10	$R_L = 1\text{k}\Omega$, $V_{IN} = 1/2 (V_{DD}-V_{EE})$ p-p, $C_L = 50\text{pF}$, $20\text{ Log}(V_{OUT}/V_{IN}) = -3\text{dB}$		17		MHz
Off Channel Feedthrough Attenuation		10	$R_L = 1\text{k}\Omega$, $V_{IN} = 1/2 (V_{DD}-V_{EE})$ p-p $f_{IN} = 30\text{MHz}$		-50		dB
Channel Separation		10	$R_L = 1\text{k}\Omega$, $V_{IN} = 1/2 (V_{DD}-V_{EE})$ p-p $f_{IN} = 3\text{MHz}$		-50		dB
Crosstalk, Control Input to Common O/I		10	$R_1 = 1\text{k}\Omega$, $R_L = 10\text{k}\Omega$ Control $t_{TLH} = t_{THL} = 20\text{ns}$, Inhibit = V_{SS}		75		mV

Notes: 1. Data of "TYP" is intended as an indication of the IC's potential performance.

2. For voltage drops across the switch (ΔV_{SW}) > 600mV (> 300mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

■ TEST CIRCUIT



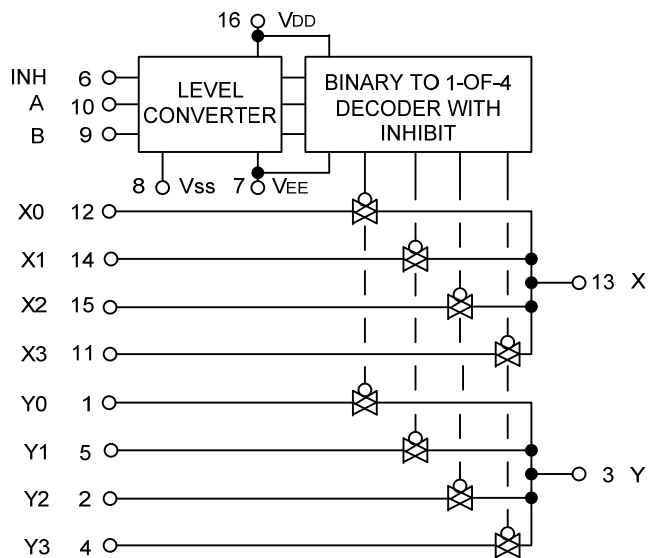
Switch Circuit Schematic

■ TRUTH TABLE

TRUTH TABLE

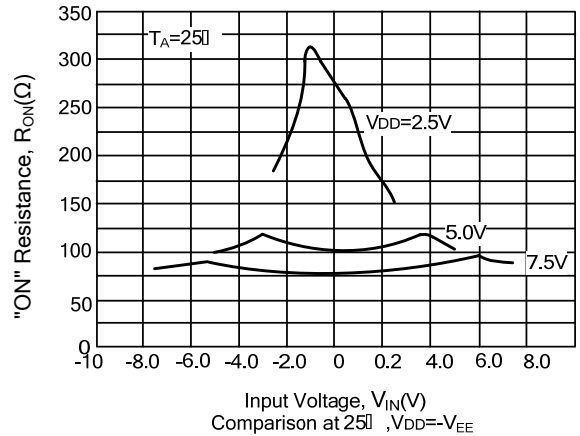
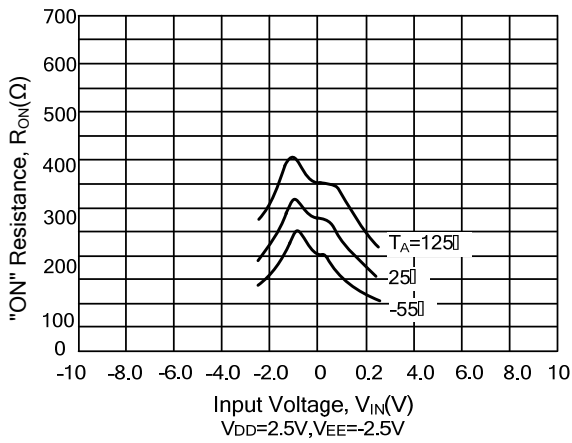
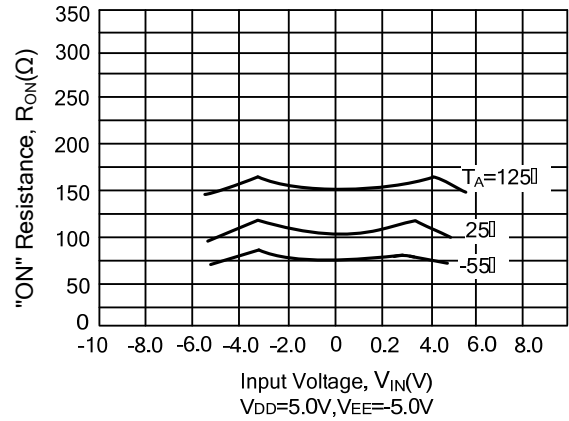
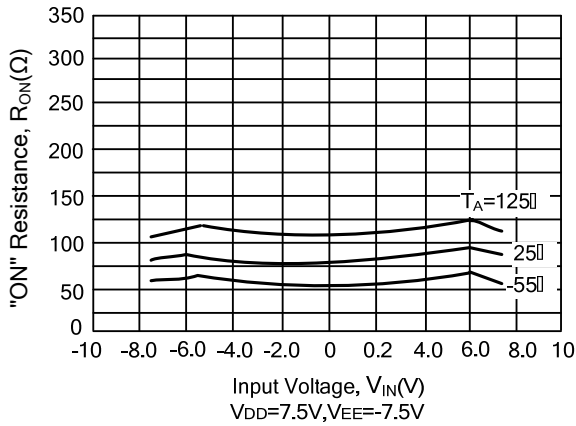
Control Inputs		ON Switches	
Inhibit	Select		Y0 X0 Y1 X1 Y2 X2 Y3 X3
	B	A	
0	0	0	Y0 X0
0	0	1	Y1 X1
0	1	0	Y2 X2
0	1	1	Y3 X3
1	X	X	None

* X=Don't Care



UTC 4052 Functional Diagram

■ TYPICAL CHARACTERISTICS



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