

## MC4558

## LINEAR INTEGRATED CIRCUIT

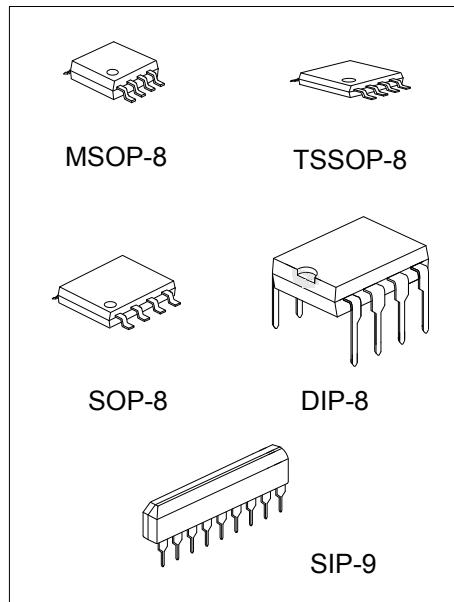
## DUAL OPERATIONAL AMPLIFIER

## ■ DESCRIPTION

The UTC **MC4558** is a monolithic integrated circuit designed for dual operational amplifier.

## ■ FEATURES

- \* No frequency compensation required
- \* No latch-up
- \* Large common mode and differential voltage range
- \* Parameter tracking over temperature range
- \* Gain and phase match between amplifiers
- \* Internally frequency compensated
- \* Low noise input transistors

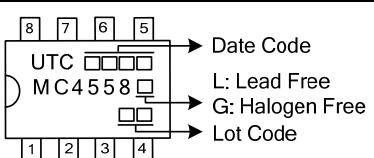
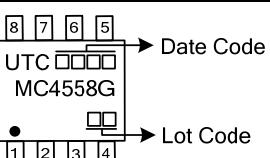
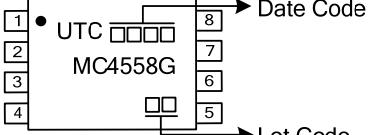
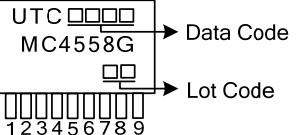


## ■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
MC4558L-D08-T	MC4558G-D08-T	DIP-8	Tube
-	MC4558G-G09-T	SIP-9	Tube
-	MC4558G-P08-R	TSSOP-8	Tape Reel
-	MC4558G-S08-R	SOP-8	Tape Reel
-	MC4558G-SM1-R	MSOP-8	Tape Reel

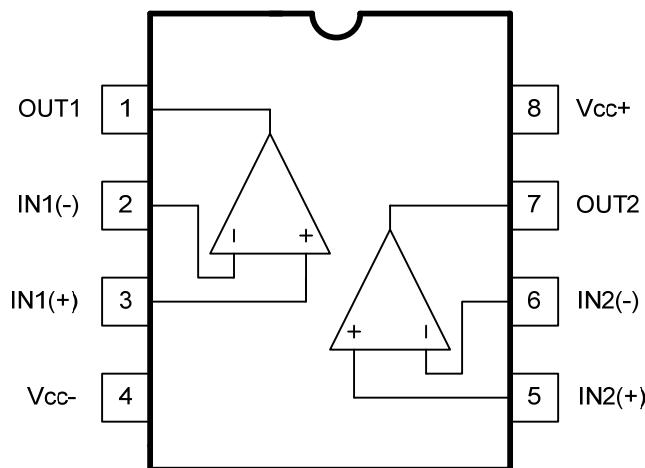
MC4558L-D08-T	(1)T: Tube, R: Tape Reel (2)D08: DIP-8, G09: SIP-9, P08: TSSOP-8 S08: SOP-8, SM1: MSOP-8 (3)L: Lead Free, G: Halogen Free and Lead Free
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## ■ MARKING

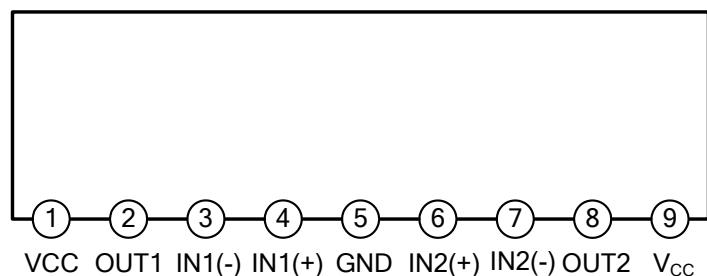
DIP-8	SOP-8/MSOP-8
 <p>8 7 6 5 UTC MC4558 1 2 3 4</p> <p>Date Code L: Lead Free G: Halogen Free Lot Code</p>	 <p>8 7 6 5 UTC MC4558 1 2 3 4</p> <p>Date Code Lot Code</p>
TSSOP-8	SIP-9
 <p>1 • UTC MC4558 2 3 4</p> <p>Date Code Lot Code</p>	 <p>UTC MC4558 1 2 3 4 5 6 7 8 9</p> <p>Data Code Lot Code</p>

### ■ PIN CONFIGURATIONS

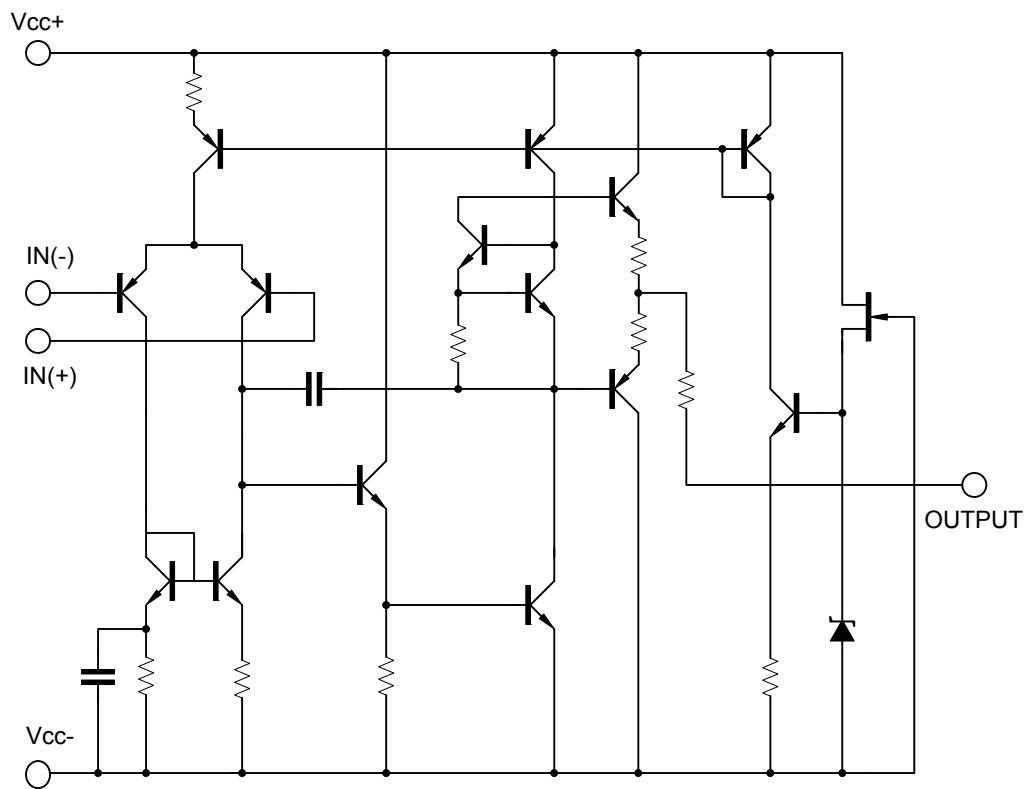
SOP-8/DIP-8/MSOP-8/TSSOP-8



SIP-9



### ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	$\pm 22$	V
Differential input voltage	$V_{I(DIFF)}$	$\pm 18$	V
Power Dissipation	DIP-8	600	mW
	SOP-8	400	mW
	TSSOP-8	300	mW
	SIP-9	750	mW
	MSOP-8	250	mW
Input Voltage	$V_{IN}$	$\pm 15$	V
Junction Temperature	$T_J$	+125	°C
Operating Temperature	$T_{OPR}$	-20 ~ +85	°C
Storage Temperature	$T_{STG}$	-40 ~ +150	°C

Note 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

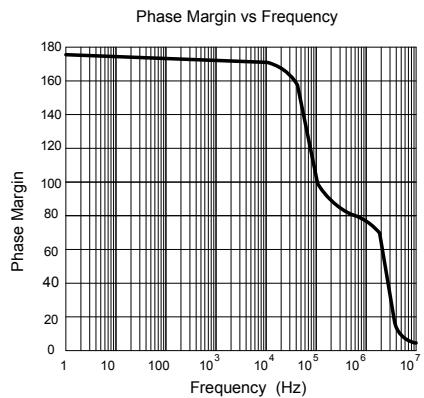
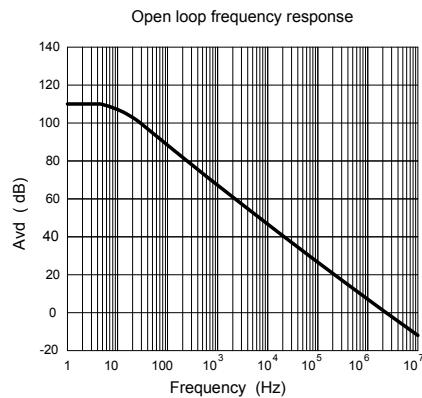
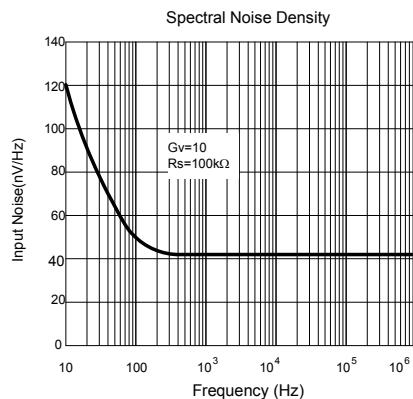
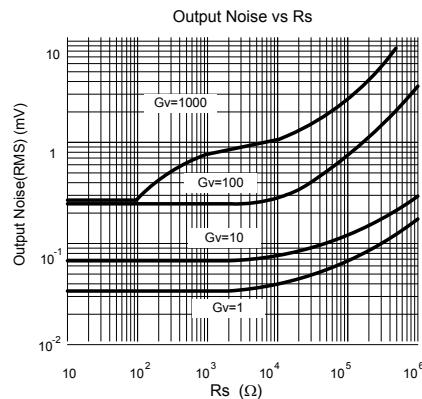
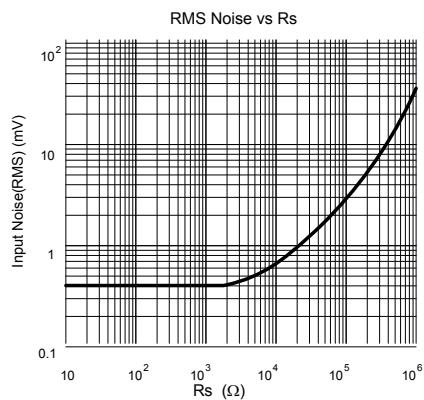
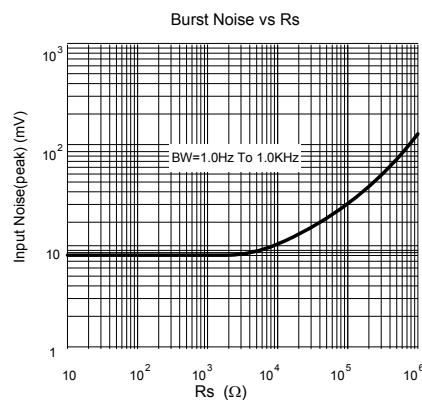
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The device is guaranteed to meet performance specification within 0°C ~ +70°C operating temperature range and assured by design from -20°C ~ +85°C.

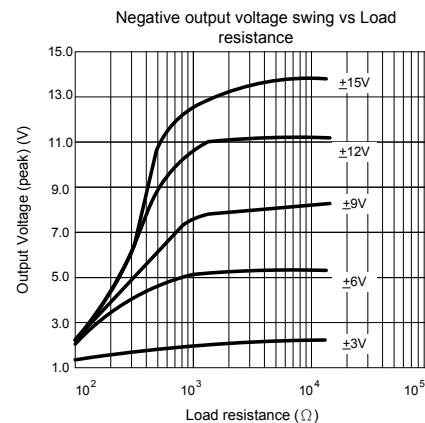
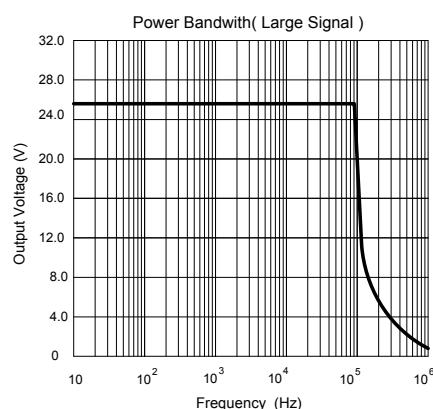
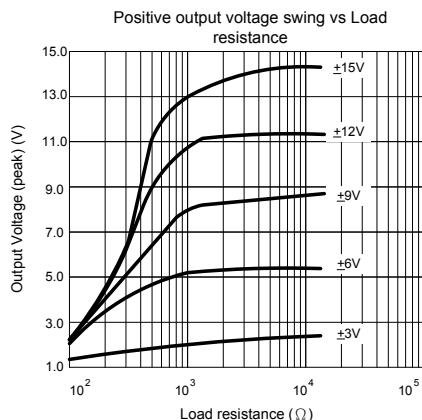
■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ ,  $V_{CC}=15\text{V}$ ,  $V_{EE}=-15\text{V}$ )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current, all Amp, no load	$I_{CC}$			2.3	4.5	mA
Input offset voltage	$V_{I(OFF)}$	$R_S < 10\text{k}\Omega$		2	6	mV
Input offset current	$I_{I(OFF)}$			5	200	nA
Input bias current	$I_{I(BIAS)}$			30	500	nA
Large signal voltage gain	$G_V$	$V_o(p-p) = \pm 10\text{V}$ , $R_L \leq 2\text{k}\Omega$	20	200		V/mV
Common Mode Input Voltage Range	$V_{I(COM)}$		$\pm 12$	$\pm 13$		V
Common Mode Rejection Ratio	$RR_{(COM)}$	$R_S \leq 10\text{k}\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$RR_{(VCC)}$	$R_S \leq 10\text{k}\Omega$	76	90		dB
Output Voltage swing	$V_{O(p-p)}$	$R_L \geq 10\text{k}\Omega$	$\pm 12$	$\pm 14$		V
Power Consumption	$P_C$			70	170	mV
Slew Rate	$SR$	$V_{IN} = \pm 10\text{V}$ , $R_L \geq 2\text{k}\Omega$ , $C_L \leq 100\text{pF}$	1.2	2.2		V/ $\mu$ s
Rise Time	$T_{RIS}$	$V_{IN} = \pm 20\text{mV}$ , $R_L \geq 2\text{k}\Omega$ , $C_L \leq 100\text{pF}$		0.3		$\mu$ s
Overshoot	$OS$	$V_{IN} = \pm 20\text{mV}$ , $R_L \geq 2\text{k}\Omega$ , $C_L \leq 100\text{pF}$		15		%
Input Resistance	$R_{IN}$		0.3	2		M $\Omega$
Output Resistance	$R_{OUT}$			75		$\Omega$
Total Harmonic Distortion	THD	$f = 1\text{kHz}$ , $Av = 20\text{dB}$ , $R_L = 2\text{k}\Omega$ , $V_{OUT} = 2\text{Vpp}$ , $C_L = 100\text{pF}$		0.008		%
Channel Separation	$V_{O1}/V_{O2}$			120		dB
<b>FREQUENCY CHARACTERISTIC</b>						
Unity Gain Bandwidth	BW		2.0	2.8		MHz

■ TYPICAL CHARACTERISTICS



### ■ TYPICAL CHARACTERISTICS(Cont.)



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