



## TL074

## LINEAR INTEGRATED CIRCUIT

### LOW NOISE QUAD J-FET OPERATIONAL AMPLIFIER

#### DESCRIPTION

The UTC **TL074** is a high speed J-FET input quad operational amplifier. It incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit. The device features high slew rates, low input bias and offset current and low offset voltage temperature coefficient.

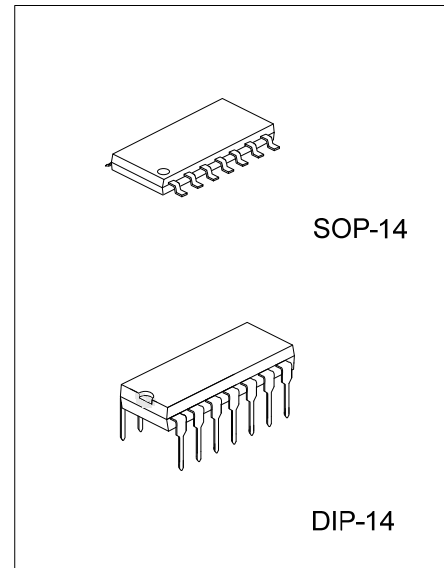
#### FEATURES

- \*Low power consumption
- \*Wide common-mode (up to  $V_{cc+}$ ) and differential voltage range
- \*Low input bias and offset current
- \*Low noise  $eN = 15nV / \sqrt{Hz}$ (typ)
- \*Output short-circuit protection
- \*High input impedance J-FET input stage
- \*Low harmonic distortion:0.01%(typ)
- \*Internal frequency compensation
- \*Latch up free operation
- \*High slewrate:13V/ $\mu$ s(typ)

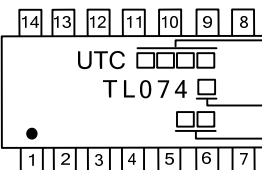
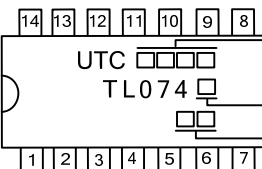
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
TL074L-D14-T	TL074G-D14-T	DIP-14	Tube
TL074L-S14-R	TL074G-S14-R	SOP-14	Tape Reel

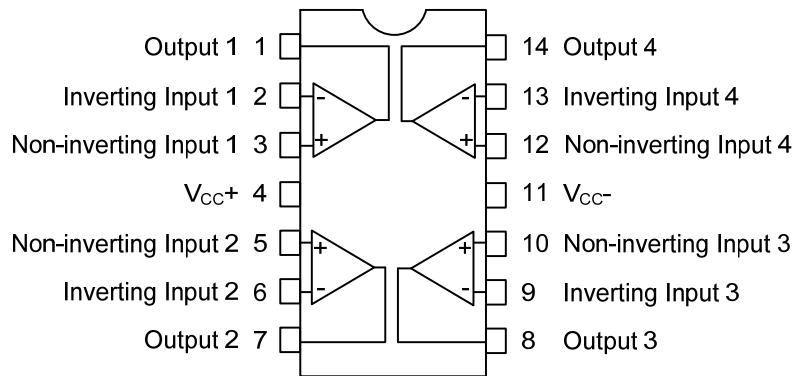
<p>TL074L-D14-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) T: Tube, R: Tape Reel (2) D14: DIP-14, S14: SOP-14 (3) G: Halogen Free, L: Lead Free</p>
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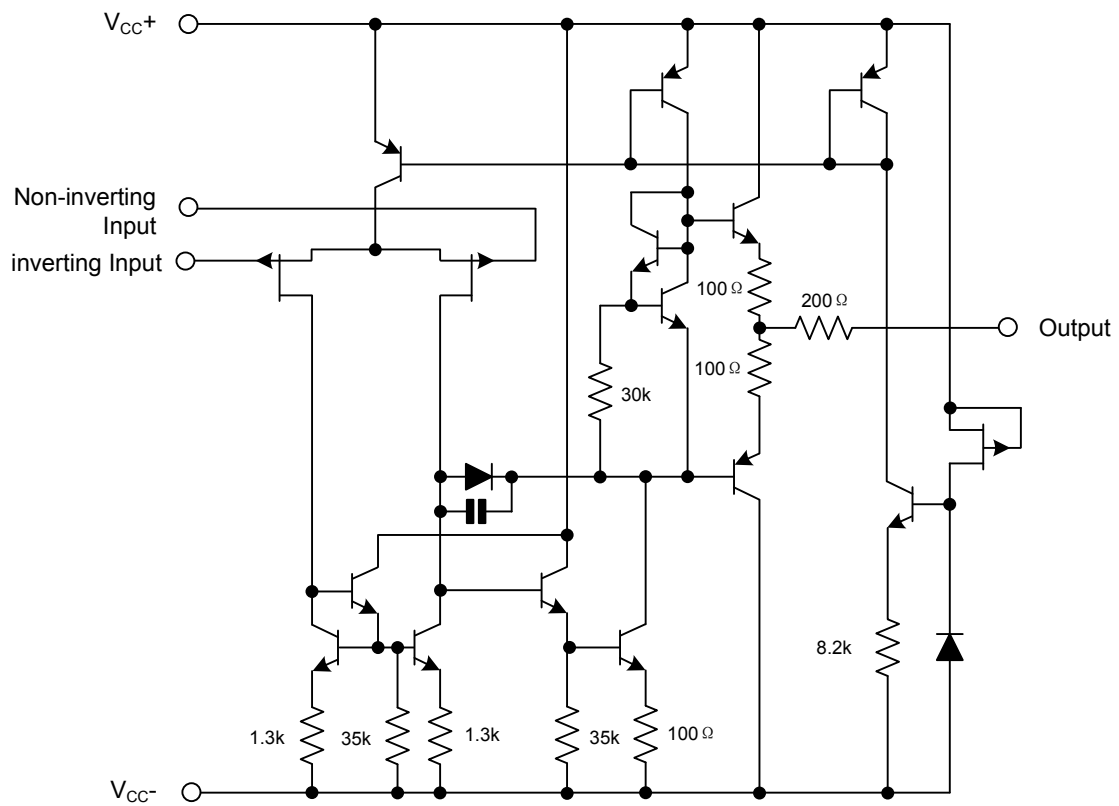
### MARKING INFORMATION

PACKAGE	MARKING
SOP-14	 <p>                     14 13 12 11 10 9 8 → Date Code                      UTC □□□□                      TL074 □                      □ □ → L: Lead Free                      □ □ → G: Halogen Free                      □ □ → Lot Code                      1 2 3 4 5 6 7                 </p>
DIP-14	 <p>                     14 13 12 11 10 9 8 → Date Code                      UTC □□□□                      TL074 □                      □ □ → L: Lead Free                      □ □ → G: Halogen Free                      □ □ → Lot Code                      1 2 3 4 5 6 7                 </p>

### PIN CONFIGURATIONS



■ SCHEMATIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage (Note 1)	V <sub>CC</sub>	±18	V
Input Voltage (Note 2)	V <sub>IN</sub>	±15	V
Differential Input Voltage (Note 3)	V <sub>I(DIFF)</sub>	±30	V
Power Dissipation	P <sub>D</sub>	680	mW
Output Short-Circuit Duration (Note 4)		Infinite	
Operating Temperature	T <sub>OPR</sub>	-20 ~ +85	°C
Storage Temperature	T <sub>STG</sub>	-65 ~ 150	°C

Notes: 1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V<sub>CC-</sub> and V<sub>CC+</sub>.

2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

### ■ ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub>=±15V, T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input Offset Voltage	V <sub>I(OFF)</sub>	R <sub>S</sub> =50Ω	T <sub>A</sub> =25°C		3	6	mV
			T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>			7	mV
Temperature Coefficient of Input Offset Voltage	ΔV <sub>I(OFF)</sub>	R <sub>S</sub> =50Ω		10		μV/°C	
Input Offset Current (Note)	I <sub>I(OFF)</sub>	T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>	T <sub>A</sub> =25°C		5	100	pA
						4	nA
Input Bias Current (Note)	I <sub>I(BIAS)</sub>	T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>	T <sub>A</sub> =25°C		20	200	pA
						20	nA
Input Common Mode Voltage	V <sub>I(CM)</sub>		±11	-12~+15		V	
Output Voltage Swing	V <sub>O(SW)</sub>	R <sub>L</sub> =2kΩ	T <sub>A</sub> =25°C	10	12		V
		R <sub>L</sub> =10kΩ		12	13.5		V
		R <sub>L</sub> =2kΩ	T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>	10			V
		R <sub>L</sub> =10kΩ		12			V
Large Signal Voltage Gain	G <sub>V</sub>	R <sub>L</sub> =10kΩ, V <sub>OUT</sub> =±10V	T <sub>A</sub> =25°C	50	200		V/mV
			T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>	25			V/mV
Gain Bandwidth Product	GB <sub>W</sub>	R <sub>L</sub> =10kΩ, C <sub>L</sub> =100pF	2	3		MHz	
Input Resistance	R <sub>IN</sub>			10 <sup>12</sup>		Ω	
Common Mode Rejection Ratio	CMR	R <sub>S</sub> =50Ω	T <sub>A</sub> =25°C	80	86		dB
			T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>	80			dB
Supply Voltage Rejection Ratio	SVR	R <sub>S</sub> =50Ω	T <sub>A</sub> =25°C	80	86		dB
			T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>	80			dB
Supply Current	I <sub>CC</sub>	No Load	T <sub>A</sub> =25°C		1.4	2.5	mA
			T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>			2.5	mA
Channel Separation	V <sub>O1</sub> /V <sub>O2</sub>	G <sub>V</sub> =100		120		dB	
Output Short-circuit Current	I <sub>O(SC)</sub>	T <sub>MIN</sub> ≤T <sub>A</sub> ≤T <sub>MAX</sub>	T <sub>A</sub> =25°C	10	40	60	mA
				10		60	mA
Slew Rate	SR	V <sub>IN</sub> =10V, R <sub>L</sub> =2kΩ, C <sub>L</sub> =100pF, unity gain	8	13		V/μs	
Rise Time	t <sub>R</sub>	V <sub>IN</sub> =20mV, R <sub>L</sub> =2kΩ, C <sub>L</sub> =100pF, unity gain		0.1		μs	
Overshoot Factor	K <sub>OV</sub>	V <sub>IN</sub> =20mV, R <sub>L</sub> =2kΩ, C <sub>L</sub> =100pF, unity gain		10		%	
Total Harmonic Distortion	THD	G <sub>V</sub> =20dB, f=1kHz, R <sub>L</sub> =2kΩ, C <sub>L</sub> =100pF, V <sub>OUT</sub> =2Vpp)		0.01		%	
Phase Margin				45		Deg.	
Equivalent Input Noise Voltage	e <sub>N</sub>	R <sub>S</sub> =100Ω, f=1KHz		15			

Note: The Input bias currents are junction leakage currents, which approximately double for every 10°C increase in the junction temperature.

■ PARAMETER MEASUREMENT INFORMATION

Figure 1. Voltage Follow

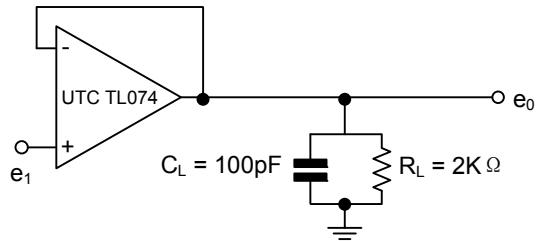
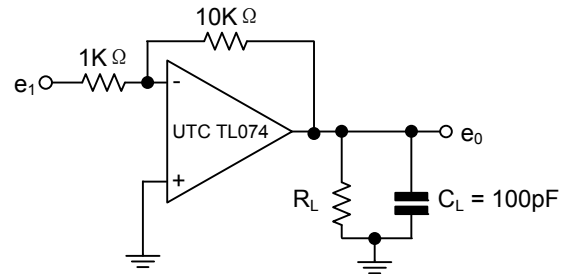
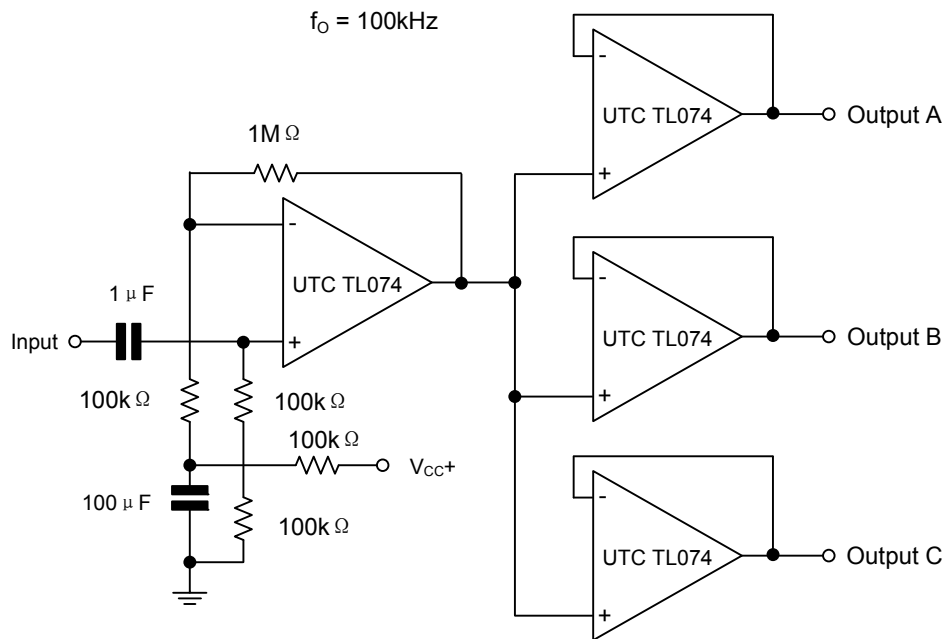


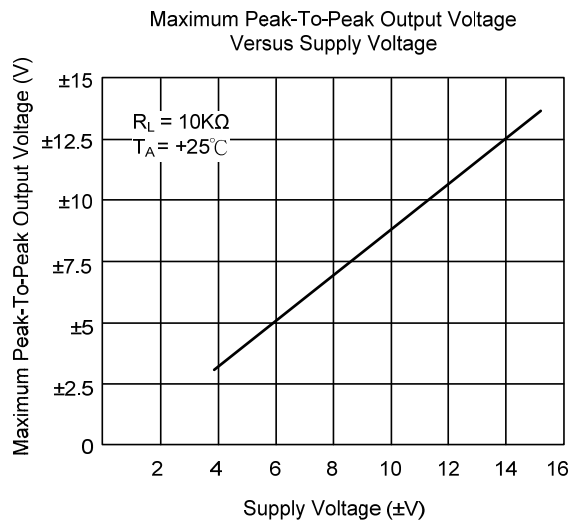
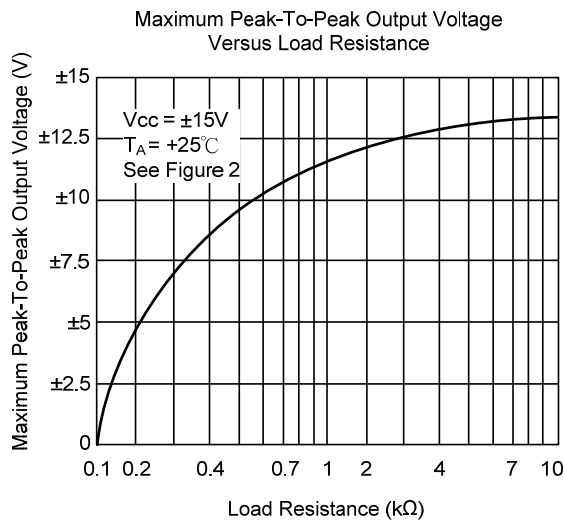
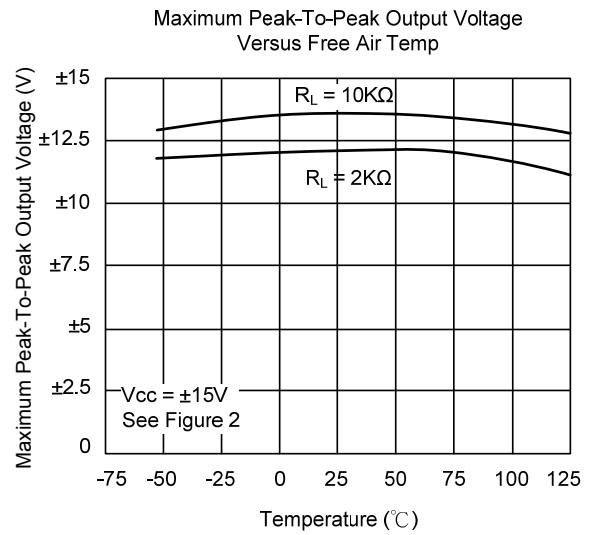
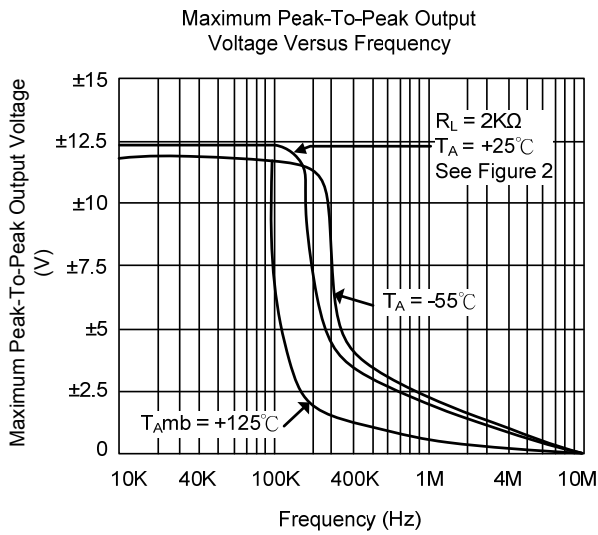
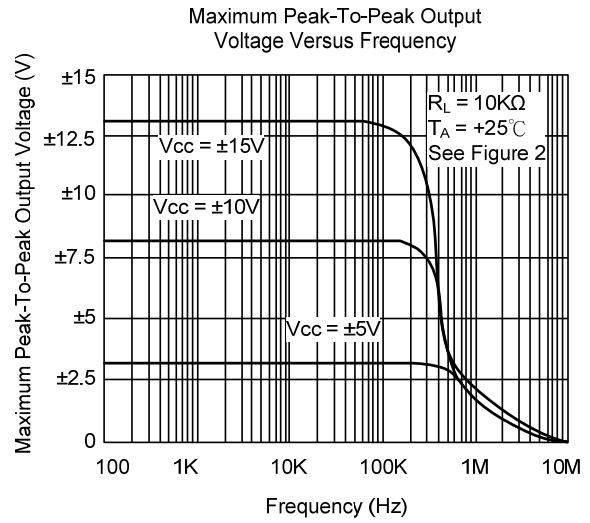
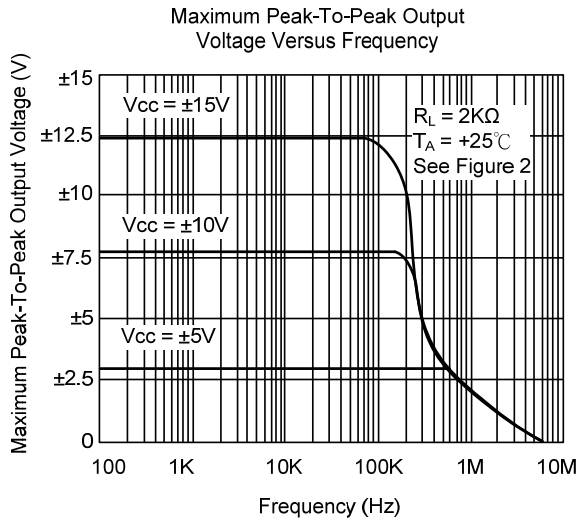
Figure 2. Gain-of-10 Inverting Amplifier



### ■ TYPICAL APPLICATION

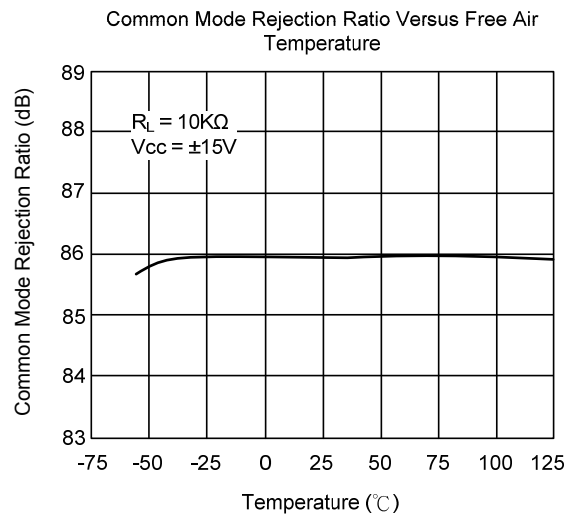
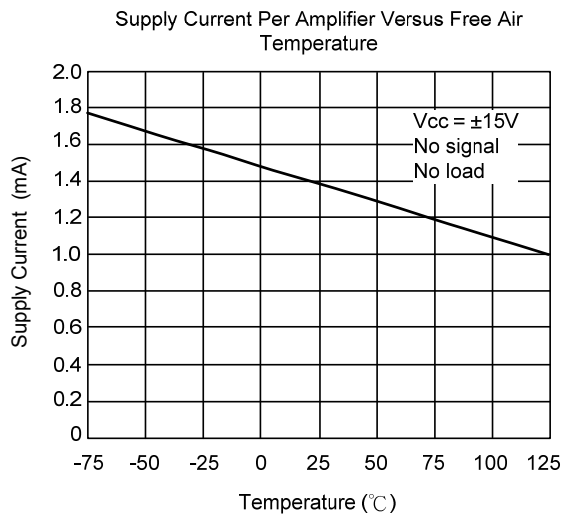
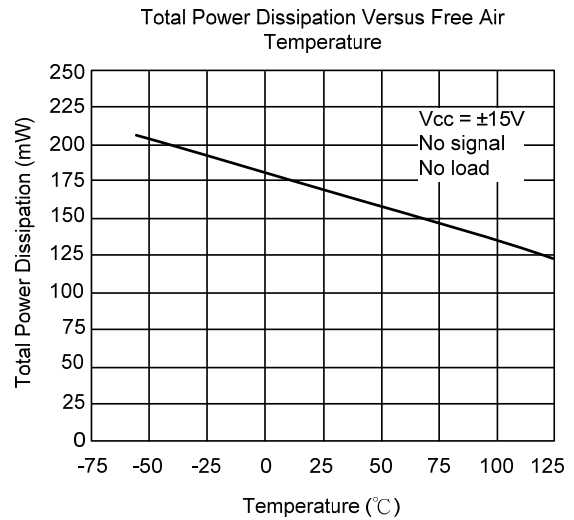
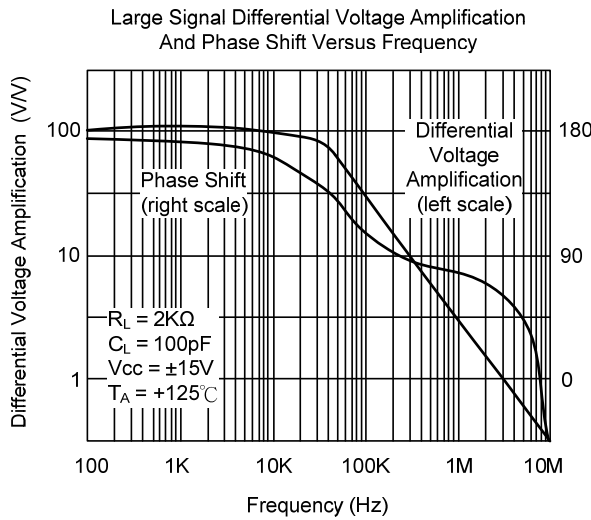
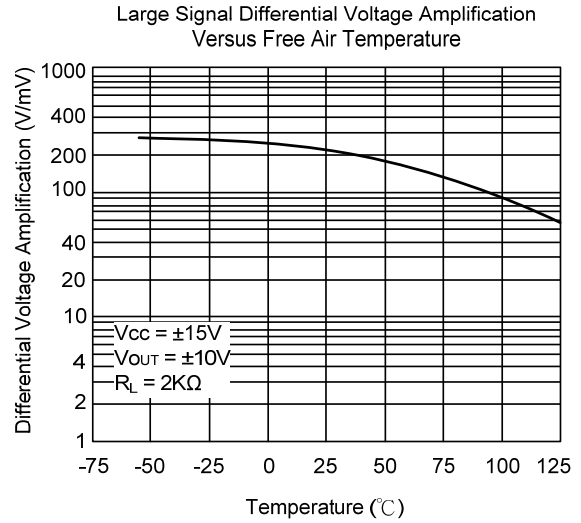
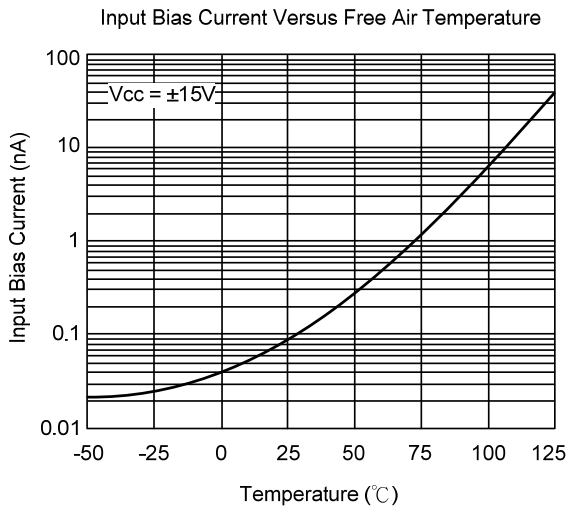


■ TYPICAL CHARACTERISTICS

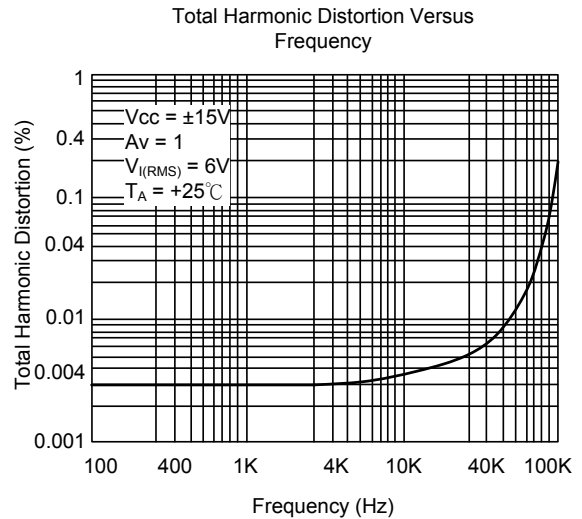
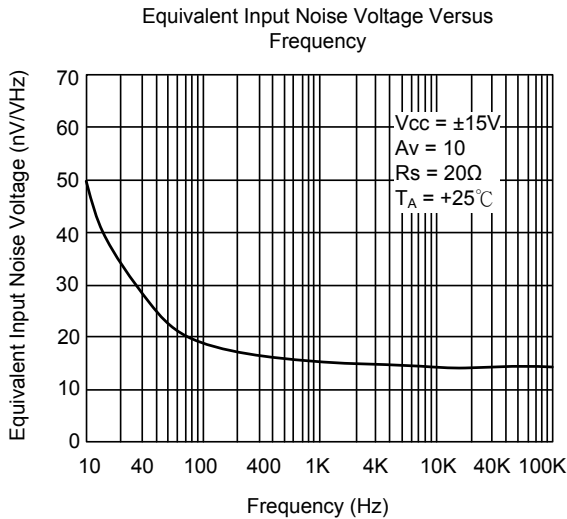
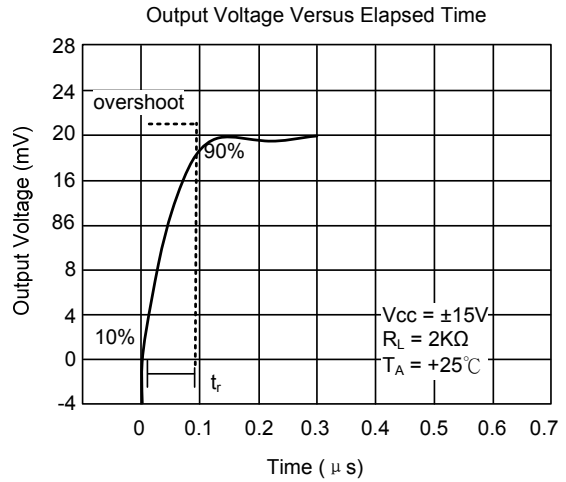
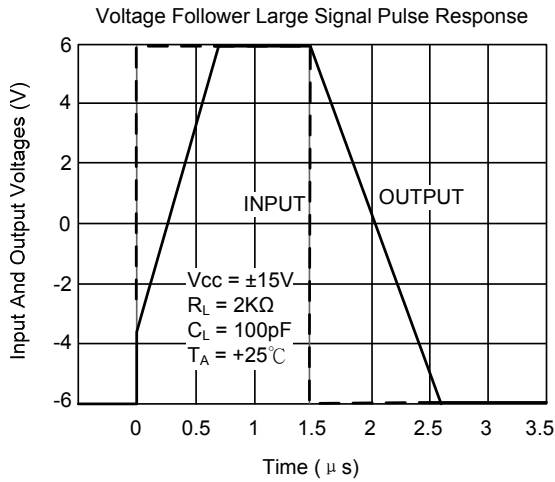




■ TYPICAL CHARACTERISTICS(Cont.)



■ TYPICAL CHARACTERISTICS(Cont.)



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