



U74HC244

CMOS IC

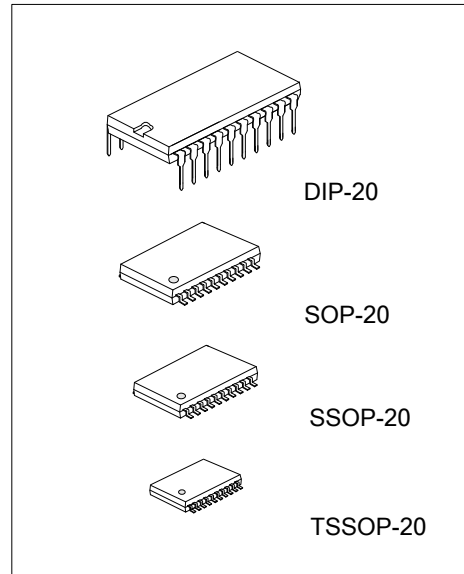
OCTAL BUFFER AND LINE DRIVER WITH 3-STATE OUTPUT

DESCRIPTION

The **U74HC244** are octal buffer and line drivers with non-inverting 3-state outputs. When \overline{nOE} is High, the outputs nQ will be in the high impedance.

FEATURES

- * Operation voltage range: 2 ~ 6V
- * 3-state output
- * Output Drive Capability: 15 LSTTL Loads

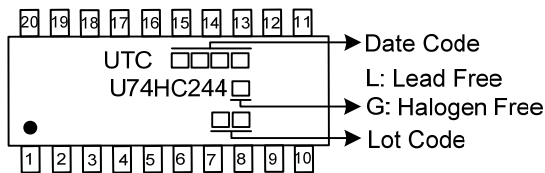


ORDERING INFORMATION

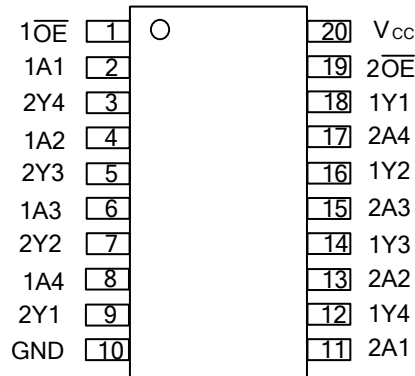
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC244L-D20-T	U74HC244G-D20-T	DIP-20	Tube
U74HC244L-S20-R	U74HC244G-S20-R	SOP-20	Tape Reel
U74HC244L-R20-R	U74HC244G-R20-R	SSOP-20	Tape Reel
U74HC244L-P20-R	U74HC244G-P20-R	TSSOP-20	Tape Reel

<p>U74HC244G-D20-T</p>	<p>(1) R: Tape Reel, T: Tube (2) D20: DIP-20, P20: TSSOP-20, R20: SSOP-20, S20: SOP-20 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



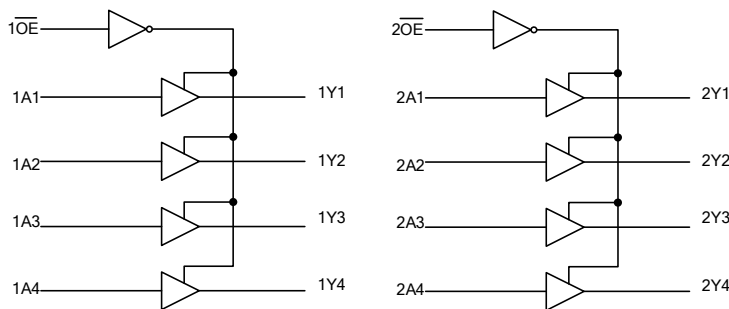
■ PIN CONFIGURATION



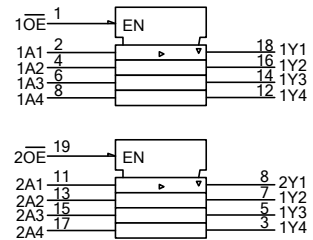
■ FUNCTION TABLE (each gate)

INPUT(nOE)	INPUT(nAn)	OUTPUT(nYn)
H	X	Z
L	H	H
L	L	L

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol

■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_{OUT}	±35	mA
V_{CC} or GND Current	I_{CC}	±70	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2		6	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Rise or Fall Times	t_R, t_F	$V_{CC}=2V$			1000	ns
		$V_{CC}=4.5V$			500	ns
		$V_{CC}=6V$			400	ns
Operating Temperature	T_A		-40		+125	°C

■ STATIC CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=2V$	1.5			V
		$V_{CC}=4.5V$	3.15			V
		$V_{CC}=6V$	4.2			V
Low-Level Input Voltage	V_{IL}	$V_{CC}=2V$			0.5	V
		$V_{CC}=4.5V$			1.35	V
		$V_{CC}=6V$			1.8	V
High-Level Output Voltage	V_{OH}	$V_{CC}=2V, I_{OH}=-20\mu\text{A}$	1.9	1.998		V
		$V_{CC}=4.5V, I_{OH}=-20\mu\text{A}$	4.4	4.499		V
		$V_{CC}=6V, I_{OH}=-20\mu\text{A}$	5.9	5.999		V
		$V_{CC}=4.5V, I_{OH}=-6\text{mA}$	3.98	4.3		V
		$V_{CC}=6V, I_{OH}=-7.8\text{mA}$	5.48	5.8		V
Low-Level Output Voltage	V_{OL}	$V_{CC}=2V, I_{OL}=20\mu\text{A}$		0.002	0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu\text{A}$		0.001	0.1	V
		$V_{CC}=6V, I_{OL}=20\mu\text{A}$		0.001	0.1	V
		$V_{CC}=4.5V, I_{OL}=6\text{mA}$		0.17	0.26	V
		$V_{CC}=6V, I_{OL}=7.8\text{mA}$		0.15	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6V, V_{IN}=V_{CC}$ or 0			±100	nA
Output OFF-State Current	I_{OZ}	$V_{CC}=6V, V_{OUT}=V_{CC}$ or 0, $V_{IN}=V_{IH}$ or V_{IL}			±0.5	μA
Quiescent Supply Current	I_Q	$V_{CC}=6V, V_{IN}=V_{CC}$ or 0, $I_{OUT}=0$			8	μA
Input Capacitance	C_{IN}	$V_{CC}=2V\sim 6V$		3	10	pF

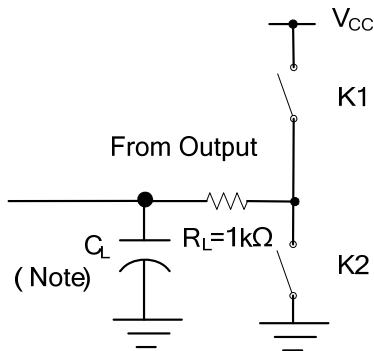
■ DYNAMIC CHARACTERISTICS (Input: $t_R, t_F=6ns$ $T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH} / t_{PHL}	$V_{CC}=2V, C_L=50pF$		40	115	ns
		$V_{CC}=2V, C_L=150pF$		56	165	ns
		$V_{CC}=4.5V, C_L=50pF$		13	23	ns
		$V_{CC}=4.5V, C_L=150pF$		18	33	ns
		$V_{CC}=6V, C_L=50pF$		11	20	ns
		$V_{CC}=6V, C_L=150pF$		15	28	ns
3-state output enable time $n\overline{OE}$ to nYn	t_{PZH} / t_{PZL}	$V_{CC}=2V, C_L=50pF$		75	150	ns
		$V_{CC}=2V, C_L=150pF$		100	200	ns
		$V_{CC}=4.5V, C_L=50pF$		15	30	ns
		$V_{CC}=4.5V, C_L=150pF$		20	40	ns
		$V_{CC}=6V, C_L=50pF$		13	26	ns
		$V_{CC}=6V, C_L=150pF$		17	34	ns
3-state output disable time $n\overline{OE}$ to nYn	t_{PHZ} / t_{PLZ}	$V_{CC}=2V, C_L=50pF$		75	150	ns
		$V_{CC}=4.5V, C_L=50pF$		15	30	ns
		$V_{CC}=6V, C_L=50pF$		13	26	ns

■ OPERATING CHARACTERISTICS

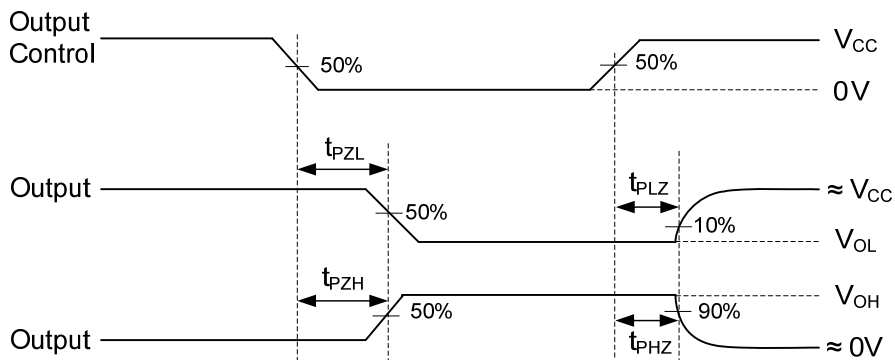
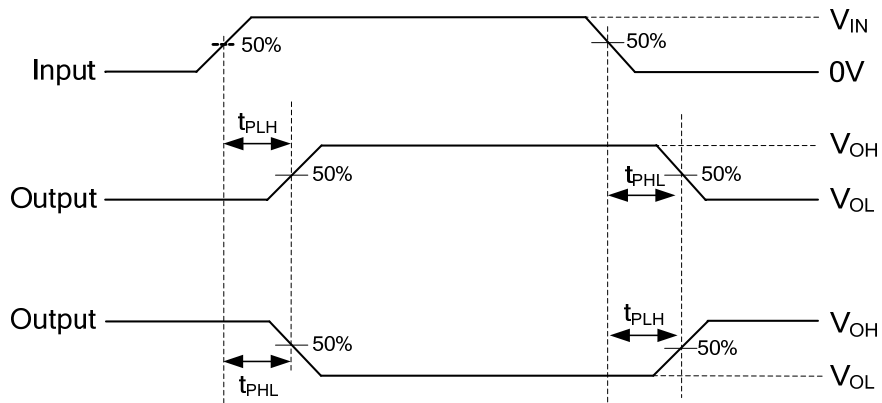
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		35		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

Note: C_L includes probe and jig capacitance.



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