



U74HC373

CMOS IC

OCTAL D-TYPE TRANSPARENT LATCH

DESCRIPTION

The **U74HC373** consists of eight D-type transparent latches with 3-state outputs. When latched enable (LE) is high, the latches operate at the transparent mode, and the latches' output will change

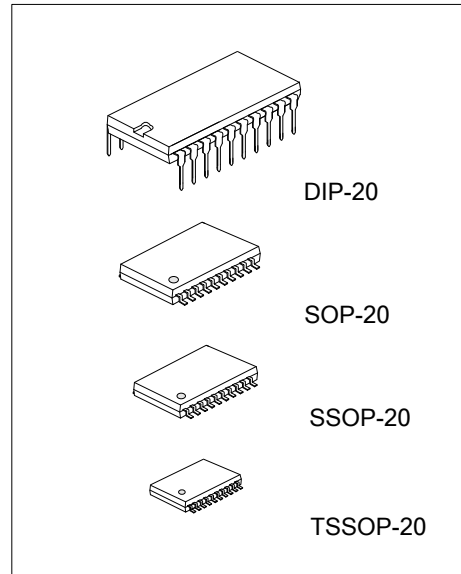
corresponding with the data present at D0 to D7. When output enable (\overline{OE}) is low, the contents of the latches will be present at the outputs. The outputs will be in the high impedance when \overline{OE} goes high.

FEATURES

- * Operation Voltage Range: 2~6V
- * Drive Up to 15 LSTTL Loads
- * 3-State Outputs
- * Output Capability Suitable for Bus Driving

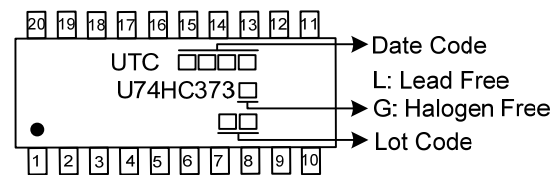
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC373L-D20-T	U74HC373G-D20-T	DIP-20	Tube
U74HC373L-S20-R	U74HC373G-S20-R	SOP-20	Tape Reel
U74HC373L-R20-R	U74HC373G-R20-R	SSOP-20	Tape Reel
U74HC373L-P20-R	U74HC373G-P20-R	TSSOP-20	Tape Reel

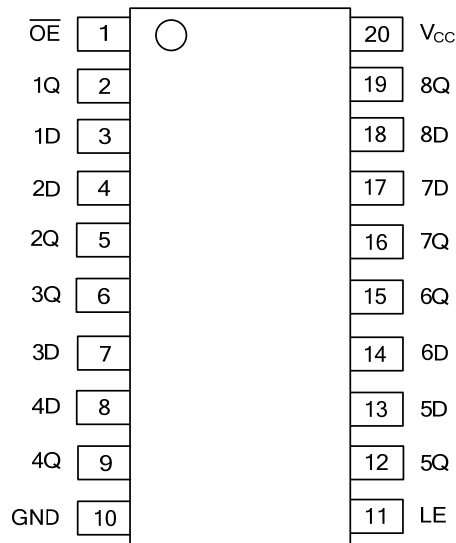


<p>U74HC373G-D20-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel, T: Tube</p> <p>(2) D20: DIP-20, P20: TSSOP-20, R20: SSOP-20, S20: SOP-20</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION

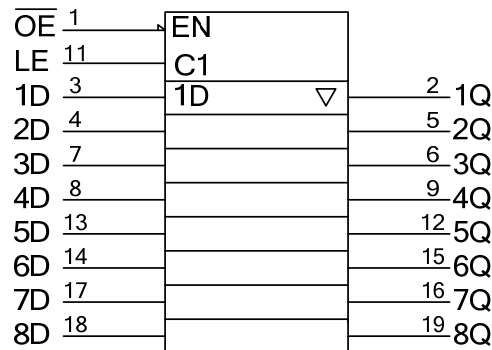


■ FUNCTION TABLE

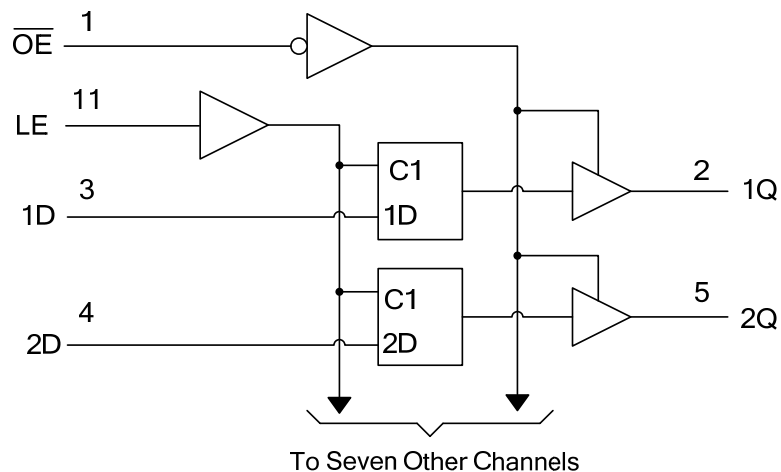
INPUTS(OE)	INPUTS(LE)	INPUTS(D)	OUTPUT(Q)
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ 7	V
V _{CC} or GND Current	I _{CC}	±70	mA
Output Current	I _{OUT}	±35	mA
Input Clamp Current	I _{IK}	±20	mA
Output Clamp Current	I _{OK}	±20	mA
Operating Temperature	T _{OPR}	-40 ~ + 85	°C
Storage Temperature	T _{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-20	θ _{JA}	°C/W
	SOP-20		
	SSOP-20		
	TSSOP-20		

■ RECOMMENDED OPERATING CONDITIONS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		2	5	6	V
High-level Input Voltage	V _{IH}	V _{CC} =2.0V	1.5			V
		V _{CC} =4.5V	3.15			
		V _{CC} =6.0V	4.2			
Low-level Input Voltage	V _{IL}	V _{CC} =2.0V	0		0.5	V
		V _{CC} =4.5V	0		1.35	
		V _{CC} =6.0V	0		1.8	
Input Voltage	V _{IN}		0		V _{CC}	V
Output Voltage	V _{OUT}	High or low state	0		V _{CC}	V
Input Rise or Fall Times	t _R , t _F	V _{CC} =2.0V			1	µs
		V _{CC} =4.5V			0.5	
		V _{CC} =6.0V			0.4	

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V _{OH}	V _{CC} =2.0V	1.9	1.998		V
		V _{CC} =4.5V	4.4	4.499		
		V _{CC} =6.0V	5.9	5.999		
		V _{CC} =4.5V, I _{OH} =-20µA, V _{IN} =V _{IH} or V _{IL}	3.98	4.3		
		V _{CC} =6.0V, I _{OH} =-7.8mA, V _{IN} =V _{IH} or V _{IL}	5.48	5.8		
Output Voltage Low-Level	V _{OL}	V _{CC} =2.0V		2	100	mV
		V _{CC} =4.5V		1	100	
		V _{CC} =6.0V		1	100	
		V _{CC} =4.5V, I _{OL} =6mA, V _{IN} =V _{IH} or V _{IL}		170	260	
		V _{CC} =6.0V, I _{OL} =7.8mA, V _{IN} =V _{IH} or V _{IL}		150	260	
Input Leakage Current	I _{I(LEAK)}	V _{CC} =6.0V, V _{IN} =V _{CC} or 0		±0.1	±100	nA
Disable Output Leakage Current	I _{OZ}	V _{CC} =6.0V, V _{OUT} =V _{CC} or 0		±0.01	±0.5	µA
Quiescent Supply Current	I _Q	V _{CC} =6.0V, V _{IN} =V _{CC} or 0, I _{OUT} =0			8	µA
Input Capacitance	C _{IN}	V _{CC} =2.0V~6.0V		3	10	pF

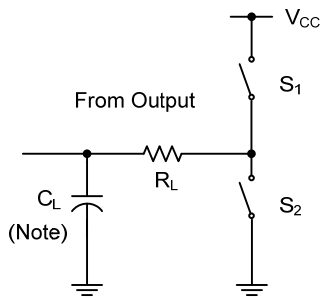
■ SWITCHING CHARACTERISTICS (see test circuit and waveforms)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Propagation delay from input (D) to output (Q)	t_{PLH}/t_{PHL}	$V_{CC}=2.0V$	50pF		58	150	ns	
		$V_{CC}=4.5V$			15	30		
		$V_{CC}=6.0V$			13	26		
		$V_{CC}=2.0V$		150pF		82		200
		$V_{CC}=4.5V$				22		40
		$V_{CC}=6.0V$				19		34
Propagation delay from input (LE) to output (Q)		$V_{CC}=2.0V$	50pF		73	175		ns
					18	35		
					15	30		
			150pF		100	225		
					24	45		
					20	38		
Output enable time from input (\overline{OE}) to output (Q)	t_{PZL}/t_{PZH}	$V_{CC}=2.0V$	50pF		65	150	ns	
		$V_{CC}=4.5V$			17	30		
		$V_{CC}=6.0V$			14	26		
		150pF	$V_{CC}=2.0V$		90	200		
			$V_{CC}=4.5V$		23	40		
			$V_{CC}=6.0V$		19	34		
Output disable time from input (\overline{OE}) to output (Q)	t_{PLZ}/t_{PHZ}	$V_{CC}=2.0V$	50pF		50	150	ns	
		$V_{CC}=4.5V$			15	30		
		$V_{CC}=6.0V$			13	26		
to Q	t_r	$V_{CC}=2.0V$	150pF		28	60	ns	
		$V_{CC}=4.5V$			8	12		
		$V_{CC}=6.0V$			6	10		
Pulse Width	t_w	$V_{CC}=2.0V$		80		ns		
		$V_{CC}=4.5V$		16				
		$V_{CC}=6.0V$		14				
Setup Time	t_{SU}	$V_{CC}=2.0V$		50		ns		
		$V_{CC}=4.5V$		10				
		$V_{CC}=6.0V$		9				
Hold Time	t_H	$V_{CC}=2.0V$		20		ns		
		$V_{CC}=4.5V$		10				
		$V_{CC}=6.0V$		10				

■ OPERATING CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

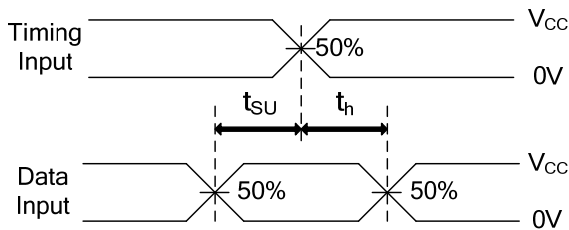
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No Load		100		pF

■ TEST CIRCUIT AND WAVEFORMS

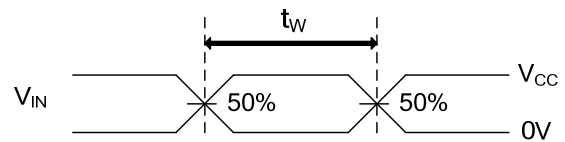


TEST CIRCUIT

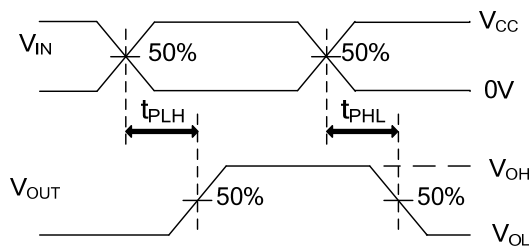
	R_L	C_L	S_1	S_2
t_{PZH}	1k Ω	50pF,	Open	Closed
t_{PZL}		150pF	Closed	Open
t_{PHZ}	1k Ω	50pF	Open	Closed
t_{PLZ}		150pF	Closed	Open
t_{PHL}	-	50pF,	Open	Open
t_{PLH}		150pF		



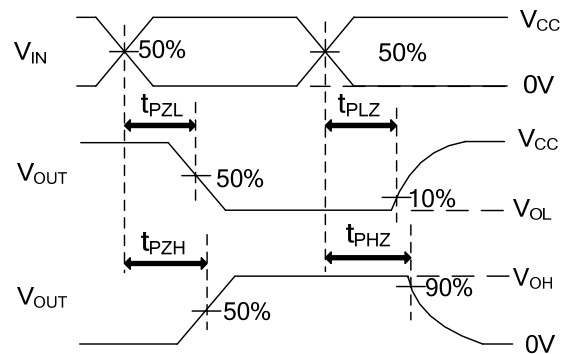
SETUP TIME AND HOLD TIME



PULSE WIDTH



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: C_L includes probe and jig capacitance.
 $PRR \leq 1\text{MHz}$, $Z_o = 50\Omega$, $t_R = 6\text{ns}$, $t_F = 6\text{ns}$

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