



## U74HC4060

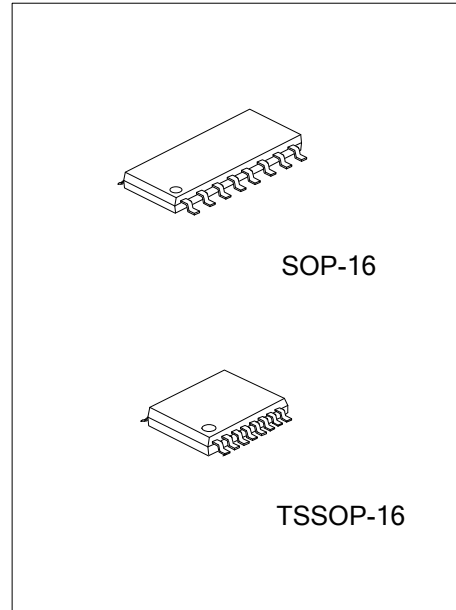
CMOS IC

### 14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

#### DESCRIPTION

The **U74HC4060** are high-speed Si-gate CMOS device.

The **U74HC4060** devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits with three oscillator terminals (CLKI,  $\overline{\text{CLKO}}$ , CLKO) , ten buffered outputs ( $Q_D$  to  $Q_J$  and  $Q_L$  to  $Q_M$ ) and an overriding asynchronous master reset (CLR) . The oscillator may be replaced by an external clock signal at input CLKI. In this case keep the other oscillator pins ( $\overline{\text{CLKO}}$ , CLKO) floating. The counter advances on the negative-going transition of CLKI. A high level at the clear (CLR) input disables the oscillator and resets the counter to zero (all Q output low).



#### FEATURES

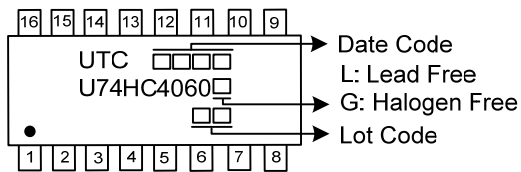
- \* Operate from 2.0V to 6.0V
- \* Low Input Current:1.0uA
- \* Outputs Can Drive Up To 10 LSTTL Loads
- \* Low Power Consumption ,80uA Max  $I_{CC}$
- \* 4mA Output Drive at 5V
- \* Typical  $t_{PD}$ =14ns
- \* Allow Design of Either RC or Crystal Oscillator Circuits

#### ORDERING INFORMATION

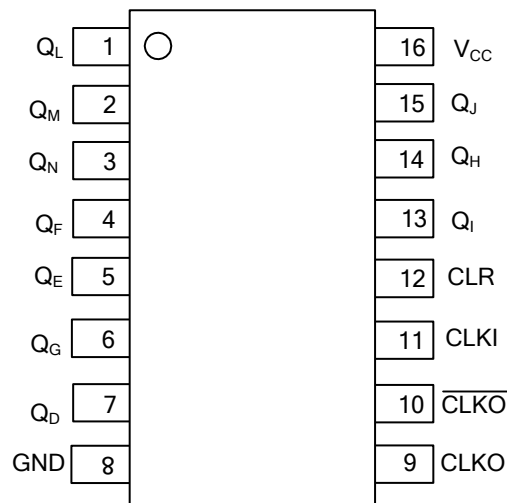
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC4060L-S16-R	U74HC4060G-S16-R	SOP-16	Tape Reel
U74HC4060L-P16-R	U74HC4060G-P16-R	TSSOP-16	Tape Reel

<p>U74HC4060G-S16-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S16: SOP-16, P16: TSSOP-16</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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## MARKING



## PIN CONFIGURATION

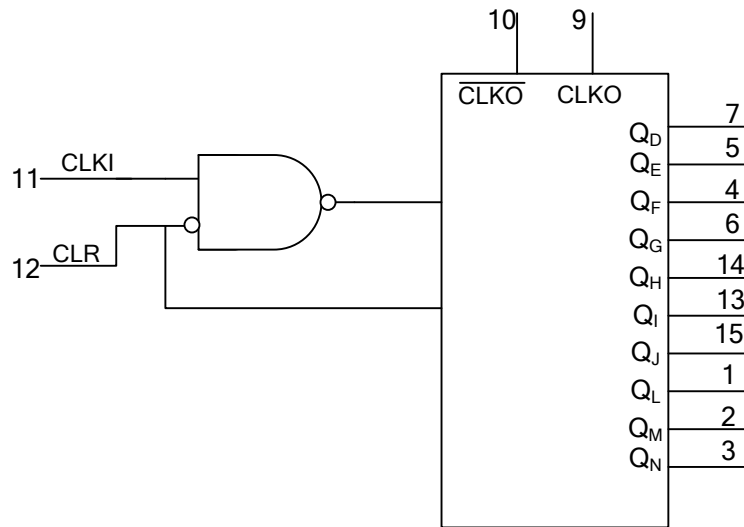


## FUNCTION TABLE

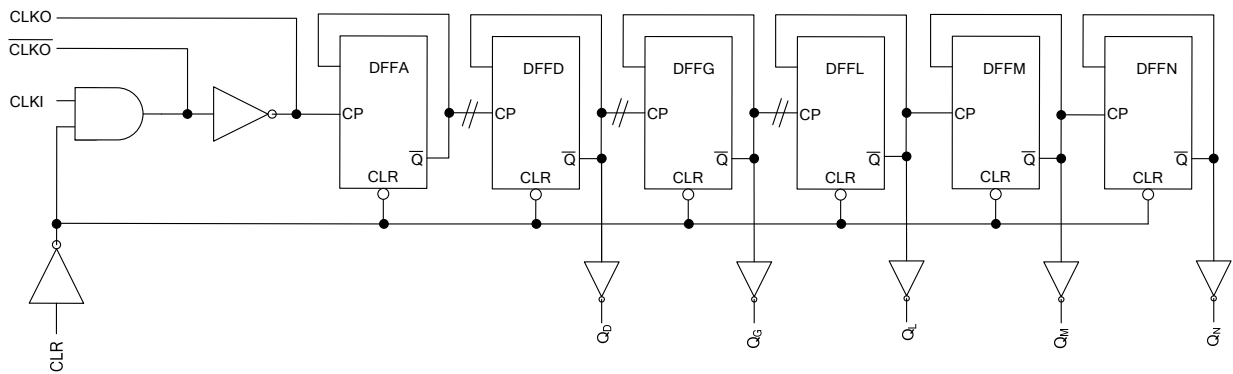
INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

Note: H: HIGH voltage level  
 L: LOW voltage level  
 X: Don't care. High impedance OFF-state  
 ↑: Low-to-High CP transition  
 ↓: High-to-Low CP transition

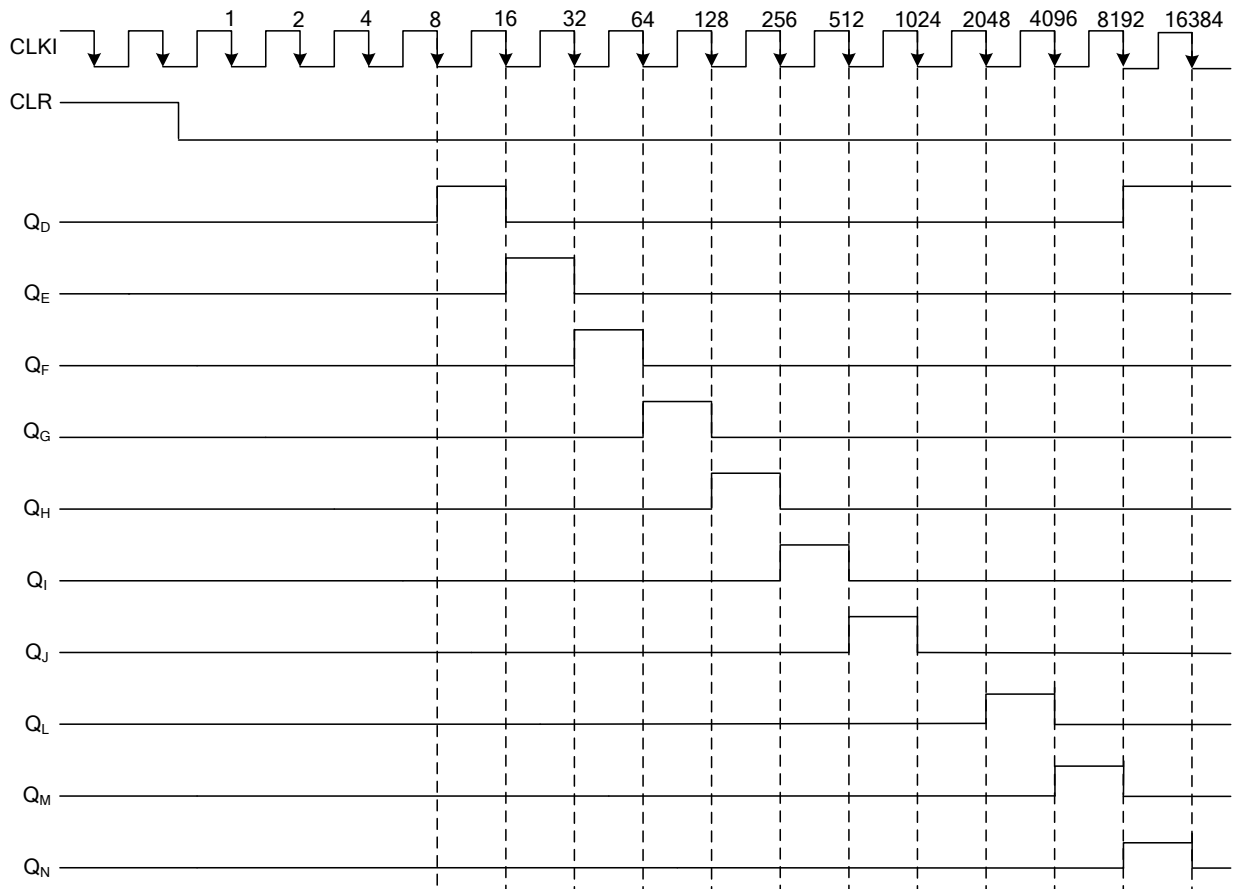
■ LOGIC SYMBOL



■ LOGIC DIAGRAM



## ■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-0.5 ~ 7.0	V
Input Clamp Current ( $V_I < 0$ or $V_I > V_{CC}$ )	$I_{IK}$	±20	mA
Output Clamp Current ( $V_O < 0$ or $V_O > V_{CC}$ )	$I_{OK}$	±20	mA
$V_{CC}$ or GND Current	$I_{CC}$	±50	mA
Continuous Output Current ( $V_O = 0$ to $V_{CC}$ )	$I_{OUT}$	±25	mA
Storage Temperature	$T_{STG}$	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$	Operating	2.0		6.0	V
Input Voltage	$V_{IN}$		0		$V_{CC}$	V
Output Voltage	$V_{OUT}$		0		$V_{CC}$	V
Input Rise or Fall Times	$t_R, t_F$	$V_{CC}=2.0V$			1000	ns
		$V_{CC}=4.5V$			500	ns
		$V_{CC}=6.0V$			400	ns
Operating Temperature	$T_A$		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	$V_{IH}$	$V_{CC}=2V$	1.5			V
		$V_{CC}=4.5V$	3.15			V
		$V_{CC}=6V$	4.2			V
Low-Level Input Voltage	$V_{IL}$	$V_{CC}=2V$			0.5	V
		$V_{CC}=4.5V$			1.35	V
		$V_{CC}=6V$			1.8	V
High-Level Output Voltage	$V_{OH}$	$V_{CC}=2V, I_{OH}=-20\mu A$	1.9	1.998		V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.499		V
		$V_{CC}=6V, I_{OH}=-20\mu A$	5.9	5.999		V
		$V_{CC}=4.5V, I_{OH}=-4.0mA$	3.98	4.3		V
		$V_{CC}=6V, I_{OH}=-5.2mA$	5.48	5.8		V
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=2V, I_{OL}=20\mu A$		0.002	0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=6V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=4.5V, I_{OL}=4mA$		0.17	0.26	V
		$V_{CC}=6V, I_{OL}=5.2mA$		0.15	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6V, V_{IN}=V_{CC}$ or GND			±100	nA
Quiescent Supply Current	$I_{CC}$	$V_{CC}=6V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			8	μA

## ■ TIMING REQUIREMENTS

(over recommended operating free-air temperature range, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	$f_{\text{clock}}$	$V_{\text{CC}}=2\text{V}$			4.3	MHz
		$V_{\text{CC}}=4.5\text{V}$			22	MHz
		$V_{\text{CC}}=6\text{V}$			25	MHz
Pulse Duration	$C_{\text{LKl}}$ high or low	$V_{\text{CC}}=2\text{V}$	115			ns
		$V_{\text{CC}}=4.5\text{V}$	23			ns
		$V_{\text{CC}}=6\text{V}$	20			ns
	$C_{\text{LR}}$ high	$V_{\text{CC}}=2\text{V}$	115			ns
		$V_{\text{CC}}=4.5\text{V}$	23			ns
		$V_{\text{CC}}=6\text{V}$	20			ns
Setup time, $C_{\text{LR}}$ Inactive Before $C_{\text{LKl}}$ High To Low	$t_{\text{su}}$	$V_{\text{CC}}=2\text{V}$	200			ns
		$V_{\text{CC}}=4.5\text{V}$	40			ns
		$V_{\text{CC}}=6\text{V}$	34			ns

## ■ SWITCHING CHARACTERISTICS

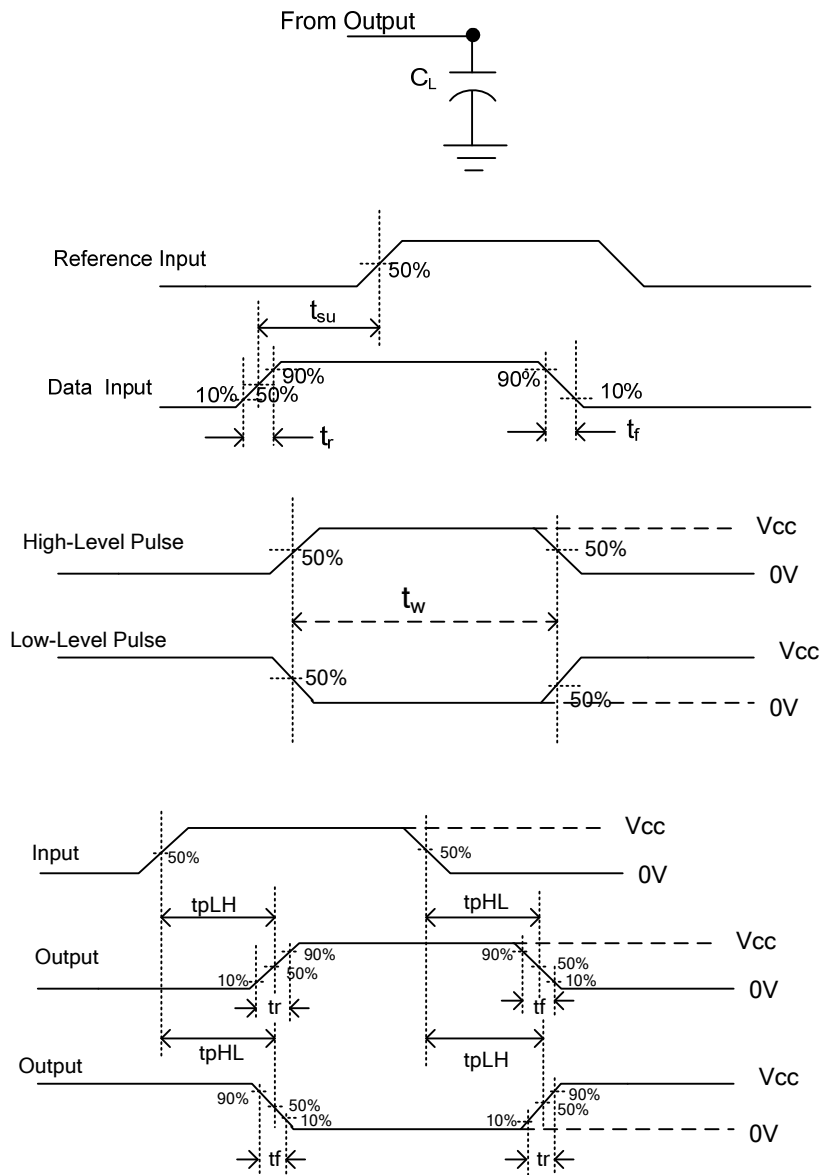
(over recommended operating free-air temperature range,  $C_{\text{L}}=50\text{pF}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Clock Pulse Frequency	$f_{\text{MAX}}$	$V_{\text{CC}}=2\text{V}$	4.3			MHz
		$V_{\text{CC}}=4.5\text{V}$	22			MHz
		$V_{\text{CC}}=6\text{V}$	25			MHz
Propagation delay from CLKI to $Q_{\text{D}}$	$t_{\text{PD}}$	$V_{\text{CC}}=2\text{V}$			615	ns
		$V_{\text{CC}}=4.5\text{V}$			123	ns
		$V_{\text{CC}}=6\text{V}$			105	ns
Propagation delay from CLR to Any Q	$t_{\text{PHL}}$	$V_{\text{CC}}=2\text{V}$			175	ns
		$V_{\text{CC}}=4.5\text{V}$			35	ns
		$V_{\text{CC}}=6\text{V}$			30	ns
Output rise or fall time	$t_{\text{t}}$	$V_{\text{CC}}=2\text{V}$			95	ns
		$V_{\text{CC}}=4.5\text{V}$			19	ns
		$V_{\text{CC}}=6\text{V}$			16	ns

## ■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	$C_{\text{PD}}$	No load		88		pF

## ■ TEST CIRCUIT AND WAVEFORMS



Note: A.  $C_L = 50\text{pF}$ ,  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics : PRR  $\leq 1\text{MHz}$ ,  $Z_o = 50\Omega$ ,  $t_r \leq 6\text{ns}$ ,  $t_f \leq 6\text{ns}$ .

C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

D.  $t_{pLH}$  and  $t_{pHL}$  are the same as  $t_{pd}$ .

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