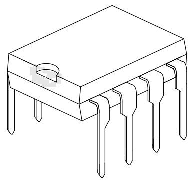
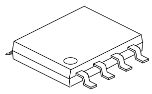
HIGH-PERFORMANCE CURRENT-MODE PWM CONTROLLERS



DIP-8



SOP-8

■ DESCRIPTION

The UTC **UC2843B** provides off-line or DC-DC fixed-frequency current-mode control design with minimum external components. Internally-implemented circuits include an under-voltage lockout (UVLO) and a precision reference with accuracy at the error amplifier input. The UTC **UC2843B** also contain internal circuits which include a pulse width modulation (PWM) comparator providing current-limit control, logic ensuring latched operation, and a totem-pole output stage designed to source or sink high-peak current. The output stage is low when it is in off-state condition and suitable for N-channel MOSFETs driving.

The UTC **UC2843B** also has following advantages: the start-up current lower than 0.5mA while the oscillator discharge current is specified to 8.3mA (Typ.). In UVLO conditions, the output has a maximum saturation voltage of 1.2V when sinking 10mA @ V_{CC} = 5V.

The typical UVLO threshold of the UTC **UC2843B** is 8.4V (on) and 7.6V (off) and can operate to duty cycles approximately 100%.

■ FEATURES

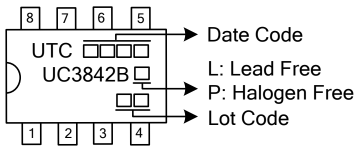
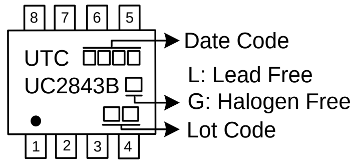
* Current mode operation:500 kHz
* Low start-up current value<0.5mA
* Latching PWM for cycle-by-cycle current limiting
* Trimmed oscillator discharge current
* Automatic feed-forward compensation
* Internally trimmed reference with UVLO
* High-current totem-pole output UVLO with hysteresis
* Double-pulse suppression

■ ORDERING INFORMATION

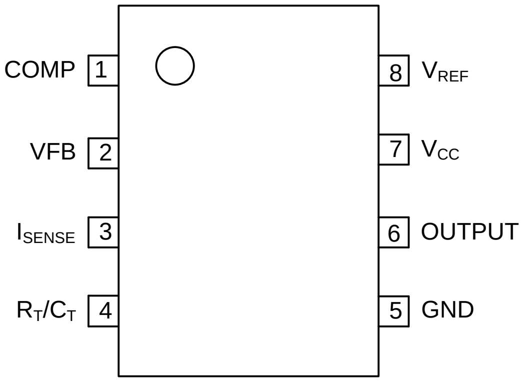
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC2843BL-D08-T	UC2843BG-D08-T	DIP-8	Tube
UC2843BL-S08-T	UC2843BG-S08-T	SOP-8	Tube
UC2843BL-S08-R	UC2843BG-S08-R	SOP-8	Tape Reel

UC2843BG-S08-R	
(1)Packing Type	(1) T: Tube, R: Tape Reel
(2)Package Type	(2) D08: DIP-8, S08: SOP-8
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

DIP-8	SOP-8
	

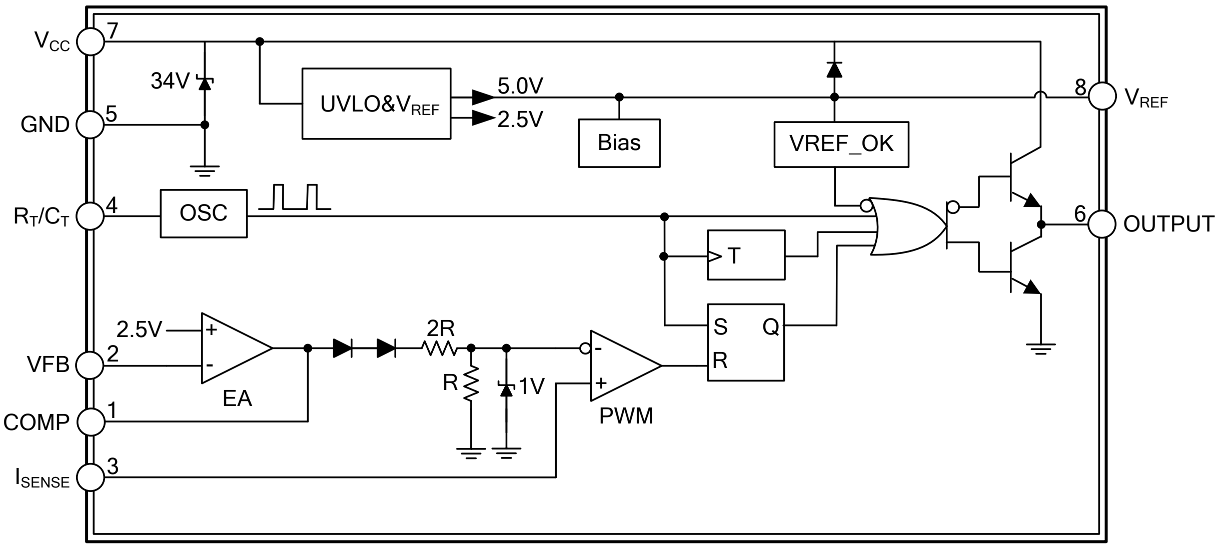
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	VFB	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{REF} and capacitor C_T to ground. Operation to 500 kHz is possible.
5	GND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{REF}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage (Low impedance source)		V_{CC}	30	V
Analog Input Voltage (V_{FB} and I_{SENSE})		V_{IN}	-0.3~+6.3	V
Supply Current		I_{CC}	30	mA
Error Amplifier Output Sink Current		$I_{O(SINK)}$	10	mA
Output Current		I_{OUT}	±1	A
Power Dissipation	SOP-8	P_D	800	mW
	DIP-8		1250	
Output Energy (Capacitive load)		W	5	μJ
Junction Temperature		T_J	150	°C
Operating Temperature		T_{OPR}	-40~+85	°C
Storage Temperature		T_{STG}	-65~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. All voltages are concerning the device GND terminal.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Thermal Resistance Junction to Ambient	SOP-8	θ_{JA}	156	°C/W
	DIP-8		100	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}			30	V
Input Voltage	R_T/C_T	V_{IN}	0		5.5	V
	VFB and I_{SENSE}		0		5.5	V
Output Voltage (OUTPUT)		V_{OUT}	0		30	V
Supply Current, Externally Limited		I_{CC}			25	mA
Output Current		I_{OUT}			200	mA
Reference Output Current		$I_{O(REF)}$			-20	mA
Oscillator Frequency		f_{OSC}		100	500	kHz
Operating Temperature		T_A	-40		+85	°C

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=15V, R_T =10kΩ, C_T=3.3nF, T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	I_{OUT} =1mA, T_J =25°C	4.95	5	5.05	V
Line Regulation	ΔV_{OUT}	V_{CC} = 12V~25V		6	20	mV
Load Regulation	ΔV_{OUT}	I_{OUT} = 1mA~20mA		6	25	mV
Average Temperature Coefficient Of Output Voltage	T_S			0.2	0.4	mV/°C
Total Output Variation	V_{REF}	V_{CC} =12V~25V, I_{OUT} =1mA~20mA	4.9		5.1	V
Output Noise Voltage	e_N	f = 10Hz~10kHz, T_J =25°C		50		μV
Long Term Stability		T_J=25°C For 1000 hours		5	25	mV
Output Short Circuit Current	I_{SC}		-30	-100	-180	mA

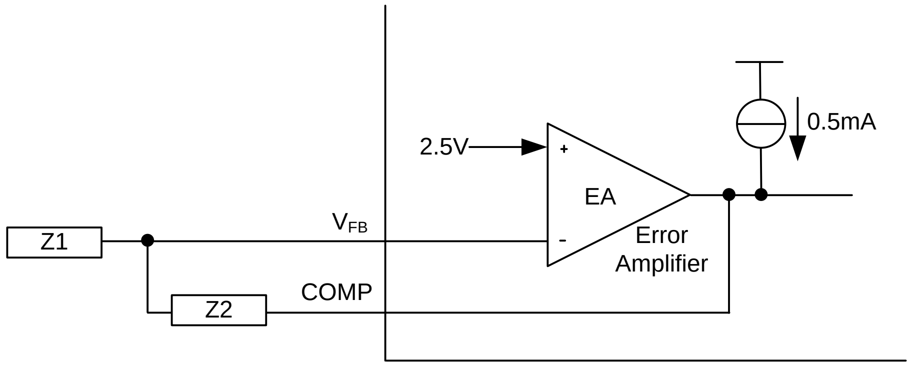
■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR SECTION						
Frequency	f_{OSC}	T_J =25°C, R_T =62kΩ, C_T =1nF, Min =225 kHz, Max =275 kHz	49	52	55	kHz
		T_J = Full range	48		56	kHz
Frequency Change with Voltage	$\Delta f_{OSC}/\Delta V$	V_{CC} = 12V ~ 25V		0.2	1	%
Frequency Change with Temperature	$\Delta f_{OSC}/\Delta T$	T_J = Full range		5		%
Oscillator Voltage Swing	V_{OSC}	Peak to peak		1.7		V
Discharge Current	I_{DISC}	T_J =25°C, R_T/C_T =2V	7.8	8.3	8.8	mA
		R_T/C_T =2V	7.5		8.8	mA
ERROR-AMPLIFIER SECTION						
Voltage Feedback Input	V_{FB}	COMP =2.5V	2.45	2.5	2.55	V
Input Bias Current	$I_{I(BIAS)}$			-0.3	-1	μA
Open Loop Voltage Gain	G_{VO}	V_{OUT} =2V~4V	65	90		dB
Unity Gain Bandwidth	G_{BW}		0.7	1		MHz
Power Supply Rejection Ratio	PSRR	V_{CC} =12V~25V	60	70		dB
Output Sink Current	I_{SINK}	V_{FB} =2.7V, COMP=1.1V	2	6		mA
Output Source Current	I_{SOURCE}	V_{FB} =2.3V, COMP =5V	-0.5	-0.8		mA
Output Voltage Swing High State	V_{OH}	V_{FB} =2.3V, R_L =15kΩ to GND	5	6		V
	V_{OL}	V_{FB} =2.7V, R_L =15kΩ to GND		0.7	1.1	V
CURRENT-SENSE SECTION						
Current Sense Input Voltage Gain	G_V	(Note 2,3)	2.85	3	3.15	V/V
Maximum Current Sense Input Threshold	V_{TH}	COMP =5V (Note 2)	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	V_{CC} =12V~25V (Note 2)		70		dB
Input Bias Current	$I_{I(BIAS)}$			-2	-10	μA
Propagation Delay	t_D	V_{FB} =0V~2V		150	300	ns
OUTPUT SECTION						
High-Level Output Voltage	V_{OH}	I_{OH} =-20mA	13	13.5		V
		I_{OH} =-200mA	12	13.5		V
Low-Level Output Voltage	V_{OL}	I_{OL} =20mA		0.1	0.4	V
		I_{OL} =200mA		1.5	2.2	V
Under-Voltage Lockout Output Voltage	V_{UVLO}	V_{CC} =5V, I_{OL}=1mA		0.7	1.2	V
Output Voltage Rise Time	t_R	C_L =1nF, T_J = 25°C		50	150	ns
Output Voltage Fall Time	t_F	C_L =1nF, T_J = 25°C		50	150	ns
UNDERVOLTAGE-LOCKOUT SECTION						
Startup Threshold	V_{TH}		7.8	8.4	9	V
Minimum Operating Voltage After Start-Up	$V_{CC(MIN)}$		7	7.6	8.2	V
PULSE-WIDTH MODULATOR SECTION						
Maximum Duty Cycle	$D_{C(MAX)}$		94	96	100	%
Minimum Duty Cycle	$D_{C(MIN)}$				0	%
SUPPLY VOLTAGE						
Power Startup Supply Current	$I_{CC}+I_C$			0.3	0.5	mA
Power Operating Supply Current	$I_{CC}+I_C$	V_{FB} and I_{SENSE} at 0V		11	17	mA
Power Supply Zener Voltage	V_Z	I_{CC} =25mA	30	34		V

Notes: 1. Adjust V_{CC} above the start threshold before setting it to 15V.
2. Measured at the trip point of the latch, with VFB at 0V.
3. Measured between I_{SENSE} and COMP, with the input changing from 0V ~ 0.8V.

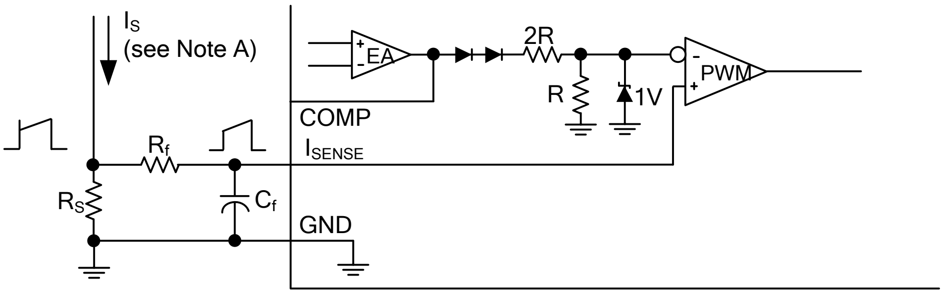
■ APPLICATION INFORMATION

Error amplifier (EA) configuration circuit:



Note: Error amplifier can source or sink up to 0.5mA.

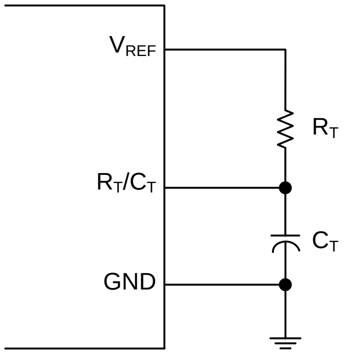
Current-sense circuit:



Notes: 1. Peak current (I_S) is determined by the formula: $I_{S(max)} = 1V/R_S$

2. A small RC filter formed by resistor R_F and capacitor C_F may be required to suppress switch transients.

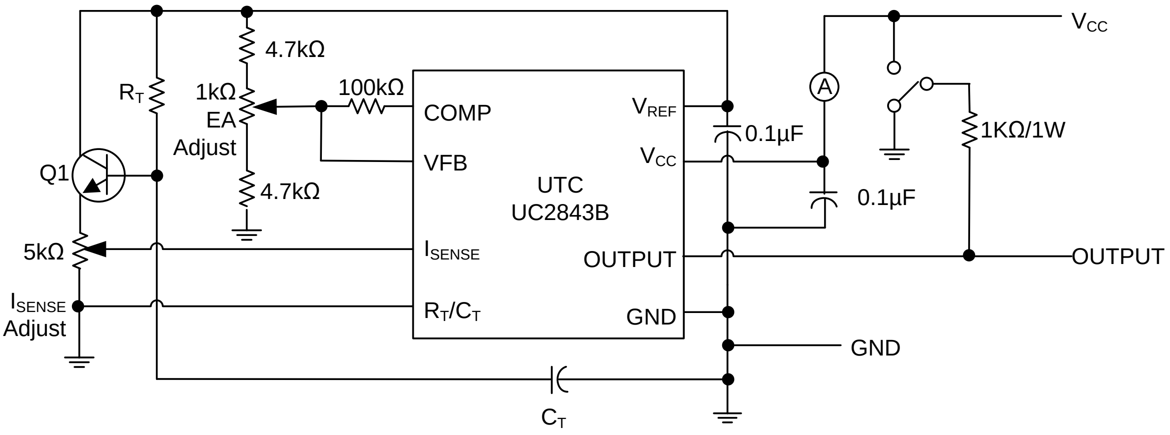
The oscillator frequency is set using the circuit:



■ APPLICATION INFORMATION (Cont.)

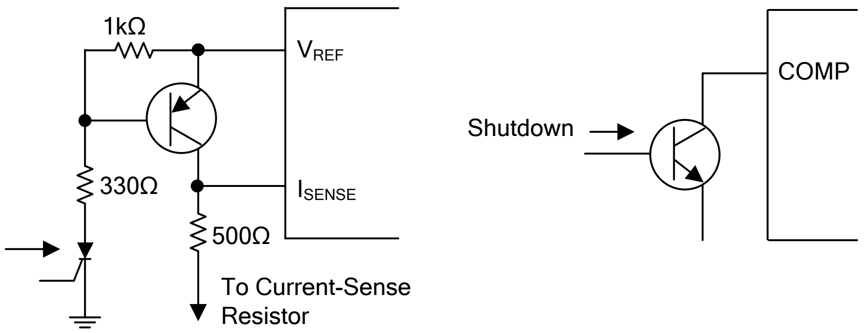
Open-Loop Laboratory Test Fixture

In the open-loop laboratory test fixture, high peak currents and loads need grounding techniques. The transistor and 5-kΩ potentiometer sample the oscillator waveform, applying an adjustable ramp to the I_{SENSE} terminal. Timing and bypass capacitors should be connected closely to the GND terminal in a single-point ground.



Shutdown Technique

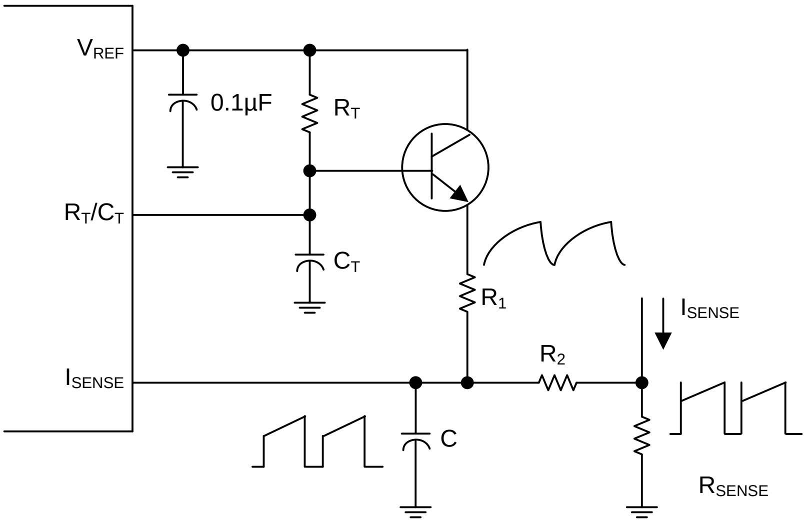
The PWM controller can be shut down through two methods: the one is raising voltage (above 1 V) at I_{SENSE}, the other is pulling the COMP terminal below a voltage two diode drops above ground. Either method can leave the output of the PWM comparator high (refer to block diagram). To reset the PWM latch is dominant so the output can stay low in the case of the next clock cycle is coming and the COMP or I_{SENSE} terminal is removed beyond this shutdown condition. For example, an externally-latched shutdown can be accomplished by adding an SCR reset by cycling V_{CC} below the lower UVLO threshold. So the reference turns off then allows the SCR to reset at this condition.



■ APPLICATION INFORMATION (Cont.)

Shutdown Technique (cont.)

A fraction of the triangular-wave oscillator can be summed resistively with the current-sense signal providing slope compensation for converters, which requiring duty cycles over 50%. Please note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.



■ TYPICAL CHARACTERISTICS