# UC3842A/3843A

## LINEAR INTEGRATED CIRCUIT

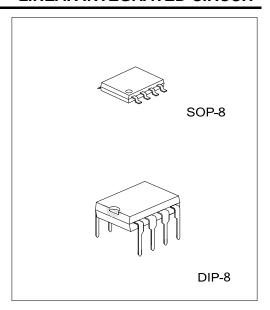
# CURRENT MODE PWM CONTROL CIRCUITS

## ■ DESCRIPTION

The UTC **UC3842A/3843A** provide the necessary functions to implement off-line or DC to DC fixed frequency current mode , controlled switching circuits with minimal external components.

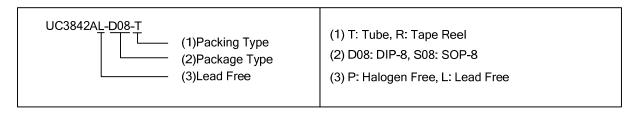
## **■** FEATURES

- \*Low Start Up Current (Typical 0.12mA)
- \*Automatic Feed Forward Compensation
- \*Pulse-by-Pulse Current Limiting
- \*Under-voltage Lockout with Hysteresis
- \*Double Pulse Suppression
- \*High Current Totem Pole Output to Drive MOSFET Directly
- \*Internally Trimmed Band Gap Reference
- \*500kHz Operation



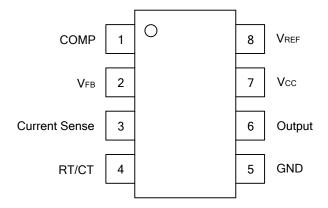
## **■ ORDERING INFORMATION**

Ordering	Number	Daakaga	Packing	
Lead Free	Halogen Free	Package		
UC3842AL-D08-T	UC3842AP-D08-T	DIP-8	Tube	
UC3842AL-S08-R	UC3842AP-S08-R	SOP-8	Tape Reel	
UC3842AL-S08-T	UC3842AP-S08-T	SOP-8	Tube	
UC3843AL-D08-T	UC3843AP-D08-T	DIP-8	Tube	
UC3843AL-S08-R	UC3843AP-S08-R	SOP-8	Tape Reel	
UC3843AL-S08-T	UC3843AP-S08-T	SOP-8	Tube	

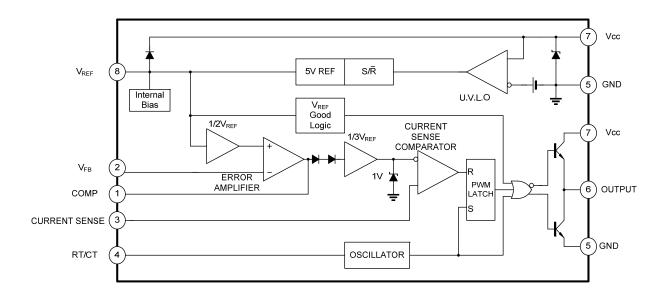


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## **■ PIN CONFIGURATION**



## **■ BLOCK DIAGRAM**



## ■ ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage(Low Impedance Source)		V <sub>CC</sub>	30	V
Supply Voltage(I <sub>CC</sub> <30mA)		V <sub>CC</sub>	Self Limiting	V
Analog Inputs (Pin 2,3)		$V_{I(ANA)}$	-0.3 ~ +6.3	V
Output Current (Peak )		I <sub>O(PEAK)</sub>	±1	А
Error Amplifier Output Sink Current		I <sub>SINK(EA)</sub>	10	mA
Output Energy (Capacity Load)			5	μJ
Power Dissipation( T <sub>A</sub> ≦25°C)	DIP-8		1250	\/
Fower Dissipation ( TA \( \frac{1}{2} \)	SOP-8	P <sub>D</sub>	800	mW
Derated at T <sub>A</sub> >25℃			8	mW/℃
Junction Temperature		TJ	+150	$^{\circ}$
Storage Temperature		T <sub>STG</sub>	-65 ~ <b>+</b> 150	$^{\circ}$

Note Absolute maximum ratings are those values beyond which the device which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ ELECTRICAL CHARACTERISTICS

 $(0^{\circ}C \leq T_A \leq 70^{\circ}C, V_{CC}=15V, R_T=10k\Omega, C_T=3.3nF, unless otherwise specified)$ 

REFERENCE SECTION           Output Voltage $V_{REF}$ $T_J$ =25°C, $I_{OUT}$ =1mA         4.9         5         5.1         N           Line Regulation $\Delta V_{REF}$ $12 \le V_{IN}25V$ 6         20         m           Load Regulation $\Delta V_{REF}$ $1 \le I_{OUT}$ =20mA         6         25         m           Temperature Stability         (Note 1)         0.2         0.4         mV           Total Output Variation         Line, Load, Temp (Note 1)         4.82         5.18         N           Output Noise Voltage         Vosc $10Hz \le f \le 10kHz$ , $T_J$ =25°C (Note 1)         50         µ           Long Term Stability $T_A$ =25°C, 1000Hrs (Note 1)         5         2.5         m           Output Short Circuit $I_{SC}$ -30         -100         -180         m           OSCILLATOR SECTION           Initial Accuracy         f $T_J$ =25°C         47         52         57         kt           Voltage Stability $\Delta f/\Delta V_{CC}$ $12 \le V_{CC} \le 25V$ 0.2         1         9           Amplitude $V_{OSC}$ $V_{PINA}$ = 2.5V         2.42         2.50         2.58         N	$(0.0 \le 1.4 \le 1.0.0)$ , ACC-12A, KL-10	K12, C†−3.3HI	, unless otherwise specified)				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line Regulation $\Delta V_{REF}$ $12 \le V_{IN}25V$ 620mLoad Regulation $\Delta V_{REF}$ $1 \le I_{OUT} = 20mA$ 625mTemperature Stability(Note 1)0.20.4mVTotal Output VariationLine, Load, Temp (Note 1)4.825.18VOutput Noise Voltage $V_{OSC}$ $10Hz \le f \le 10kHz$ , $T_J = 25 °C$ (Note 1)50 $\mu$ Long Term Stability $T_A = 25 °C$ , 1000Hrs (Note 1)525mOSCILLATOR SECTIONInitial Accuracyf $T_J = 25 °C$ 475257kHVoltage Stability $\Delta f/\Delta V_{CC}$ $12 \le V_{CC} \le 25V$ 0.219Temperature Stability $T_{MIN} \le T_A \le T_{MAX}$ (Note 1)59Amplitude $V_{OSC}$ $V_{PIN4}$ peak to peak1.71ERROR AMPLIFIER SECTIONInput Voltage $V_{I(EA)}$ $V_{PIN1} = 2.5V$ 2.422.502.58NInput Bias Current $I_{I(BIAS)}$ $-0.3$ -2 $\mu$ AVOL $2V \le V_{OUT} \le 4V$ 6090dUnity Gain Bandwidth $T_J = 25 °C$ (Note 1)0.71MIPSRR $I_2 \le V_{CC} \le 25V$ 6070dOutput Sink Current $I_{O(SINK)}$ $V_{PIN2} = 2.3V, V_{PIN1} = 5V$ -0.5-0.8mVout High $V_{OH}$ $V_{PIN2} = 2.3V, V_{PIN1} = 5V$ -0.5-0.8m	REFERENCE SECTION						
Load Regulation $\Delta V_{REF}$ 1 ≤ I <sub>OUT</sub> =20mA 6 25 m Temperature Stability (Note 1) 0.2 0.4 mV Total Output Variation Line, Load, Temp (Note 1) 4.82 5.18 V Total Output Noise Voltage $V_{OSC}$ 10Hz ≤ f ≤ 10kHz, T <sub>J</sub> =25°C (Note 1) 50 $\mu$ Coutput Short Circuit I <sub>SC</sub> -30 -100 -180 m OSCILLATOR SECTION Initial Accuracy f T <sub>J</sub> =25°C $V_{OUT}$ 12 ≤ $V_{CC}$ ≤ 25V 0.2 1 9 Temperature Stability $V_{OSC}$ 12 ≤ $V_{CC}$ ≤ 25V 0.2 1 9 Temperature Stability $V_{OSC}$ 12 ≤ $V_{CC}$ ≤ 25V 0.2 1 9 Temperature Stability $V_{OSC}$ 12 ≤ $V_{CC}$ 2.50 2.58 $V_{CC}$ 1.70 Minute $V_{CC}$ 2.70 Minute $V_{CC}$ 3.70 Minute $V_{CC}$ 3.7	Output Voltage	$V_{REF}$	T <sub>J</sub> =25℃,I <sub>OUT</sub> =1mA	4.9	5	5.1	V
Temperature Stability (Note 1) 0.2 0.4 mV Total Output Variation Line, Load, Temp (Note 1) 4.82 5.18 V Output Noise Voltage $V_{OSC}$ 10Hz $\leq$ f $\leq$ 10kHz, T, =25°C (Note 1) 50 $\mu$ Long Term Stability T <sub>A</sub> =25°C, 1000Hrs (Note 1) 5 25 m Output Short Circuit I <sub>SC</sub> -30 -100 -180 m OSCILLATOR SECTION Initial Accuracy f T <sub>J</sub> =25°C 47 52 57 kH Voltage Stability $\Delta$ f/ $\Delta$ V <sub>CC</sub> 12 $\leq$ V <sub>CC</sub> $\leq$ 25V 0.2 1 $\leq$ 9 Yoltage Stability Temperature Stability $V_{OSC}$ V <sub>PIN4</sub> peak to peak 1.7 $V_{OSC}$ V <sub>PIN4</sub> peak to peak 1.7 $V_{OSC}$ V <sub>PIN4</sub> peak to peak 1.7 $V_{OSC}$ V <sub>PIN5</sub> $V_{OSC}$ V <sub>PIN6</sub> $V_{OSC}$ V <sub>PIN7</sub> $V_{OSC}$ V <sub>PIN7</sub> $V_{OSC}$ V <sub>PIN8</sub> $V_{OSC}$ V <sub>PIN9</sub> $V_{OSC}$ V <sub>OSC</sub> V <sub>OSC</sub> $V_{OSC}$ V <sub>OSC</sub> V <sub>OSC</sub> $V_{OSC}$ V <sub>OSC</sub> V <sub>OSC</sub> V <sub>OSC</sub> $V_{OSC}$ V <sub>OSC</sub>	Line Regulation	$\Delta V_{REF}$	$12 \! \leq \! V_{IN}25V$		6	20	mV
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Load Regulation	$\Delta V_{REF}$	$1 \le I_{OUT}$ =20mA		6	25	mV
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Temperature Stability		(Note 1)		0.2	0.4	mV/℃
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Total Output Variation		Line, Load, Temp (Note 1)	4.82		5.18	V
Output Short Circuit $I_{SC}$ -30-100-180mOSCILLATOR SECTIONInitial Accuracyf $T_J=25^{\circ}C$ 475257kHVoltage Stability $\Delta f/\Delta V_{CC}$ $12 \le V_{CC} \le 25V$ 0.219Temperature Stability $T_{MIN} \le T_A \le T_{MAX}$ (Note 1)59Amplitude $V_{OSC}$ $V_{PIN4}$ peak to peak1.71ERROR AMPLIFIER SECTIONInput Voltage $V_{I(EA)}$ $V_{PIN1}=2.5V$ 2.422.502.58\mathred{N}Input Bias Current $I_{I(BIAS)}$ -0.3-2 $\mu$ AVOL $2V \le V_{OUT} \le 4V$ 6090dUnity Gain Bandwidth $T_J=25^{\circ}C$ (Note 1)0.71MIPSRR $I_2 \le V_{CC} \le 25V$ 6070dOutput Sink Current $I_{O(SINK)}$ $V_{PIN2}=2.7V, V_{PIN1}=1.1V$ 26mOutput Source Current $I_{O(SOURCE)}$ $V_{PIN2}=2.3V, V_{PIN1}=5V$ -0.5-0.8m $V_{OUT}$ High $V_{OH}$ $V_{PIN2}=2.3V, R_L=15k\Omega$ to GND56\mathred{N}	Output Noise Voltage	Vosc	10Hz≦f≦10kHz,T <sub>J</sub> =25°C (Note 1)		50		μV
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Long Term Stability		T <sub>A</sub> =25℃,1000Hrs (Note 1)		5	25	mV
Initial Accuracy	Output Short Circuit	I <sub>SC</sub>		-30	-100	-180	mA
Voltage Stability $\Delta f/\Delta V_{CC}$ $12 \le V_{CC} \le 25V$ 0.219Temperature Stability $T_{MIN} \le T_A \le T_{MAX}$ (Note 1)59Amplitude $V_{OSC}$ $V_{PIN4}$ peak to peak1.7 $V_{OSC}$ ERROR AMPLIFIER SECTIONInput Voltage $V_{I(EA)}$ $V_{PIN1} = 2.5V$ 2.422.502.58 $V_{OSC}$ Input Bias Current $I_{I(BIAS)}$ -0.3-2 $\mu$ AVOL $2V \le V_{OUT} \le 4V$ 6090dUnity Gain Bandwidth $T_{J} = 25 \ C$ (Note 1)0.71MIPSRR $I_{2} \le V_{CC} \le 25V$ 6070dOutput Sink Current $I_{O(SINK)}$ $V_{PIN2} = 2.7V, V_{PIN1} = 1.1V$ 26mOutput Source Current $I_{O(SOURCE)}$ $V_{PIN2} = 2.3V, V_{PIN1} = 5V$ -0.5-0.8m $V_{OUT}$ High $V_{OH}$ $V_{PIN2} = 2.3V, V_{PIN1} = 5V$ -0.5-0.8m	OSCILLATOR SECTION						
Temperature Stability $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Initial Accuracy	f	TJ=25℃	47	52	57	kHz
Amplitude $V_{OSC}$ $V_{PIN4}$ peak to peak         1.7 $V_{OSC}$ ERROR AMPLIFIER SECTION           Input Voltage $V_{I(EA)}$ $V_{PIN1}=2.5V$ 2.42         2.50         2.58 $V_{II}$ Input Bias Current $I_{I(BIAS)}$ -0.3         -2 $µ$ AVOL $2V \le V_{OUT} \le 4V$ 60         90         d           Unity Gain Bandwidth $T_{J}=25^{\circ}C$ (Note 1)         0.7         1         MI           PSRR $I_{2} \le V_{CC} \le 25V$ 60         70         d           Output Sink Current $I_{O(SINK)}$ $V_{PIN2}=2.7V, V_{PIN1}=1.1V$ 2         6         m           Output Source Current $I_{O(SOURCE)}$ $V_{PIN2}=2.3V, V_{PIN1}=5V$ -0.5         -0.8         m $V_{OUT}$ High $V_{OH}$ $V_{PIN2}=2.3V, V_{PIN1}=5V$ 5         6 $V_{OH}$	Voltage Stability	$\Delta f/\Delta V_{CC}$	12≦V <sub>CC</sub> ≦25V		0.2	1	%
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Temperature Stability		$T_{MIN} \le T_A \le T_{MAX}$ (Note 1)		5		%
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Amplitude	Vosc	V <sub>PIN4</sub> peak to peak		1.7		V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ERROR AMPLIFIER SECTION						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input Voltage	$V_{I(EA)}$	V <sub>PIN1</sub> =2.5V	2.42	2.50	2.58	V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input Bias Current	I <sub>I(BIAS)</sub>			-0.3	-2	μΑ
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	AVOL		$2V \leq V_{OUT} \leq 4V$	60	90		dB
Output Sink Current $I_{O(SINK)}$ $V_{PIN2}$ =2.7V, $V_{PIN1}$ =1.1V         2         6         m           Output Source Current $I_{O(SOURCE)}$ $V_{PIN2}$ =2.3V, $V_{PIN1}$ =5V         -0.5         -0.8         m           V <sub>OUT</sub> High $V_{OH}$ $V_{PIN2}$ =2.3V, $V_{PIN2}$ =15kΩ to GND         5         6         N	Unity Gain Bandwidth		T <sub>J</sub> =25°C (Note 1)	0.7	1		MHz
Output Source Current $I_{O(SOURCE)}$ $V_{PIN2}$ =2.3V, $V_{PIN1}$ =5V -0.5 -0.8 mt $V_{OUT}$ High $V_{OH}$ $V_{PIN2}$ =2.3V, $V_{RL}$ =15k $\Omega$ to GND 5 6	PSRR		$I_2 \leq V_{CC} \leq 25V$	60	70		dB
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Output Sink Current	I <sub>O(SINK)</sub>	V <sub>PIN2</sub> =2.7V,V <sub>PIN1</sub> =1.1V	2	6		mA
011 1112 / 2	Output Source Current		V <sub>PIN2</sub> =2.3V,V <sub>PIN1</sub> =5V	-0.5	-0.8		mA
$V_{OUT}$ Low $V_{OL}$ $V_{PIN2}$ =2.7 $V$ , $V_{PIN1}$ =1.1 $V$ 0.7 1.1 $V$	V <sub>OUT</sub> High	V <sub>OH</sub>	$V_{PIN2}$ =2.3V, $R_L$ =15k $\Omega$ to GND	5	6		V
	V <sub>OUT</sub> Low	V <sub>OL</sub>	V <sub>PIN2</sub> =2.7V,V <sub>PIN1</sub> =1.1V		0.7	1.1	V

## **■** ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
CURRENT SENSE SECTION								
Gain		G <sub>V</sub>	(Note 2, 3)	2.85	3	3.15	V/V	
Maximum Input signal		$V_{I(MAX)}$	V <sub>PIN1</sub> =5V( Note 2)	0.9	1	1.1	V	
PSRR			12V ≦ V <sub>CC</sub> ≦ 25V		70		dB	
Input Bias Current		I <sub>BIAS</sub>			-2	-10	μА	
Delay to Output			V <sub>PIN3</sub> =0 to 2V		150	300	ns	
OUTPUT SECTION	OUTPUT SECTION							
	Low	V <sub>OL</sub>	I <sub>O(SINK)</sub> =20mA		0.1	0.4	V	
Output Level	LOW	V OL	I <sub>O(SINK)</sub> =200mA		1.5	2.2	V	
Output Level	∐iah	V <sub>OH</sub>	I <sub>O(SOURCE)</sub> =20mA	13	13.5		V	
	High		I <sub>O(SOURCE)</sub> =200mA	12	13.5		V	
Rise Time		t <sub>R</sub>	$T_J=25^{\circ}C$ , $C_L=1$ nF (Note 1)		50	150	ns	
Fall Time		t <sub>F</sub>	$T_J=25^{\circ}C$ , $C_L=1$ nF (Note 1)		50	150	ns	
UNDER-VOLTAGE LOCK	UNDER-VOLTAGE LOCKOUT OUTPUT SECTION							
Start Threshold	3842A	V <sub>TH(ST)</sub>		14.5	16	17.5	V	
Start The Short	3843A			7.8	8.4	9	V	
Min. Operating Voltage	3842A	V <sub>OPR(MIN)</sub>	After Turn On	8.5	10	11.5	V	
win. Operating voitage	3843A			7	7.6	8.2	V	
PWM SECTION								
Duty Cycle	MAX	D <sub>(MAX)</sub>		95	97	100	%	
	MIN	D <sub>(MIN)</sub>				0	%	
TOTAL STANDBY CURR	ENT							
Start-up Current		I <sub>ST</sub>			0.12	0.3	mA	
Operating Supply Current		I <sub>CC(OPR)</sub>	V <sub>PIN2</sub> =V <sub>PIN3</sub> =0V		11	17	mA	
V <sub>CC</sub> Zener Voltage		$V_z$	I <sub>CC</sub> =25mA		34		V	

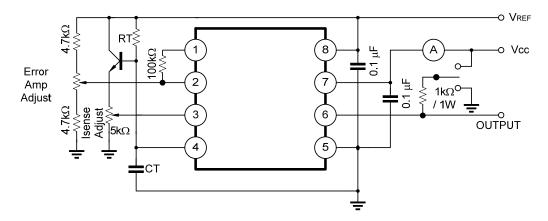
Note:1. These parameters, although guaranteed, are not 100% tested in production.

- 2. Parameters measured at trip point of latch with V<sub>PIN 2</sub>=0.
- 3. Gain defined as:

$$A = \frac{\mathbb{I} \ V_{PIN1}}{\mathbb{I} \ V_{PIN3}} \ ; 0 \mathbb{I} \ V_{PIN3} \mathbb{I} \ 0.8 V$$

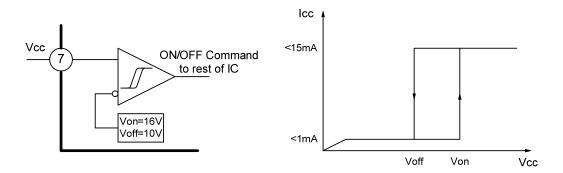
4. Adjust  $V_{CC}$  above the start threshold before setting at 15V.

## **■** OPEN-LOOP LABORATORY TEST FIXTURE



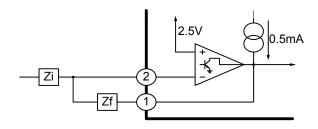
High peak current associated with capacity loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in single point GND. The transistor and  $5k\Omega$  potentio-meter are used to sample the oscillator waveform and apply an adjustable Ramp to Pin 3.

#### ■ UNDER-VOLTAGE LOCKOUT



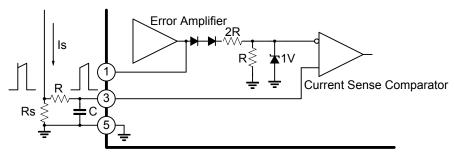
During Under-Voltage Lockout, the output driver is biased to a high impedance state. Pin 6 should be shunt to GND with a bleeder resistor to prevent activating the power switch with output leakage currents.

#### ■ ERROR AMPLIFIER CONFIGURATION



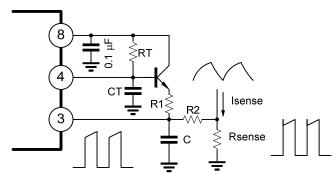
Error amplifier can source or sink up to 0.5mA

## **■ CURRENT SENSE CIRCUIT**



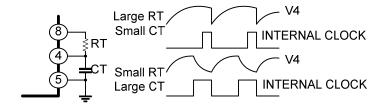
Peak current (Is) determined by the formula:  $I_{SMAX}$ =1.0V/Rs. A small RC filter be required to suppress switch transients.

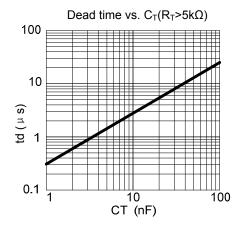
## **■ SLOPE COMPENSATION**

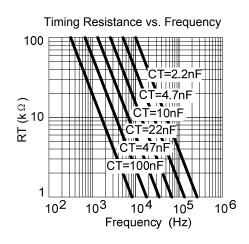


A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converts requiring duty cycles over 50%. Note that capacitor C, forms a filter with R2 to suppress the leading edge switch spikes.

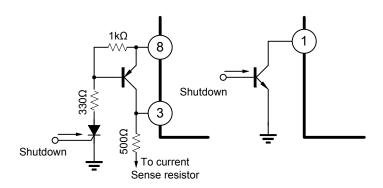
## OSCILLATOR SECTION







## ■ SHUTDOWN TECHNIQUES

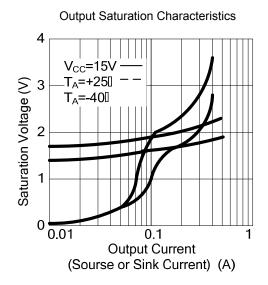


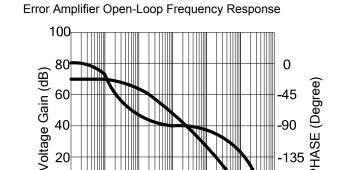
Shutdown UTC **UC3842A** can be accomplished by two methods; either raise Pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method caused the output of PWM comparator to be high(refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed. In one example, an externally latched shut-down may be accomplished by adding an SCR which be reset by cycling  $V_{CC}$  below the lower UVLO threshold. At this point the reference turns off allowing the SCR to reset.

-180

106 107

## ■ TYPICAL CHARACTERISTICS

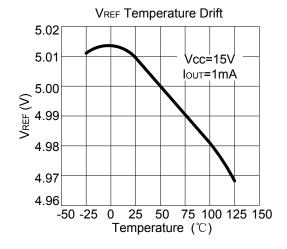


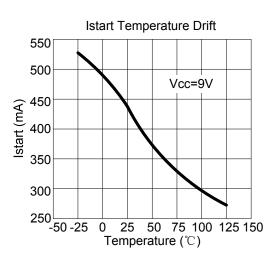


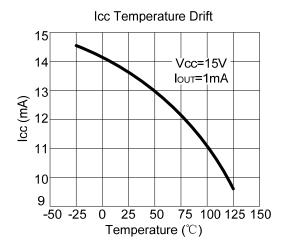
10<sup>4</sup> 10<sup>5</sup>

Frequency (Hz)

0







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NCP4204MNTXG NCP6132AMNR2G NCP81102MNTXG NCP81203MNTXG NCP81206MNTXG NX2155HCUPTR UBA2051C
IR35201MTRPBF AP3842CMTR-EI NCP1247AD065R2G NCP1015ST65T3G NCP1240AD065R2G NCP1240FD065R2G
NCP1361BABAYSNT1G NCP1230P100G NCP1612BDR2G NX2124CSTR SG2845M NCP1366BABAYDR2G NCP81101MNTXG
TEA19362T/IJ NCP81174NMNTXG NCP4308DMTTWG NCP4308DMNTWG NCP4308AMTTWG NCP1366AABAYDR2G
NCP1256ASN65T1G NCP1251FSN65T1G NCP1246BLD065R2G MB39A136PFT-G-BND-EREI NCP1256BSN100T1G LV5768V-ATLM-E NCP1365BABCYDR2G NCP1365AABCYDR2G IR35204MTRPBF MCP1633T-E/MG