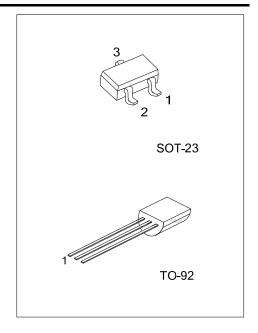
XL/ML1225 scr

# MEDIUM POWER LOW VOLTAGE TRANSISTOR

#### DESCRIPTION

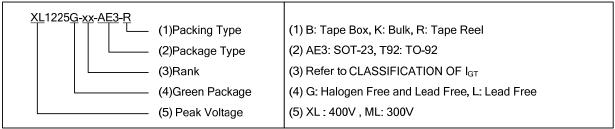
The **XL1225/ML1225** silicon controlled rectifiers are high performance planner diffused PNPN devices. These parts are intended for low cost high volume applications.



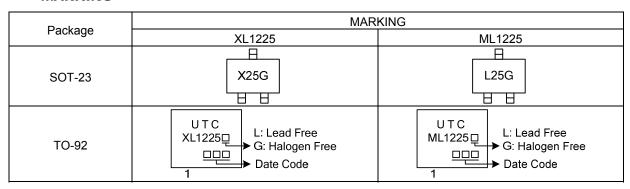
#### ORDERING INFORMATION

Ordering	Ordering Number		Pin Assignment			Da alain a	
Lead Free	Halogen Free	gen Free Package 1		2	3	Packing	
-	XL1225G-xx-AE3-R	SOT-23	G	K	Α	Tape Reel	
XL1225L-xx-T92-B	XL1225G-xx-T92-B	TO-92	K	G	Α	Tape Box	
XL1225L-xx-T92-K	XL1225G-xx-T92-K	TO-92	K	G	Α	Bulk	
-	ML1225G-xx-AE3-R	SOT-23	G	K	Α	Tape Reel	
ML1225L-xx-T92-B	ML1225G-xx-T92-B	TO-92	K	G	Α	Tape Box	
ML1225L-xx-T92-K	ML1225G-xx-T92-K	TO-92	K	G	Α	Bulk	

Note: Pin Assignment : G: Gate K: Cathode A: Anode



#### ■ MARKING



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## ■ ABSOLUATE MAXIUM RATINGS (Ta= 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Repetitive Peak Off-State Voltage	XL1225	V	400	V	
$(T_J = 40 \sim 125^{\circ}C, R_{GK} = 1k\Omega)$	ML1225	V <sub>DRM</sub> 300		V	
On-State Current (Tc=40°C)		I <sub>T(RMS)</sub>	0.8	Α	
Average On-State Current (Half Cycle=180,Tc=40°C)		I <sub>T(AV)</sub>	0.5	Α	
Peak Reverse Gate Voltage (IGR=10μA)		$V_{GRM}$	1	V	
Peak Gate Current (10μs Max.)		$I_{GM}$	0.1	Α	
Gate Dissipation (20ms Max.)		$P_{G(AV)}$	150	mW	
Junction Temperature		$T_J$	+125	°C	
Storage Temperature		T <sub>STG</sub>	-40 ~ +150	°C	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

# ■ ELECTRICAL CHARACTERISTICS (Ta= 25°C, unless otherwise specified.)

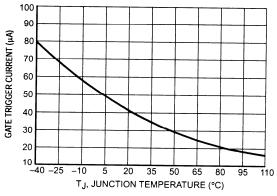
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off State Leakage Current		$V_{DRM}(R_{GK}=1K\Omega), T_J=125^{\circ}C$			0.1	mA
Off State Leakage Current		$V_{DRM}(R_{GK}=1K\Omega), T_J=25^{\circ}C$			1.0	μA
0 - 01-1-1/-11	V <sub>T</sub>	AT I <sub>T</sub> =0.4A			1.4	
On State Voltage		AT I <sub>T</sub> =0.8A			2.2	· V
On State Threshold Voltage	V <sub>T(TO)</sub>	T <sub>J</sub> =125°C			0.95	V
On State Slops Resistance	Rt	T <sub>J</sub> =125°C			600	m
Gate Trigger Current	$I_{GT}$	V <sub>D</sub> =7V			200	μA
Gate Trigger Voltage	$V_{GT}$	V <sub>D</sub> =7V			0.8	V
Holding Current	Ι <sub>Η</sub>	R <sub>GK</sub> =1KΩ			5	mA
Latching Current	ΙL	R <sub>GK</sub> =1KΩ			6	mA
Critical Rate of Voltage Rise	DV/DT	$V_D=0.67 \times V_{DRM}(R_{GK}=1K\Omega), T_J=125^{\circ}C$				V/µs
Critical Rate of Current Rise	DV/DT	$I_G$ =10mA, d $I_G$ /dt=0.1A/ $\mu$ s, $T_J$ =125°C				A/µs
Gate Controlled Delay Time	$T_GD$	l <sub>G</sub> =10mA, dl <sub>G</sub> /dt=0.1A/μs			2.2	μs
Commutated Turn-off Time	TG	$T_J = 85^{\circ}C, V_D = 0.67^*V_{DRM}, V_R = 35V,$ $I_T = I_{T(AV)}$			200	μs

# ■ CLASSIFICATION OF I<sub>GT</sub>

RANK	В	С	AA	AB	AC	AD
RANGE	50-100	100-200	8-15	15-20	20-25	25-50

<sup>2.</sup> The device is guaranteed to meet performance specification within  $0^{\circ}\text{C} \sim 70^{\circ}\text{C}$  operating temperature range and assured by design from  $-20^{\circ}\text{C} \sim 85^{\circ}\text{C}$ .

### **■ TYPICAL CHARACTERICS**



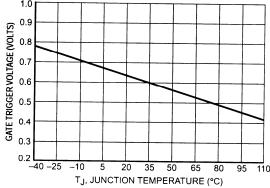
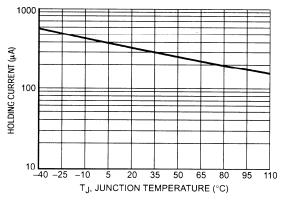


Figure 1. Typical Gate Trigger Current versus Junction Temperature

Figure 2. Typical Gate Trigger Voltage versus Junction Temperature



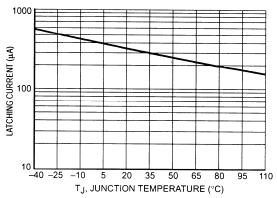


Figure 3. Typical Holding Current versus Junction Temperature

Figure 4. Typical Latching Current versus Junction Temperature

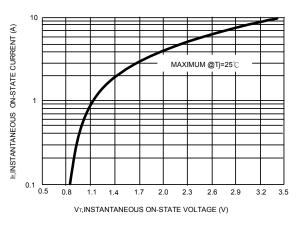


Figure 5. Typical On-State Characteristics

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