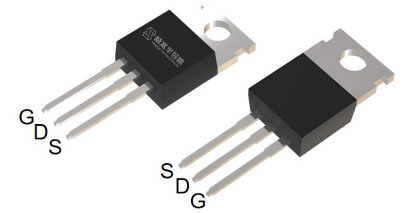


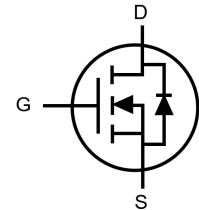
Features

- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=10\text{ V}$
- 100% Avalanche test

V_{DS}	100	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	4.5	m Ω
$I_D(\text{Silicon Limited})$	200	A
$I_D(\text{Package Limited})$	130	A


TO-220AB


Part ID	Package Type	Marking	Packing
VS1401ATH	TO-220AB	1401ATH	50pcs/Tube



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{(BR)DSS}$	Drain-Source breakdown voltage	100	V	
V_{GS}	Gate-Source voltage	± 25	V	
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	200	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 25^\circ\text{C}$	200	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 100^\circ\text{C}$	142	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	130	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	800	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	15	A
		$T_A = 70^\circ\text{C}$	12	A
E_{AS}	Avalanche energy, single pulsed ②	900	mJ	
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	375	W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	2	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$	

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.4	0.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	75	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =100V, V _{GS} =0V	--	--	100	μA
IGSS	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.4	3	3.6	V
RDS(on)	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =80A	--	4.5	5.5	mΩ
		T _j =100°C	--	6.5	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	11065	14755	19625	pF
Coss	Output Capacitance		500	665	885	pF
Crss	Reverse Transfer Capacitance		370	495	660	pF
Rg	Gate Resistance	f=1MHz	0.2	2.3	5	Ω
Qg	Total Gate Charge	V _{DS} =50V, I _D =40A, V _{GS} =10V	--	232	309	nC
Qgs	Gate-Source Charge		--	59	78	nC
Qgd	Gate-Drain Charge		--	60	90	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V _{DD} =50V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	35	--	ns
Tr	Turn-on Rise Time		--	67	--	ns
Td(off)	Turn-Off Delay Time		--	128	--	ns
Tf	Turn-Off Fall Time		--	64	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
VSD	Forward on voltage	I _{SD} =80A, V _{GS} =0V	--	0.9	1.2	V
Trr	Reverse Recovery Time	T _j =25°C, I _{sd} =40A, V _{GS} =0V	--	44	88	ns
Qrr	Reverse Recovery Charge	di/dt=100A/μs	--	77	154	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 60A, V_{GS} = 10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

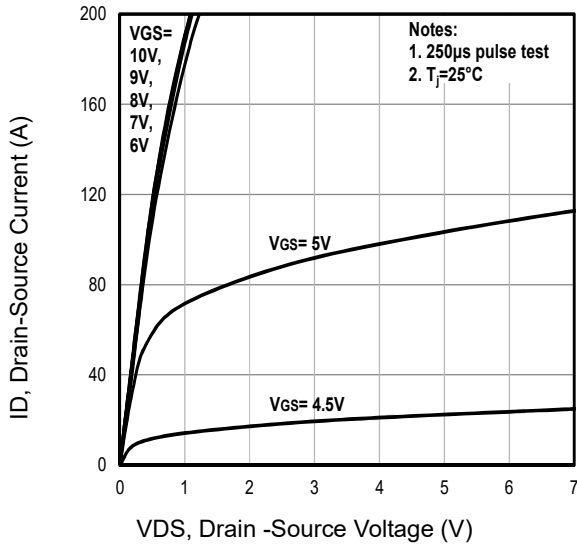


Fig1. Typical Output Characteristics

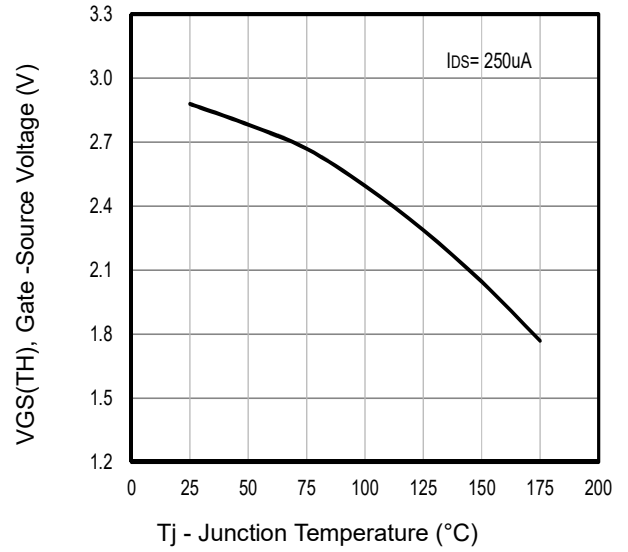


Fig2. V_{GS(TH)} Gate-Source Voltage Vs. T_j

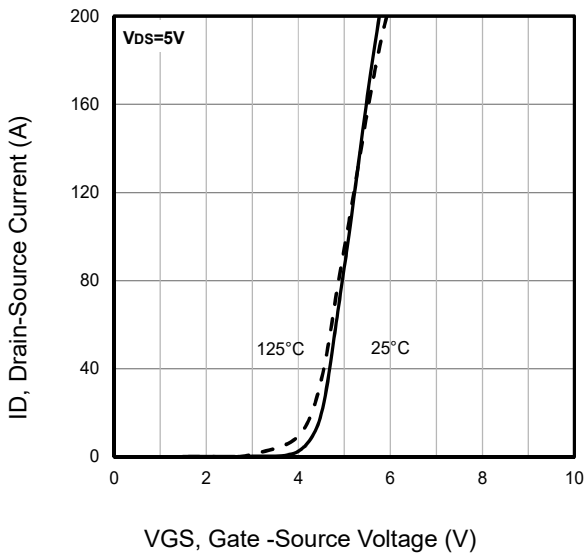


Fig3. Typical Transfer Characteristics

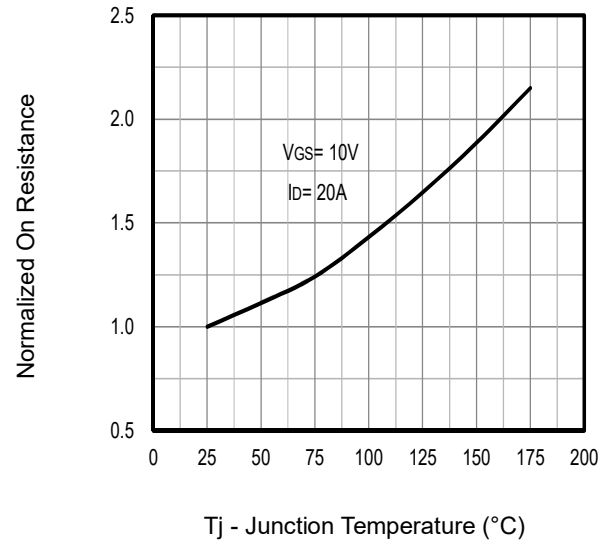


Fig4. Normalized On-Resistance Vs. T_j

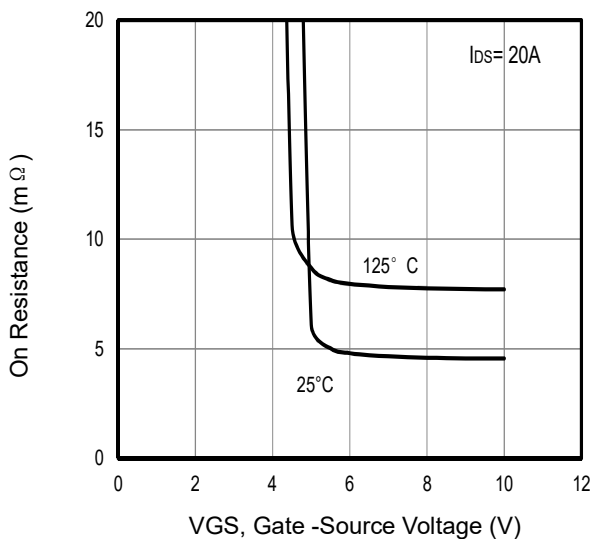


Fig5. On Resistance Vs Gate-Source Voltage

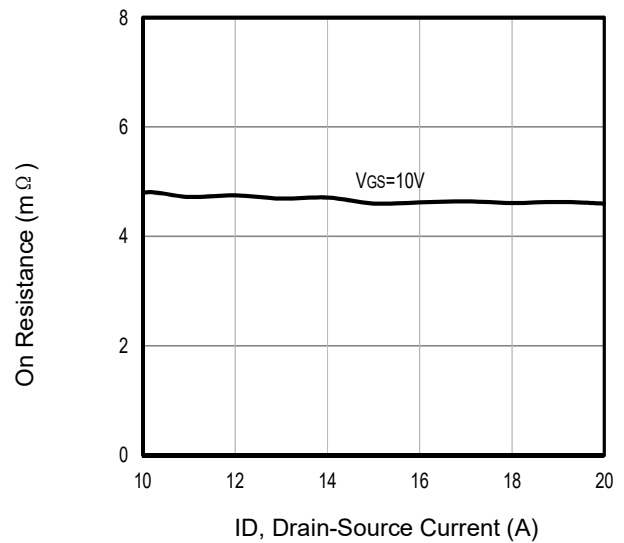


Fig6. On Resistance Vs Drain Current and Gate Voltage

Typical Characteristics

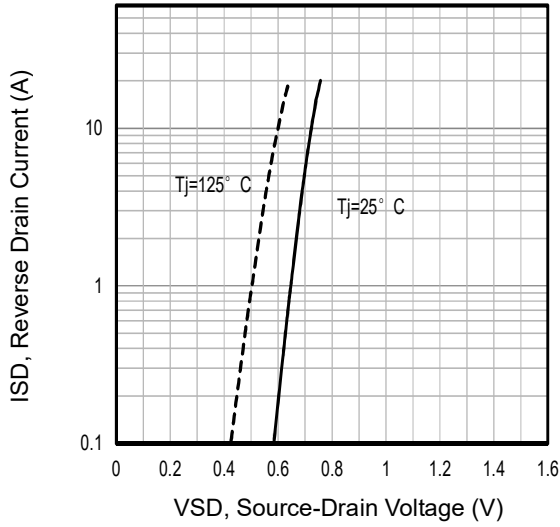


Fig7. Typical Source-Drain Diode Forward Voltage

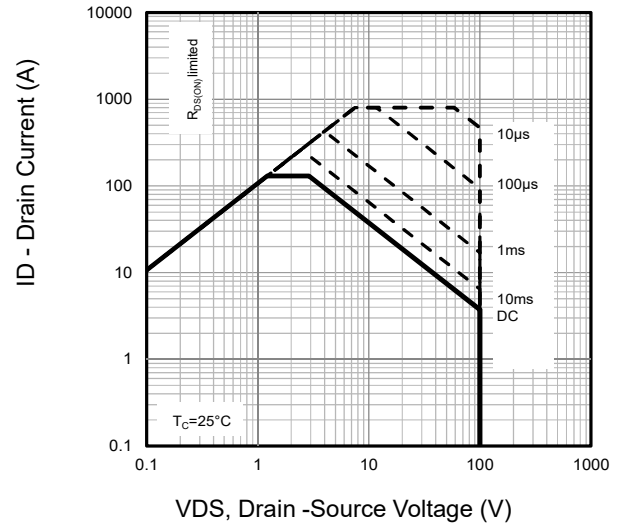


Fig8. Maximum Safe Operating Area

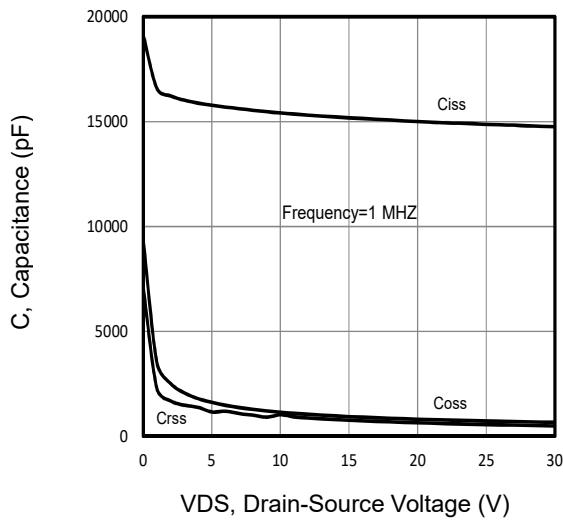


Fig9. Typical Capacitance Vs. Drain-Source Voltage

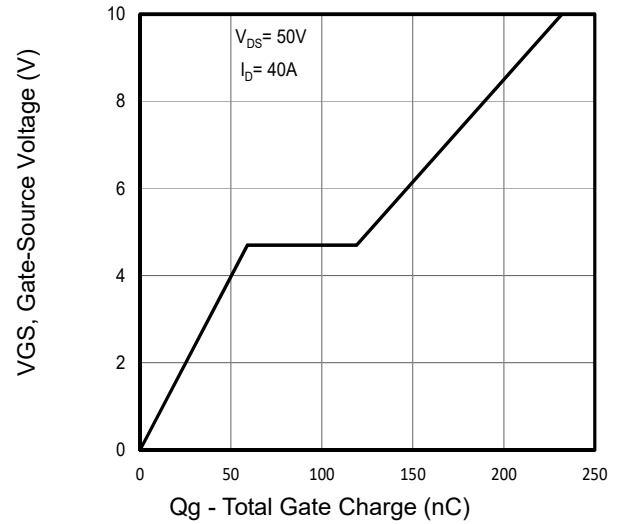


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

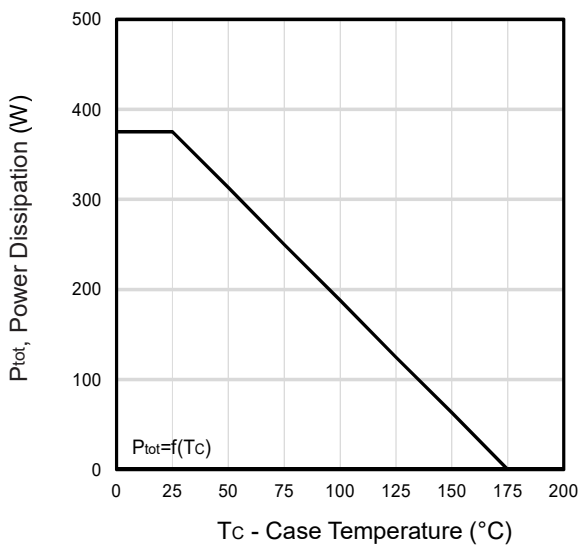


Fig11. Power Dissipation Vs. Case Temperature

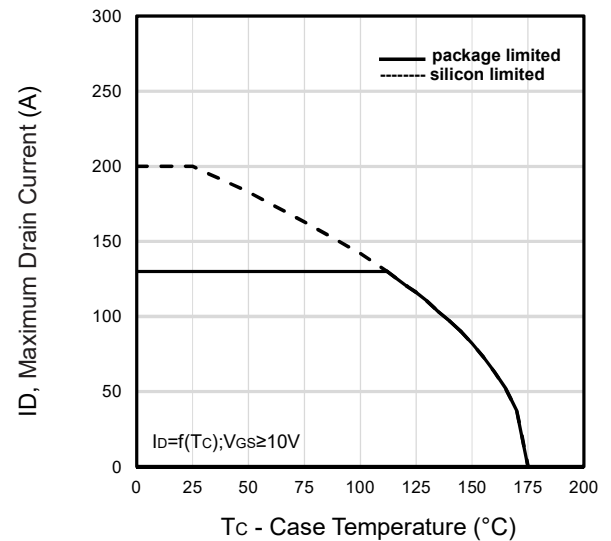


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

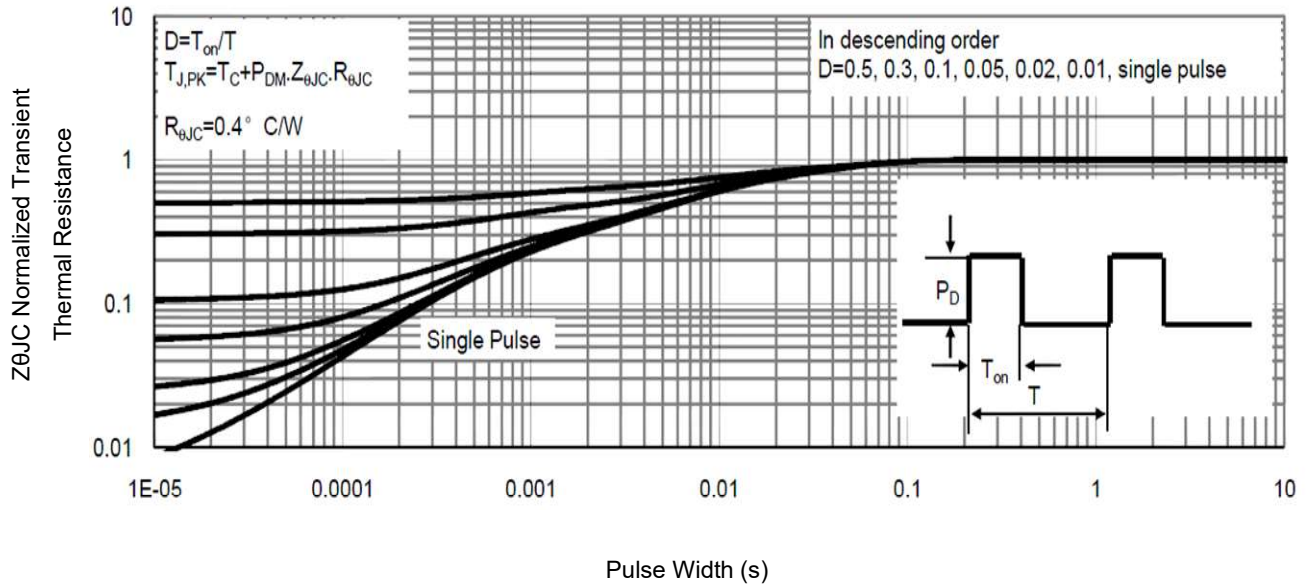


Fig13 . Normalized Maximum Transient Thermal Impedance

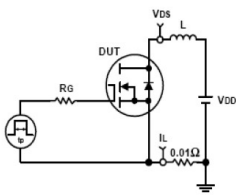


Fig14. Unclamped Inductive Test Circuit and waveforms

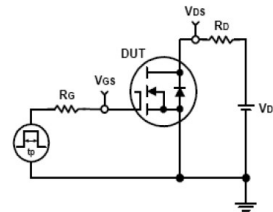
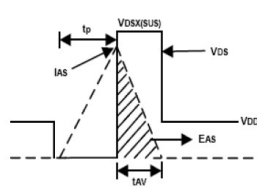
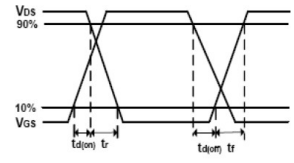
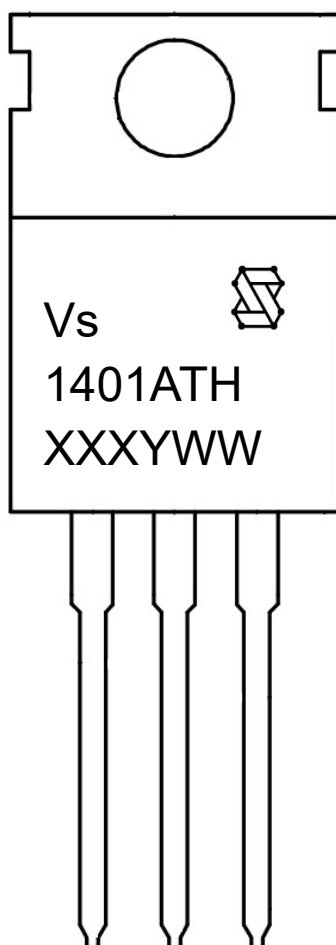


Fig15. Switching Time Test Circuit and waveforms



Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (1401ATH)

3rd line: Date code (XXXYWW)

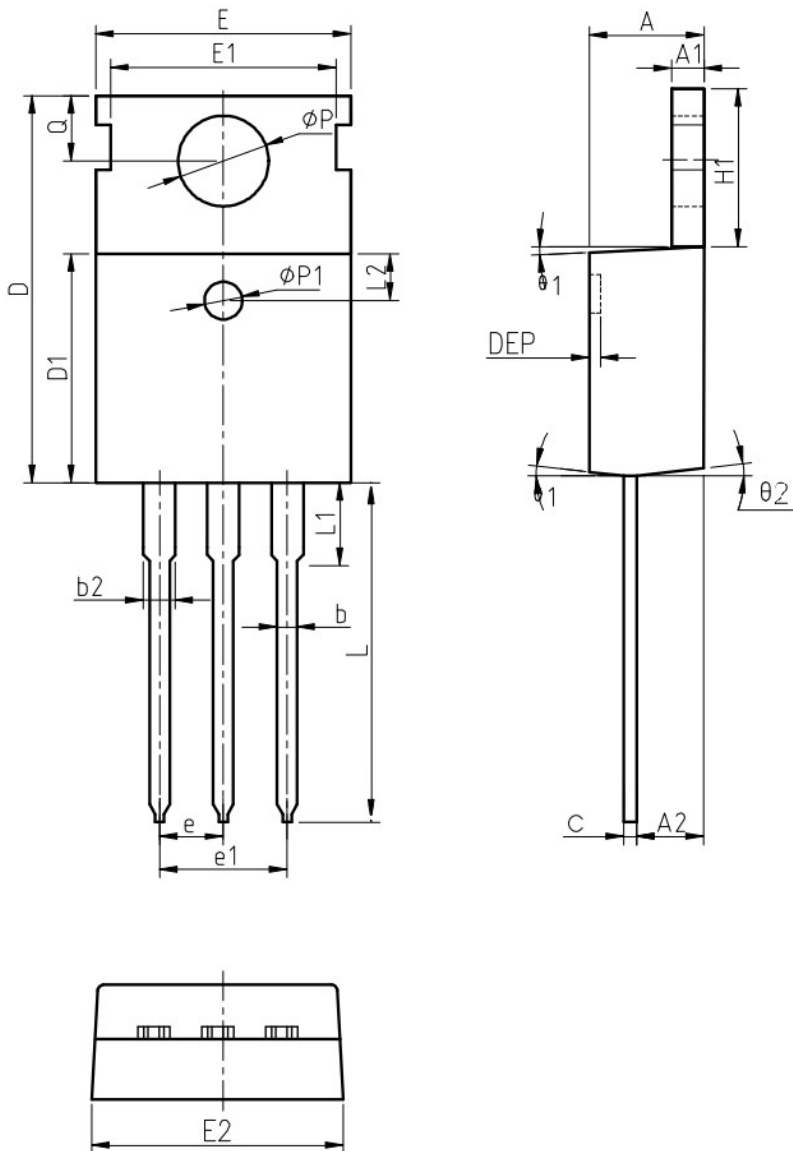
XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-220AB Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.30	4.52	4.70
A1	1.15	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.32	1.50
c	0.45	0.50	0.61
D	15.30	15.65	15.90
D1	9.00	9.20	9.40
DEP	0.05	0.10	0.25
E	9.66	9.90	10.28
E1	-	8.70	-
E2	9.80	10.00	10.20
φP1	1.40	1.50	1.60
e	2.54 BSC		
e1	5.08 BSC		
H1	6.40	6.50	6.80
L	12.70	-	14.27
L1	-	-	3.95
L2	2.40	2.50	2.60
φP	3.53	3.60	3.70
Q	2.70	2.80	2.90
θ1	5 °	7 °	9 °
θ2	1 °	3 °	5 °

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

Customer Service

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[405094E](#) [423220D](#) [MIC4420CM-TR](#) [VN1206L](#) [614234A](#) [715780A](#) [SSM6J414TU,LF\(T](#) [751625C](#) [PSMN4R2-30MLD](#)
[TK31J60W5,S1VQ\(O](#) [2SK2614\(TE16L1,Q\)](#) [DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#)
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[BSS340NWH6327XTSA1](#) [MCM3400A-TP](#) [DMTH10H4M6SPS-13](#) [IRF40SC240ARMA1](#) [IPS60R1K0PFD7SAKMA1](#)
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