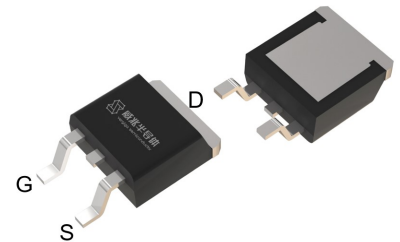


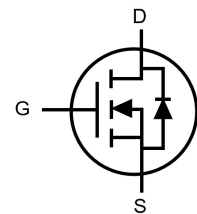
Features

- Enhancement mode
- Very low on-resistance
- VitoMOS[®] II Technology
- Fast Switching and High efficiency
- 100% Avalanche Tested, Rg 100% Tested

V_{DS}	100	V
$R_{DS(on),TYP@ V_{GS}=10V}$	3.6	mΩ
$I_{D(Silicon Limited)}$	170	A
$I_{D(Package Limited)}$	130	A

TO-263


Part ID	Package Type	Marking	Packing
VS1602GMH	TO-263	1602GMH	800pcs/Reel



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	100	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current (Wire bond limited)	$T_C = 25^\circ\text{C}$ 130	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 25^\circ\text{C}$ 170	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_C = 100^\circ\text{C}$ 120	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 25^\circ\text{C}$ 130	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$ 675	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$ 16	A
		$T_A = 70^\circ\text{C}$ 12	A
E_{AS}	Avalanche energy, single pulsed ②	484	mJ
P_D	Maximum power dissipation ③	$T_C = 25^\circ\text{C}$ 250	W
P_{DSM}	Maximum power dissipation ④	$T_A = 25^\circ\text{C}$ 2.1	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

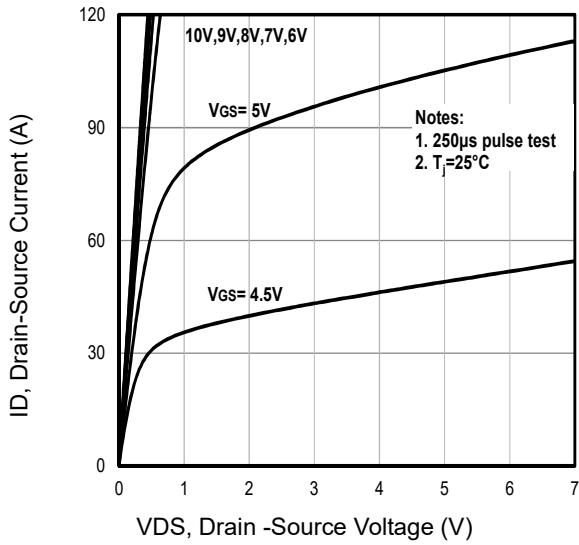
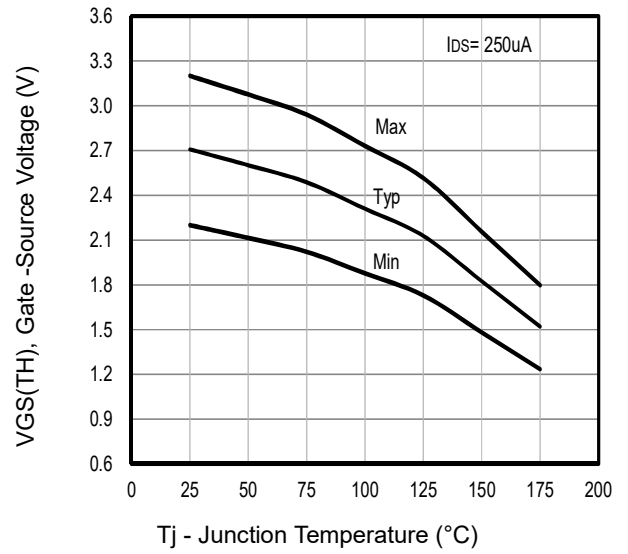
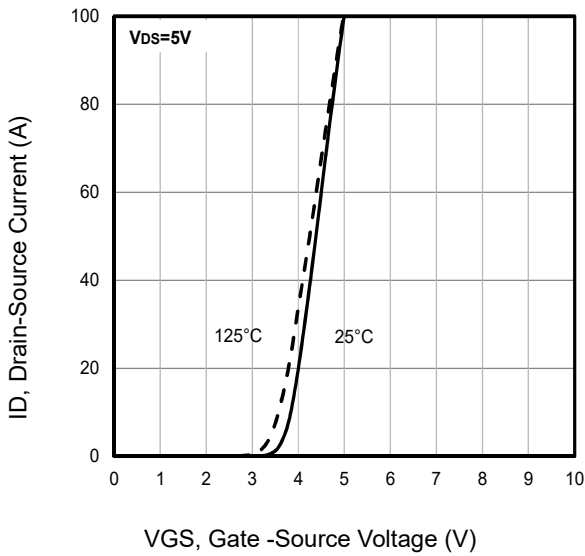
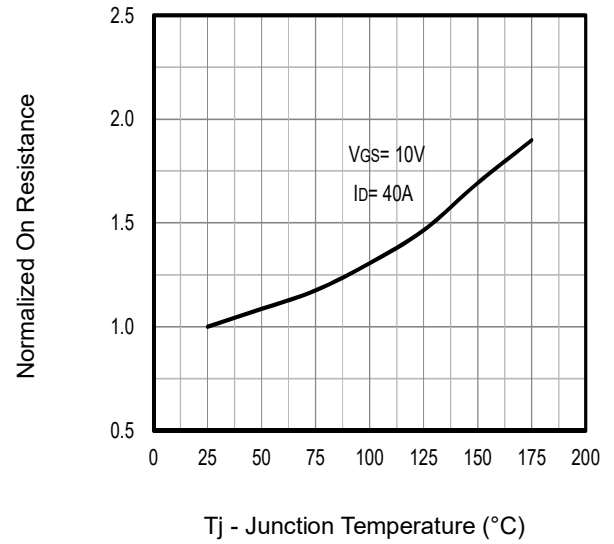
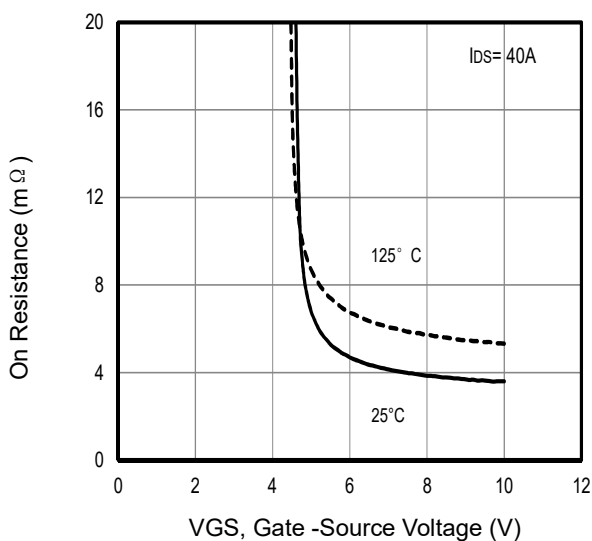
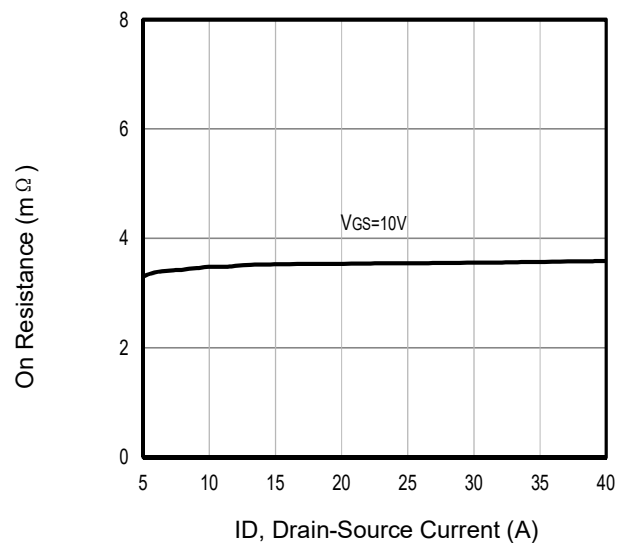
Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ⑤	0.5	0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ⑥	50	60	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C) ^⑦	V _{DS} =100V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.2	2.7	3.2	V
R _{DS(on)}	Drain-Source On-State Resistance ^⑧	V _{GS} =10V, I _D =40A	--	3.6	4.5	mΩ
		(T _j =100°C) ^⑦	--	4.7	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance ^⑦	V _{DS} =50V, V _{GS} =0V, f=1MHz	--	5440	--	pF
C _{oss}	Output Capacitance ^⑦		--	1035	--	pF
C _{rss}	Reverse Transfer Capacitance ^⑦		--	35	--	pF
R _g	Gate Resistance	f=1MHz	--	1.8	--	Ω
Q _g	Total Gate Charge ^⑦	V _{DS} =50V, I _D =40A, V _{GS} =10V	--	91	--	nC
Q _{gs}	Gate-Source Charge ^⑦		--	25	--	nC
Q _{gd}	Gate-Drain Charge ^⑦		--	25	--	nC
Switching Characteristics ^⑦						
T _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	21	--	ns
T _r	Turn-on Rise Time		--	69	--	ns
T _{d(off)}	Turn-Off Delay Time		--	57	--	ns
T _f	Turn-Off Fall Time		--	70	--	ns
Source- Drain Diode Characteristics@ T_j= 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.8	1.2	V
T _{rr}	Reverse Recovery Time ^⑦	I _{sd} =40A, V _{GS} =0V	--	59	--	ns
Q _{rr}	Reverse Recovery Charge ^⑦	di/dt=100A/μs	--	71	--	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② EAS of 484mJ is based on starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 44A, V_{GS} = 10V; 100% FT tested at L = 0.5mH, I_{AS} = 22A.
- ③ The power dissipation P_d is based on T_{j(max)}, using junction-to-case thermal resistance R_{θJC}.
- ④ The power dissipation P_{dsm} is based on T_{j(max)}, using junction-to-ambient thermal resistance R_{θJA}.
- ⑤ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.
- ⑥ The value of R_{θJA} is measured with the device in a still air environment with T_A = 25°C.
- ⑦ Guaranteed by design, not subject to production testing.
- ⑧ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

Fig1. Typical Output Characteristics

Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

Fig3. Typical Transfer Characteristics

Fig4. Typical Normalized On-Resistance Vs. T_j

Fig5. Typical On Resistance Vs Gate-Source Voltage

Fig6. Typical On Resistance Vs Drain Current and Gate

Typical Characteristics

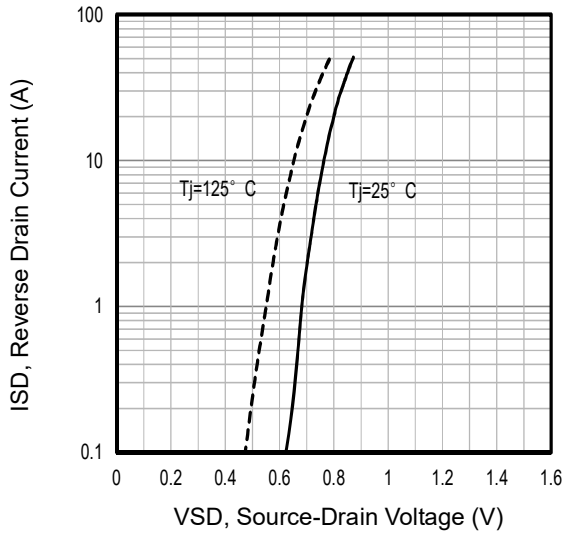


Fig7. Typical Source-Drain Diode Forward Voltage

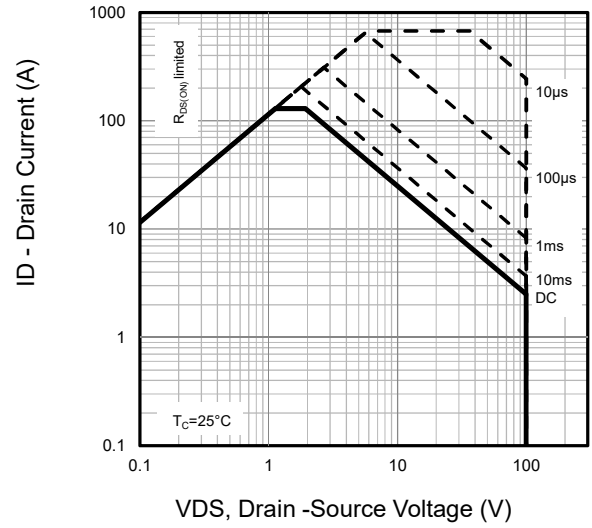


Fig8. Maximum Safe Operating Area

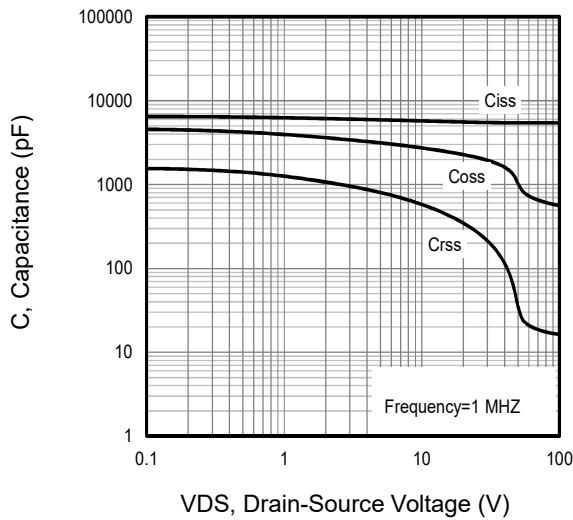


Fig9. Typical Capacitance Vs. Drain-Source Voltage

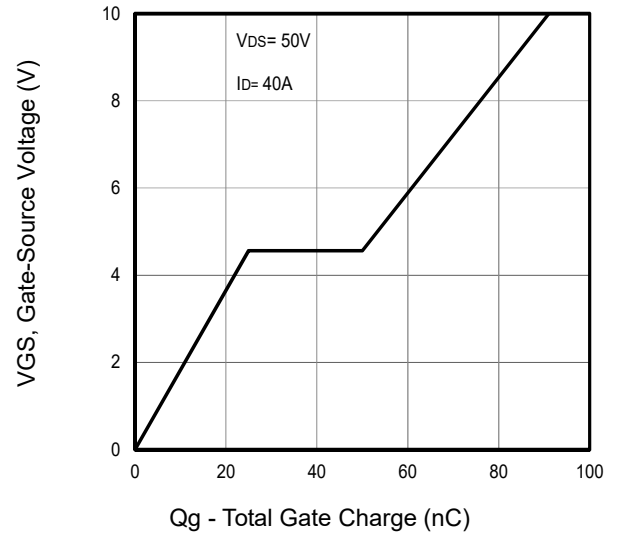


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

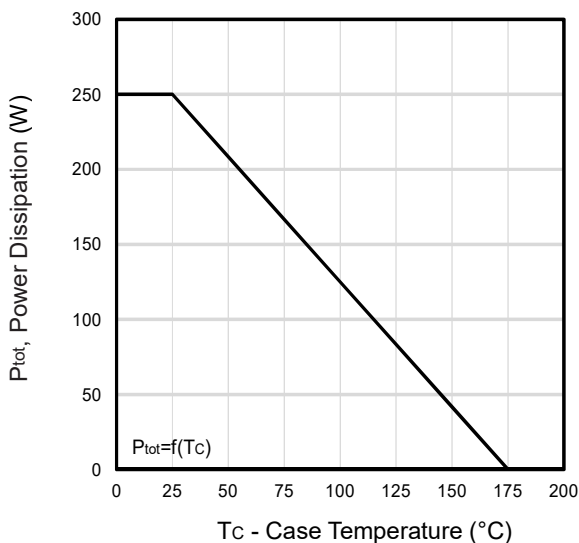


Fig11. Power Dissipation Vs. Case Temperature

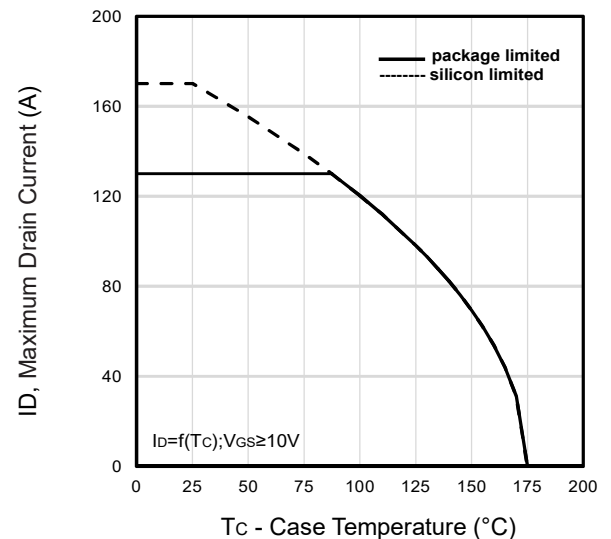


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

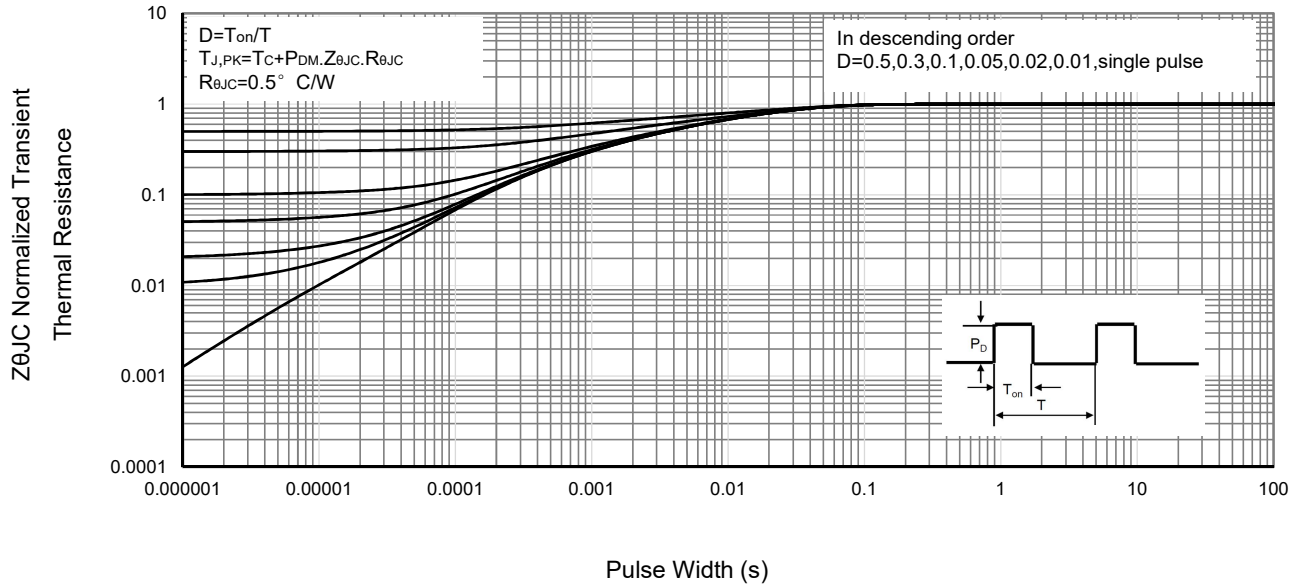


Fig13 . Normalized Maximum Transient Thermal Impedance

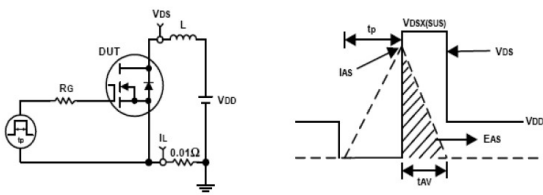


Fig14. Unclamped Inductive Test Circuit and waveforms

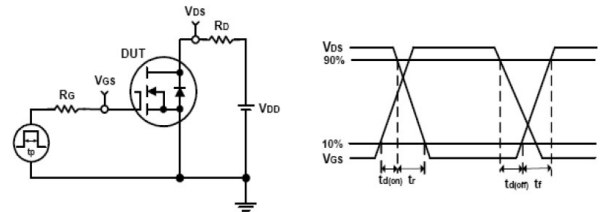
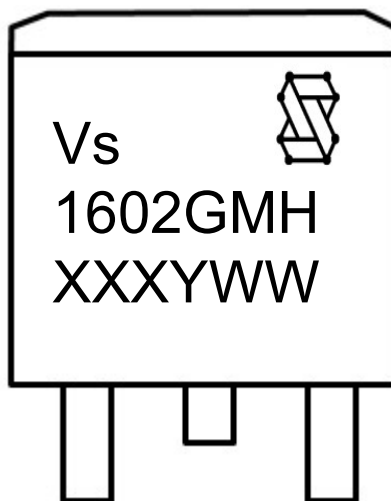


Fig15. Switching Time Test Circuit and waveforms

Marking Information


1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (1602GMH)

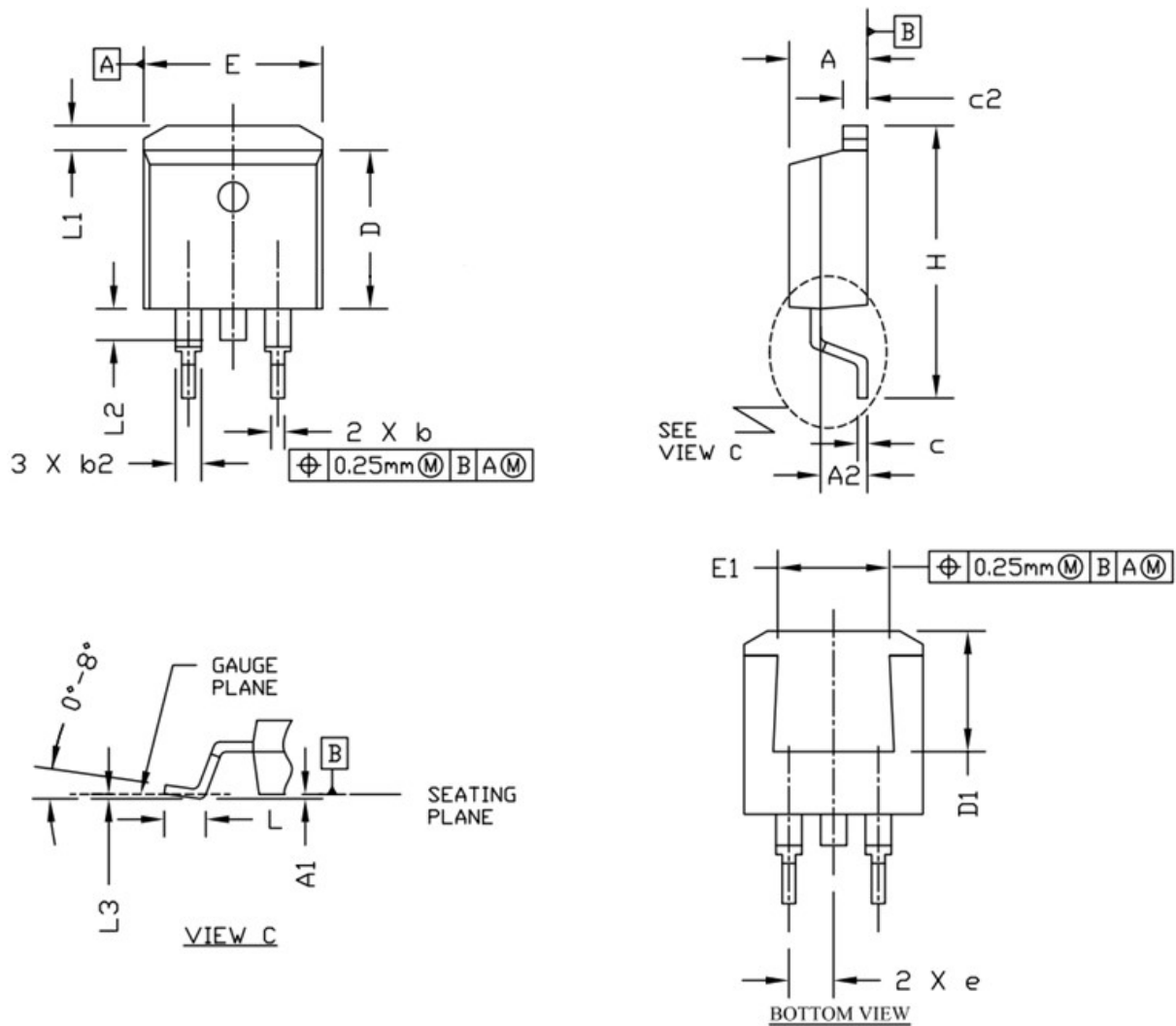
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-263 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.400	4.570	4.700
A1	0.000	0.100	0.200
A2	2.300	2.400	2.500
b	0.700	0.800	0.900
b2	1.200	1.270	1.360
c	0.381	0.500	0.737
c2	1.220	1.300	1.350
D	8.600	9.200	9.300
D1	6.860		
e	2.540 BSC		
E	9.780	9.880	10.260
E1	6.225		
H	14.700	15.100	15.500
L	2.000	2.550	2.750
L1	1.000	1.200	1.400
L2	1.300	1.600	1.700
L3	0.255 BSC		

Notes:

1. Refer to JEDEC TO-263 variation AB
2. Dimension "D" & "E" do NOT include mold flash, mold flash shall not exceed 0.127mm per side.

Customer Service
Sales and Service:
sales@vgsemi.com
Vergiga Semiconductor CO., LTD
TEL: (86-755) -26902410

FAX: (86-755) -26907027

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[BSS340NWH6327XTSA1](#) [MCM3400A-TP](#) [DMTH10H4M6SPS-13](#) [IRF40SC240ARMA1](#) [IPS60R1K0PFD7SAKMA1](#)
[IPS60R360PFD7SAKMA1](#) [IPS60R600PFD7SAKMA1](#)