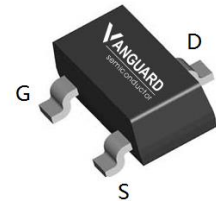


Features

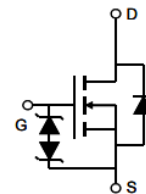
- N-Channel
- Enhancement Mode
- Fast Switching
- ESD Protected by HBM up to 2.5KV
- Pb-free lead plating; RoHS compliant

V_{DS}	60	V
$R_{DS(on),typ@VGS=10V}$	1	Ω
$R_{DS(on),typ@VGS=4.5V}$	1.1	Ω
I_D	0.76	A

SOT23



Part ID	Package Type	Marking	Tape and reel information
VS2N7002K	SOT23	72K	3000pcs/reel



Maximum ratings, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	60	V
V_{GS}	Gate-Source voltage	± 16	V
I_S	Diode continuous forward current	$T_A=25^\circ\text{C}$ 0.8	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A=25^\circ\text{C}$ 0.76	A
		$T_A=100^\circ\text{C}$ 0.48	A
I_{DM}	Pulse drain current tested ①	$T_A=25^\circ\text{C}$ 3	A
P_D	Maximum power dissipation	$T_A=25^\circ\text{C}$ 1	W
T_{STG}, T_J	Storage and operating temperature range	-55 to 150	$^\circ\text{C}$
Thermal characteristics			
Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	80	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	125	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current (T _j =125°C)	V _{DS} =48V, V _{GS} =0V	--	--	1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±16V, V _{DS} =0V	--	--	±10	μA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	1.2	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance ②	V _{GS} =10V, I _D =0.5A	--	1	3	Ω
		T _j =100°C	--	1.3	--	Ω
R _{DS(ON)}	Drain-Source On-State Resistance ②	V _{GS} =4.5V, I _D =0.05A	--	1.1	3	Ω
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	20	26	32	pF
C _{oss}	Output Capacitance		--	11	16	pF
C _{riss}	Reverse Transfer Capacitance		--	7	12	pF
Q _g (10V)	Total Gate Charge	V _{DS} =30V, I _D =1A, V _{GS} =10V	--	1.43	--	nC
Q _g (4.5V)	Total Gate Charge		--	0.7	--	nC
Q _{gs}	Gate-Source Charge		--	0.35	--	nC
Q _{gd}	Gate-Drain Charge		--	0.22	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =0.5A, R _G =3Ω, V _{GS} =10V	--	2.4	--	ns
t _r	Turn-on Rise Time		--	2.8	--	ns
t _{d(off)}	Turn-Off Delay Time		--	5.6	--	ns
t _f	Turn-Off Fall Time		--	18	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =0.5A, V _{GS} =0V	--	0.9	1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =0.5A, V _{GS} =0V	--	10.4	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	4.7	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
 ② Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

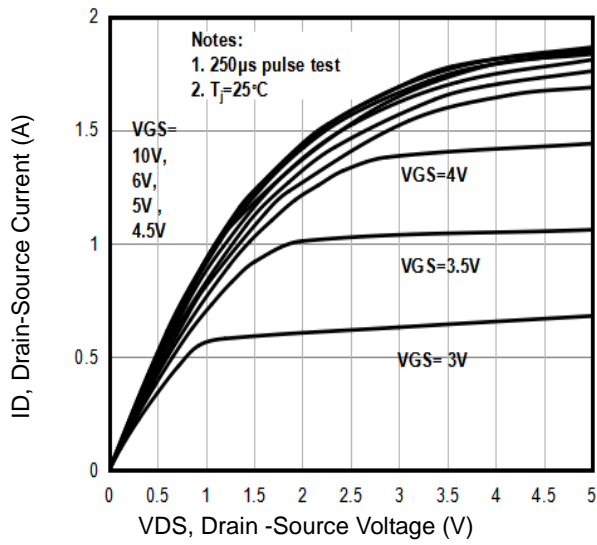


Fig1. Typical Output Characteristics

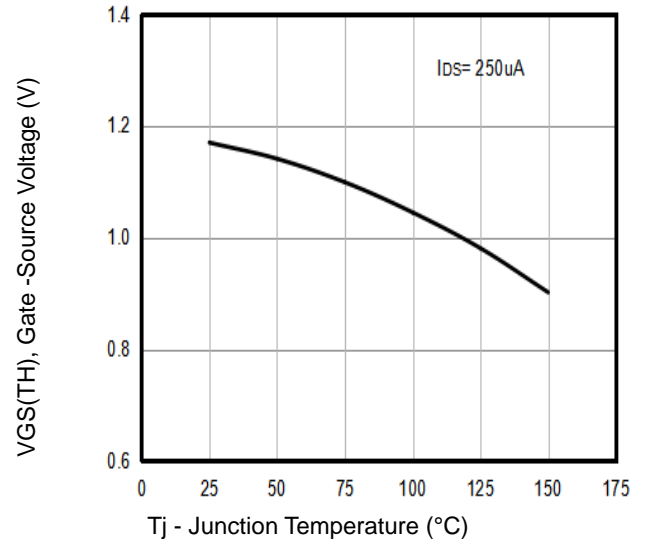


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

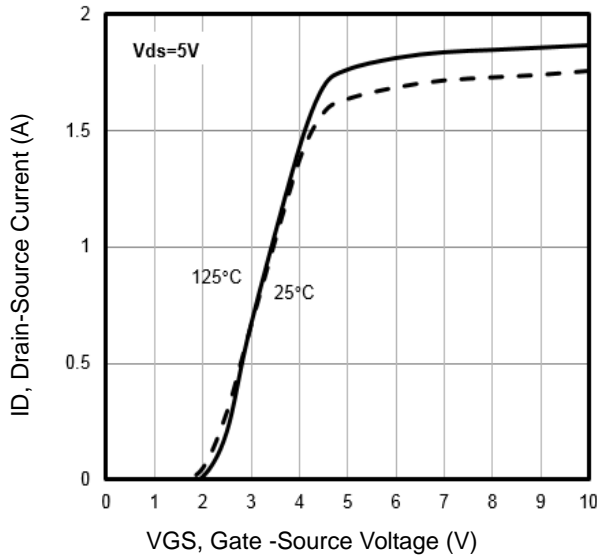


Fig3. Typical Transfer Characteristics

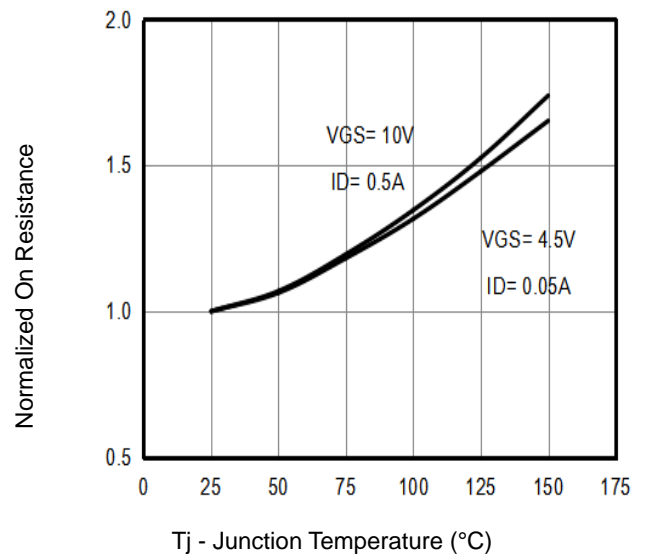


Fig4. Normalized On-Resistance Vs. T_j

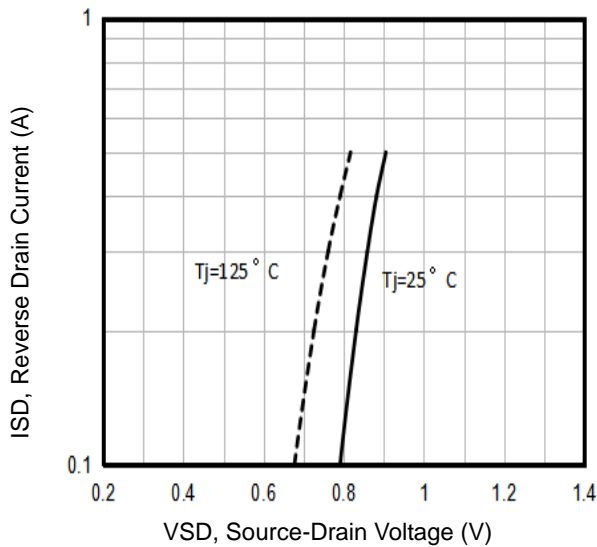


Fig5. Typical Source-Drain Diode Forward Voltage

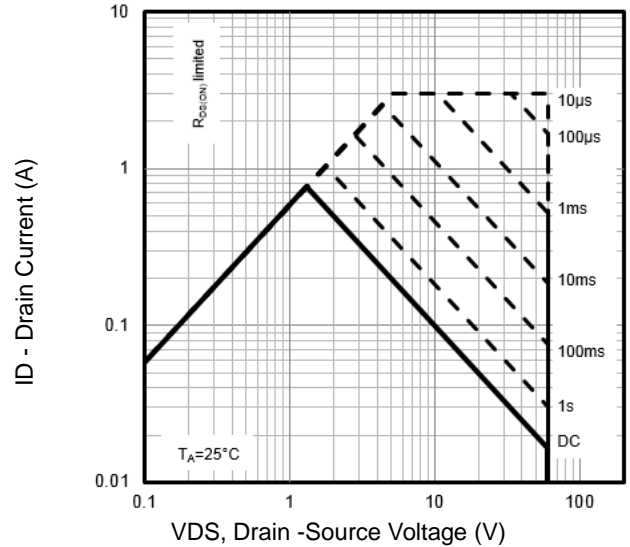


Fig6. Maximum Safe Operating Area

Typical Characteristics

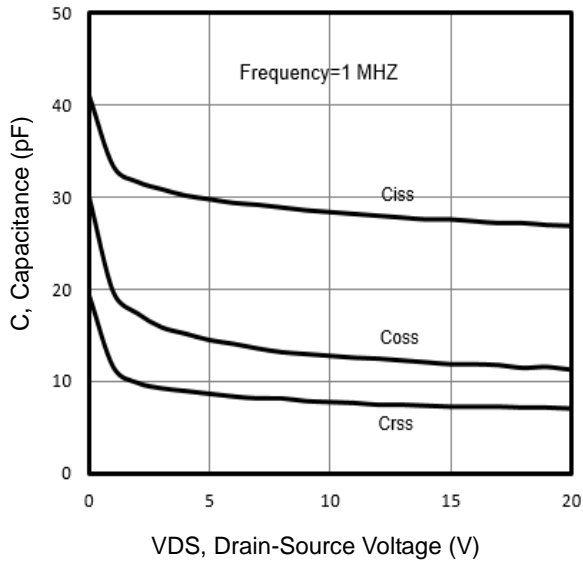


Fig7. Typical Capacitance Vs. Drain-Source Voltage

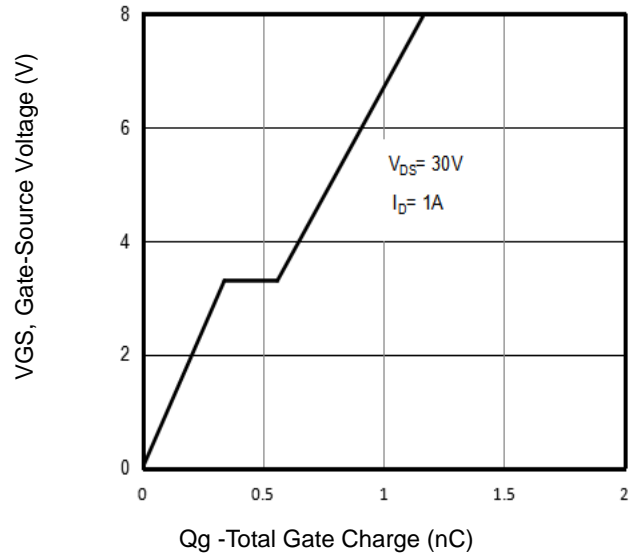


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

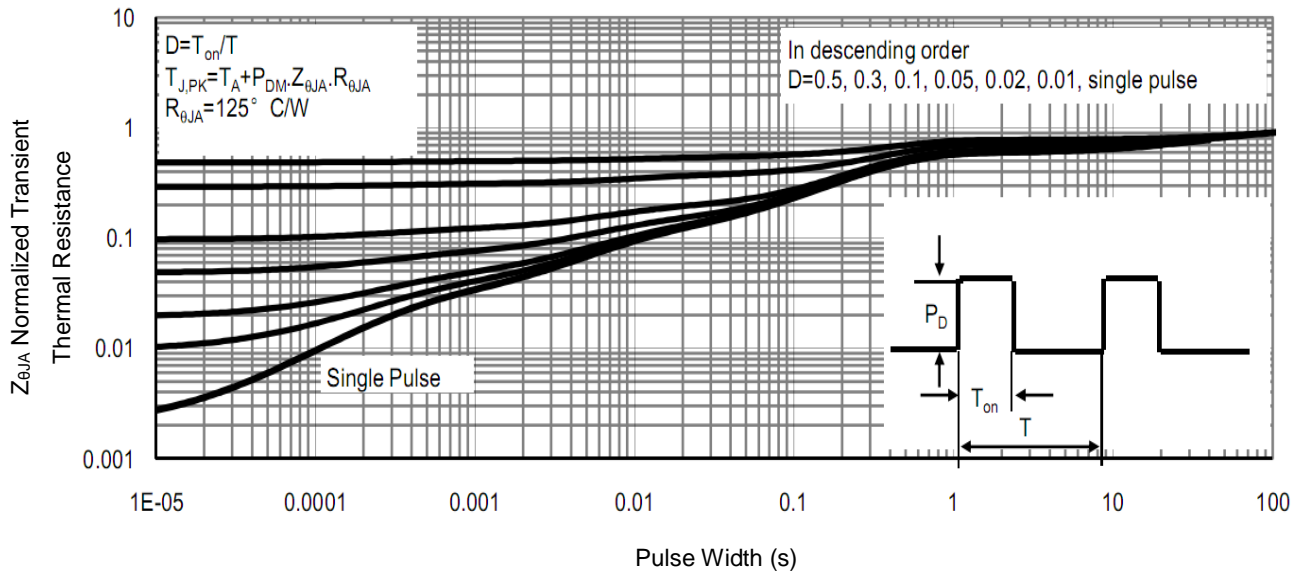


Fig9. Normalized Maximum Transient Thermal Impedance

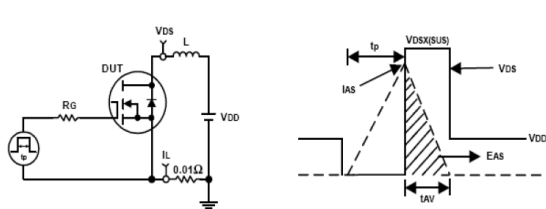


Fig10. Unclamped Inductive Test Circuit and waveforms

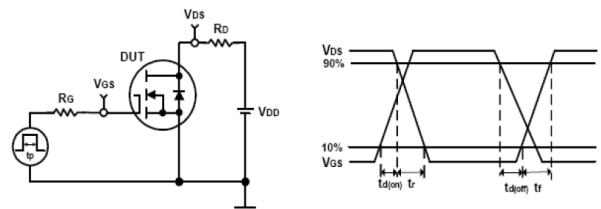
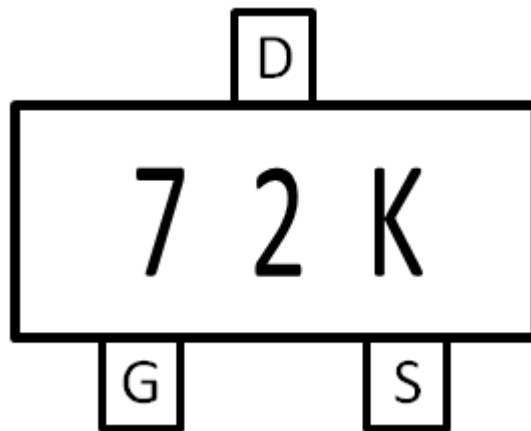


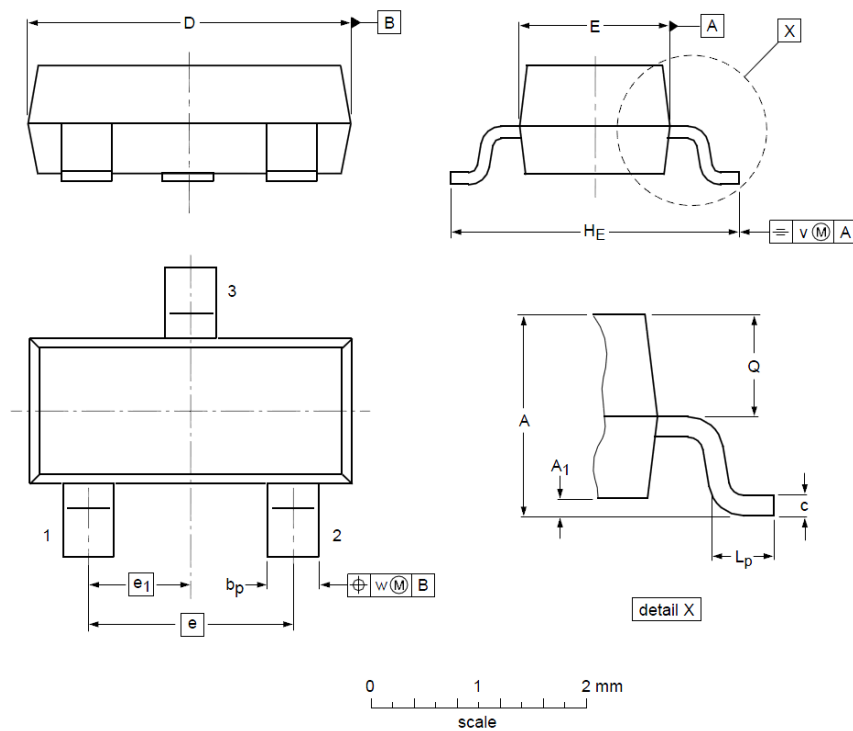
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line: Part Number (72K)

SOT23 Package Outline Data



Label	DIMENSIONS (unit: mm)		
	Min	Typ	Max
A	0.90	1.03	1.10
A ₁	0.01	0.05	0.10
b _p	0.38	0.42	0.48
c	0.09	0.13	0.15
D	2.80	2.92	3.00
E	1.20	1.33	1.40
e	--	1.90	--
e ₁	--	0.95	--
H _E	2.10	2.40	2.50
L _p	0.40	0.50	0.60
Q	0.45	0.49	0.55
v	--	0.20	--
w	--	0.10	--

Notes:

1. Follow JEDEC TO-236, variation AB.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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sales@vgsemi.com

Vanguard Semiconductor CO., LTD

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FAX: (86-755) -26907027

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