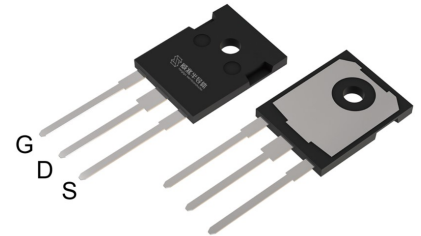


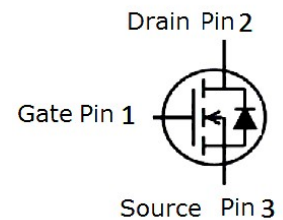
Features

- Enhancement mode
- Very Low on-resistance $R_{DS(on)}$
- Fast Switching and High efficiency
- 100% Avalanche test

V_{DS}	100	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	2.6	m Ω
I_D	320	A

TO-247


Part ID	Package Type	Marking	Packing
VS320N10AU	TO-247	320N10A	30pcs/Tube



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	100	V
V_{GS}	Gate-Source voltage	± 25	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	320 A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C = 25^\circ\text{C}$	320 A
		$T_C = 100^\circ\text{C}$	226 A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	1280 A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	23 A
		$T_A = 70^\circ\text{C}$	18 A
E_{AS}	Avalanche energy, single pulsed ②	625	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	500 W
		$T_C = 100^\circ\text{C}$	250 W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	2.5 W
		$T_A = 70^\circ\text{C}$	1.6 W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.3	0.36	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	60	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =100V, V _{GS} =0V	--	--	100	μA
IGSS	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.6	3.1	3.6	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =120A	--	2.6	3.1	mΩ
		T _j =100°C	--	3.9	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	23480	31305	41635	pF
C _{oss}	Output Capacitance		1000	1335	1775	pF
C _{rss}	Reverse Transfer Capacitance		325	430	570	pF
R _g	Gate Resistance	f=1MHz	0.2	0.7	5	Ω
Q _g	Total Gate Charge	V _{DS} =50V, I _D =80A, V _{GS} =10V	--	452	600	nC
Q _{gs}	Gate-Source Charge		--	131	174	nC
Q _{gd}	Gate-Drain Charge		--	119	179	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =80A, R _G =3Ω, V _{GS} =10V	--	77	--	ns
T _r	Turn-on Rise Time		--	142	--	ns
T _{d(off)}	Turn-Off Delay Time		--	190	--	ns
T _f	Turn-Off Fall Time		--	137	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =120A, V _{GS} =0V	--	0.9	1.2	V
T _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =80A, V _{GS} =0V	--	63	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	144	--	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L =0.5mH, R_G = 25Ω, I_{AS} =50A, V_{GS} =10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

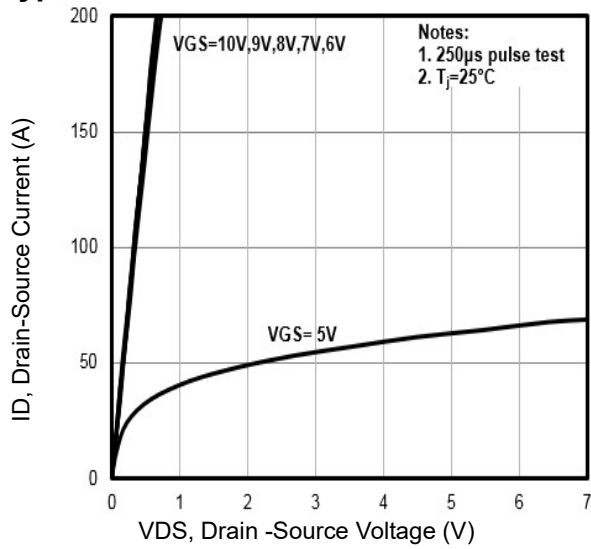


Fig1. Typical Output Characteristics

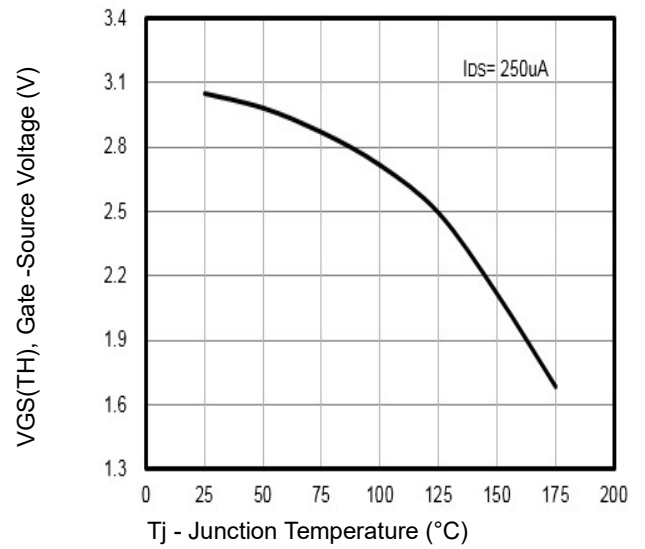


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

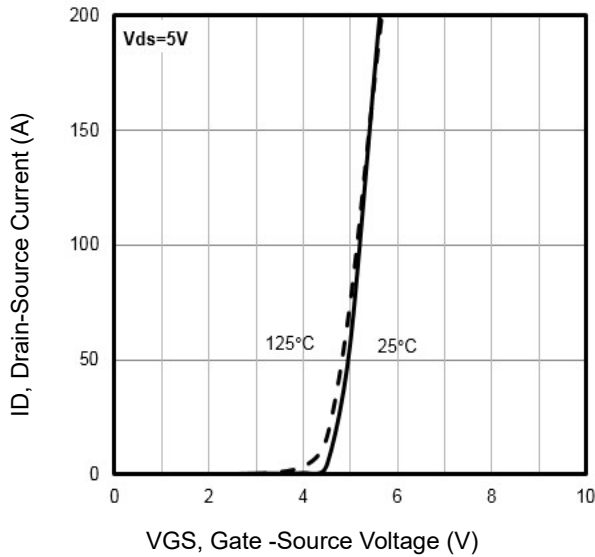


Fig3. Typical Transfer Characteristics

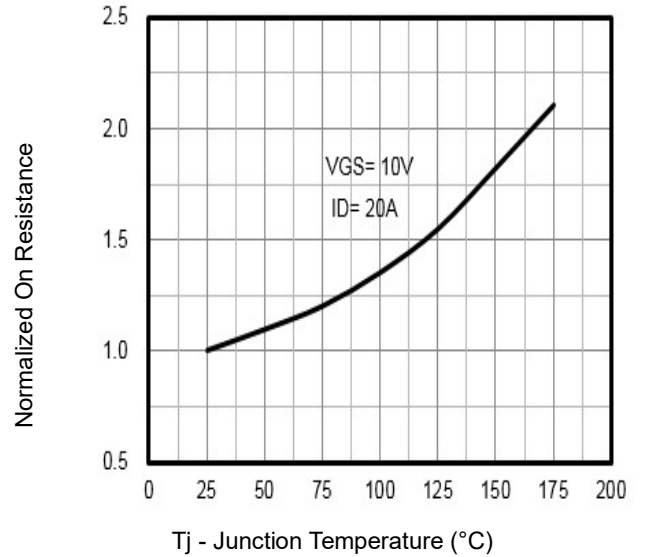


Fig4. Normalized On-Resistance Vs. T_j

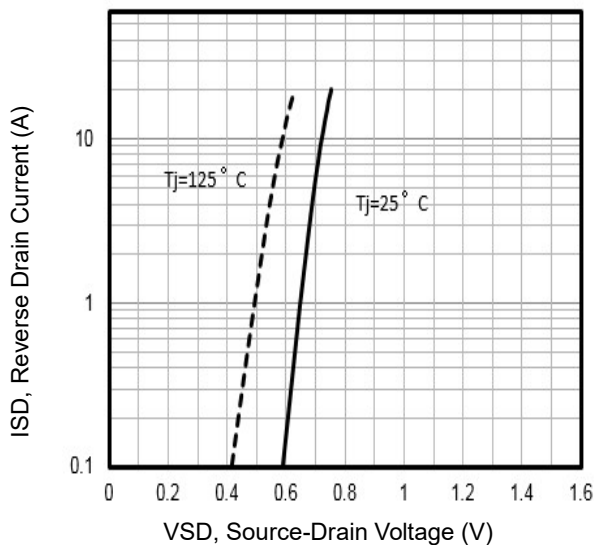


Fig5. Typical Source-Drain Diode Forward Voltage

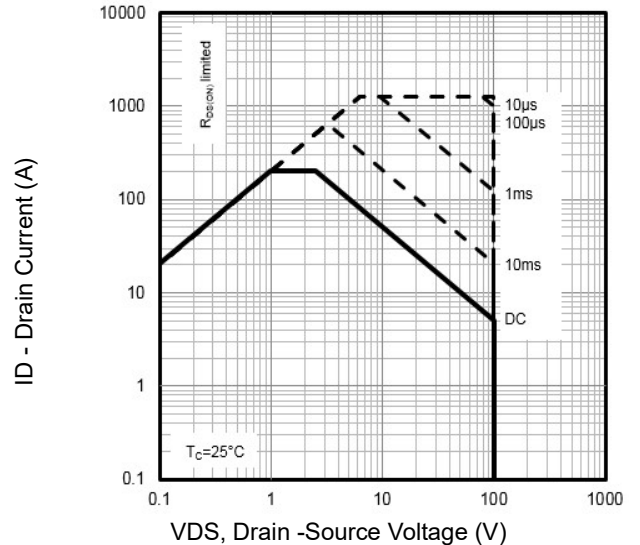


Fig6. Maximum Safe Operating Area

Typical Characteristics

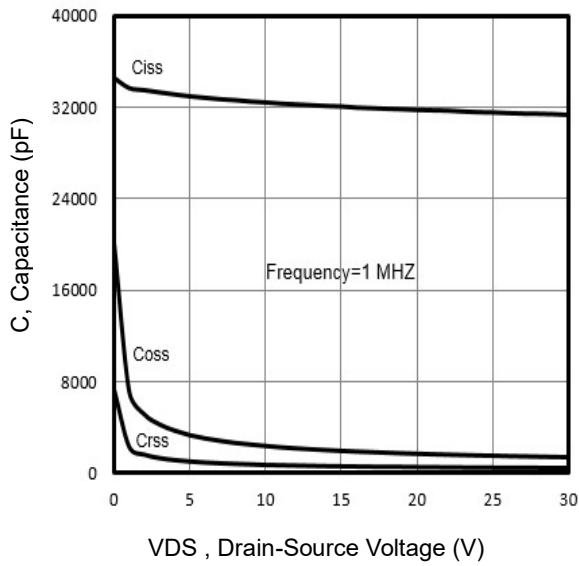


Fig7. Typical Capacitance Vs.Drain-Source Voltage

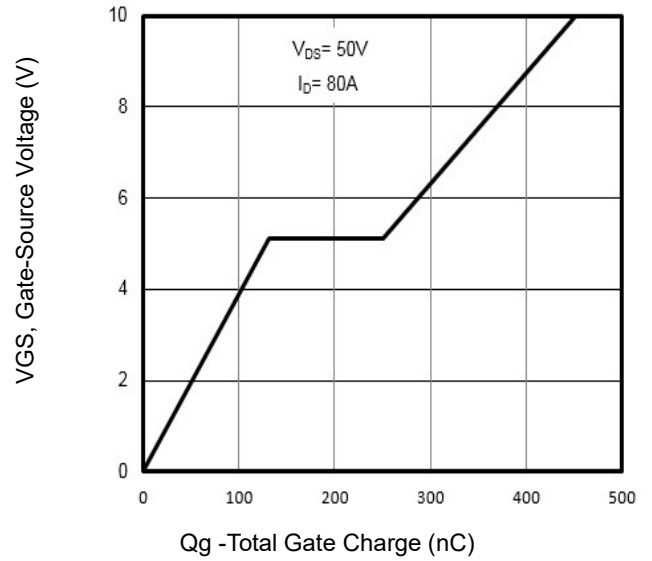


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

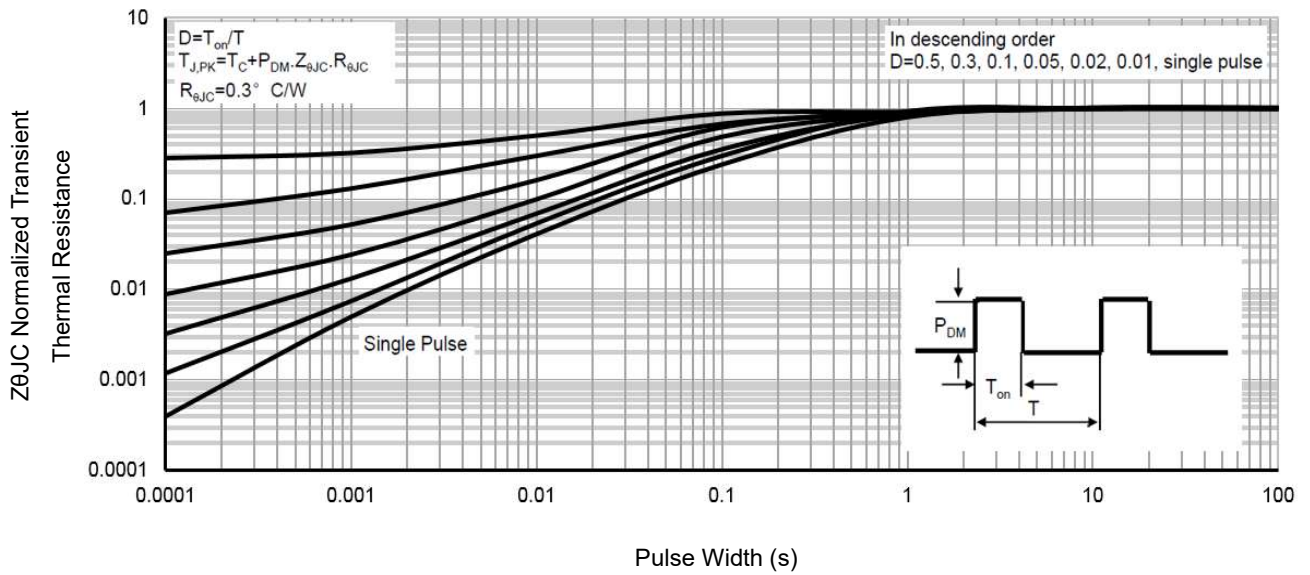


Fig9. Normalized Maximum Transient Thermal Impedance

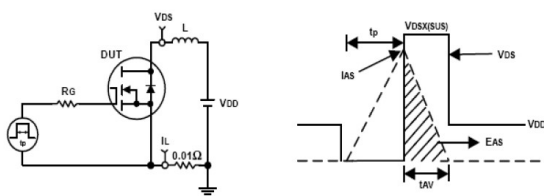


Fig10. Unclamped Inductive Test Circuit and waveforms

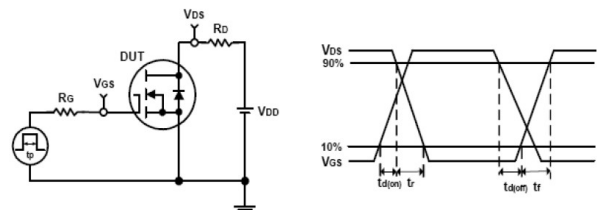
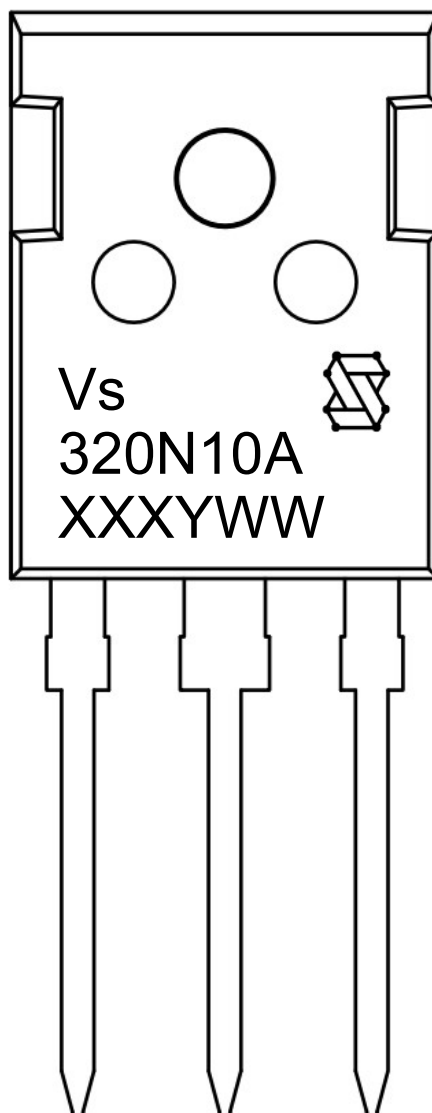


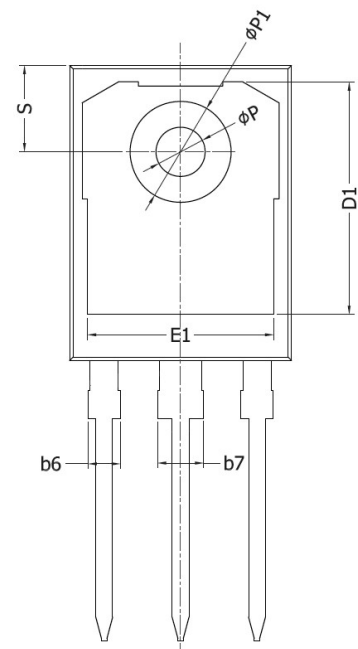
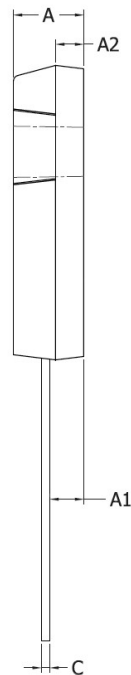
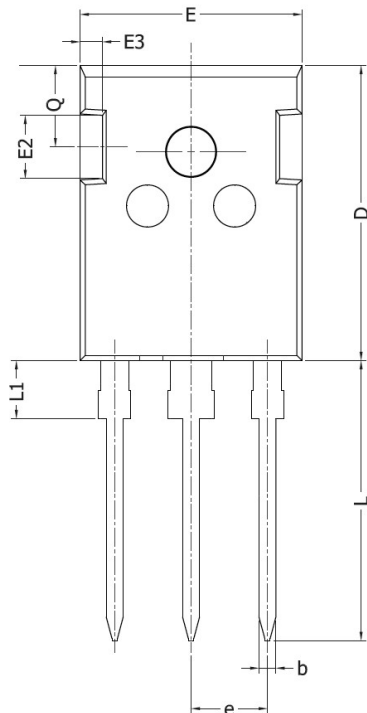
Fig11. Switching Time Test Circuit and waveforms

Marking Information



- 1st line: Vergiga Code (Vs), Vergiga Logo
- 2nd line: Part Number (320N10A)
- 3rd line: Date code (XXXYWW)
 - XXX: Wafer Lot Number Code , code changed with Lot Number
 - Y: Year Code , refer to table below
 - WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-247 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Nom	Max
A	4.80	5.00	5.20
A1	2.21	2.41	2.59
A2	1.85	2.00	2.15
b	1.11	1.21	1.36
b6	1.91	--	2.21
b7	2.91	--	3.21
C	0.51	0.61	0.75
D	20.80	21.00	21.30
D1	16.25	16.55	16.85
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.40	--	5.20
E3	1.50	1.60	1.70
e	5.44 BSC		
L	19.80	19.92	20.22
L1	--	--	4.30
ΦP	3.40	3.60	3.80
ΦP1	7.00	--	7.40
Q	5.60	5.80	6.00
S	6.05	6.15	6.25

Notes:

1. Package Reference: JEDEC TO-247, Variation AD.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side.
5. Thermal Pad Contour Optional Within Dimension D1 & E1.
6. Lead Finish Uncontrolled In L1.

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[BSS340NWH6327XTSA1](#) [MCM3400A-TP](#) [DMTH10H4M6SPS-13](#) [IRF40SC240ARMA1](#) [IPS60R1K0PFD7SAKMA1](#)
[IPS60R360PFD7SAKMA1](#) [IPS60R600PFD7SAKMA1](#)