

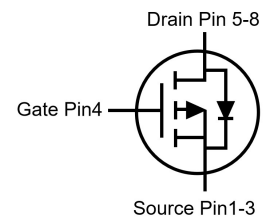
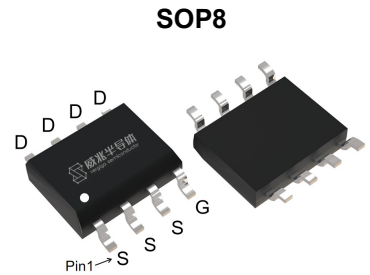
## Features

- P-Channel, -5V Logic Level Control
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=-4.5\text{ V}$
- Fast Switching
- Enhancement mode
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Packing
VS3508AS	SOP8	3508AS	3000pcs/Reel

$V_{DS}$	-30	V
$R_{DS(on),TYP}@ V_{GS}=-10\text{ V}$	8.5	m $\Omega$
$R_{DS(on),TYP}@ V_{GS}=-4.5\text{ V}$	15	m $\Omega$
$I_D$	-13	A



### Maximum ratings, at $T_A=25^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	-30	V
$I_S$	Diode continuous forward current	$T_A=25^\circ\text{C}$ -3	A
$I_D$	Continuous drain current@ $V_{GS}=-10\text{ V}$	$T_A=25^\circ\text{C}$ -13	A
		$T_A=100^\circ\text{C}$ -8.5	A
$I_{DM}$	Pulse drain current tested ①	$T_A=25^\circ\text{C}$ -52	A
EAS	Avalanche energy, single pulsed ②	81	mJ
$P_D$	Maximum power dissipation	$T_A=25^\circ\text{C}$ 3.1	W
$V_{GS}$	Gate-Source voltage	$\pm 20$	V
MSL		Level 3	
$T_{STG} T_J$	Storage and operating temperature range	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

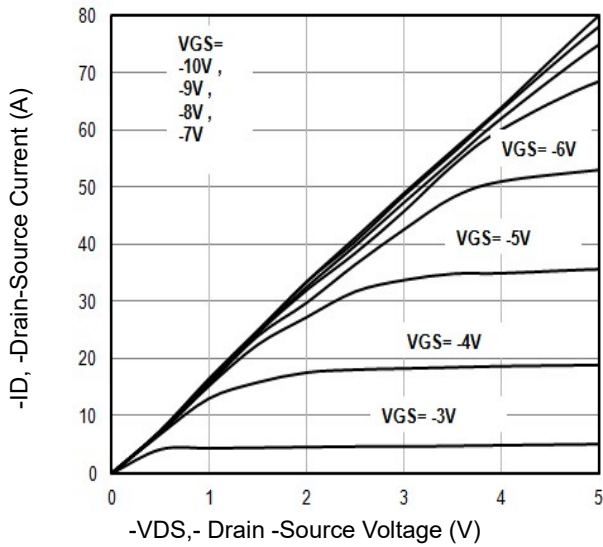
Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	24	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	40	$^\circ\text{C/W}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-30	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T <sub>j</sub> =125°C)	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	--	--	-100	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	--	--	±100	nA
V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.0	-1.8	-2.5	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance ②	V <sub>GS</sub> =-10V, I <sub>D</sub> =-10A	--	8.5	10	mΩ
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance ②	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-6A	--	15	18	mΩ
<b>Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	--	3320	--	pF
C <sub>oss</sub>	Output Capacitance		--	395	--	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	245	--	pF
R <sub>g</sub>	Gate Resistance	f=1MHz	--	2.3	--	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-15V, I <sub>D</sub> =-10A, V <sub>GS</sub> =-10V	--	39	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	7	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	11	--	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =-15V, I <sub>D</sub> =-10A, R <sub>G</sub> =6.8Ω, V <sub>GS</sub> =-10V	--	15	--	ns
t <sub>r</sub>	Turn-on Rise Time		--	33	--	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	67	--	ns
t <sub>f</sub>	Turn-Off Fall Time		--	21	--	ns
<b>Source- Drain Diode Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
V <sub>SD</sub>	Forward on voltage	I <sub>SD</sub> =-10A, V <sub>GS</sub> =0V	--	-0.83	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	T <sub>j</sub> =25°C, I <sub>sd</sub> =-10A, V <sub>GS</sub> =0V	--	29	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		di/dt=-100A/μs	--	144	--

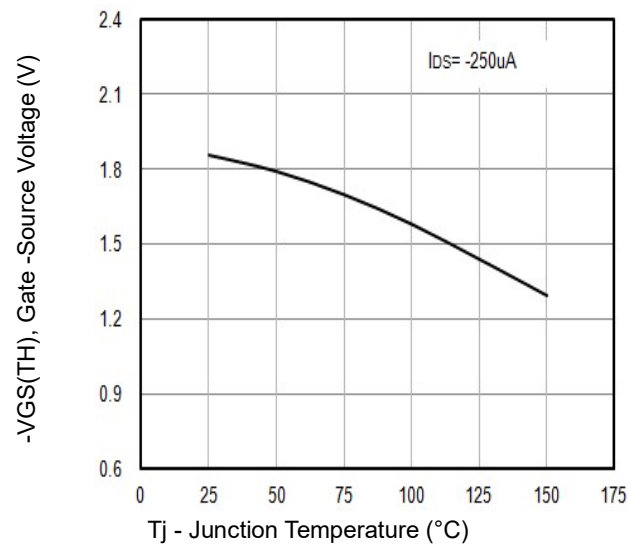
**NOTE:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>jmax</sub>, starting T<sub>j</sub> = 25°C, L = 0.5mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = -18A, V<sub>GS</sub> = -10V. Part not recommended for use above this value
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

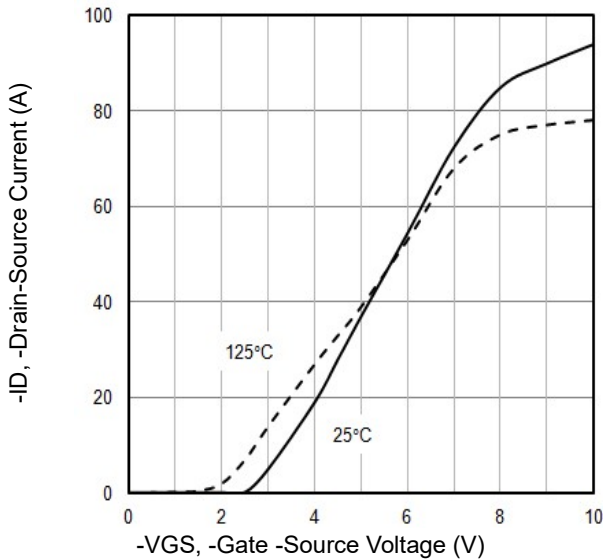
**Typical Characteristics**



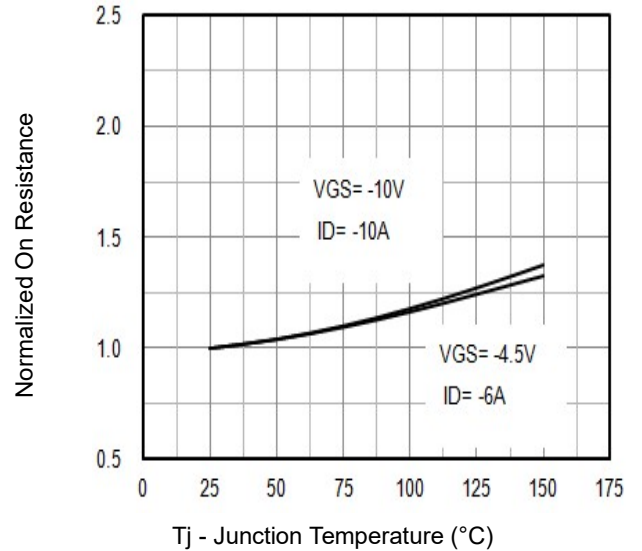
**Fig1.** Typical Output Characteristics



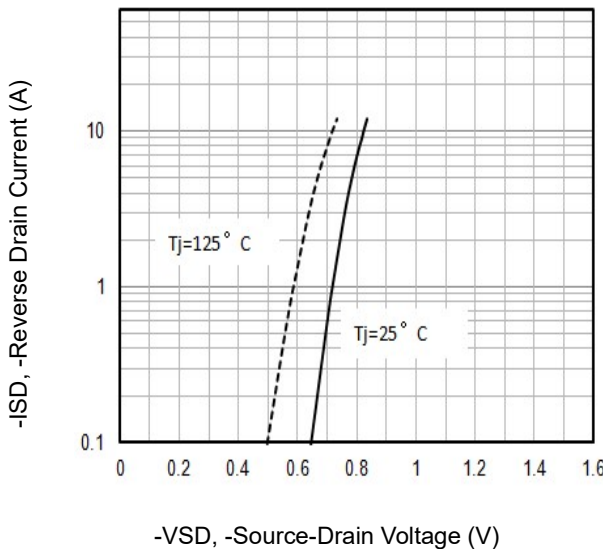
**Fig2.**  $-V_{GS(TH)}$  Gate -Source Voltage Vs.  $T_j$



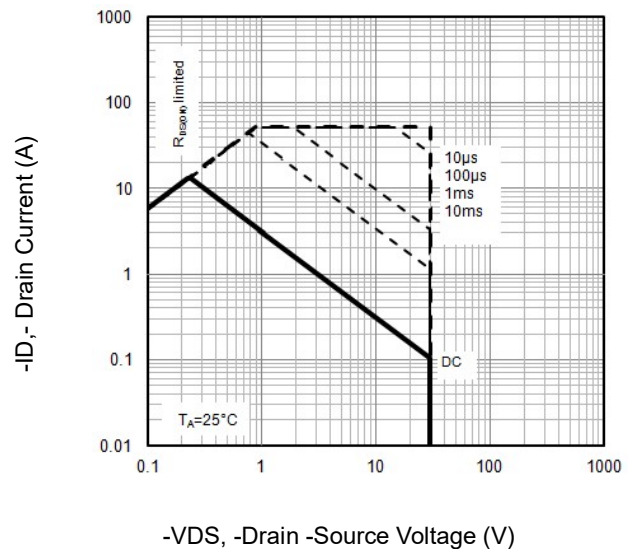
**Fig3.** Typical Transfer Characteristics



**Fig4.** Normalized On-Resistance Vs.  $T_j$

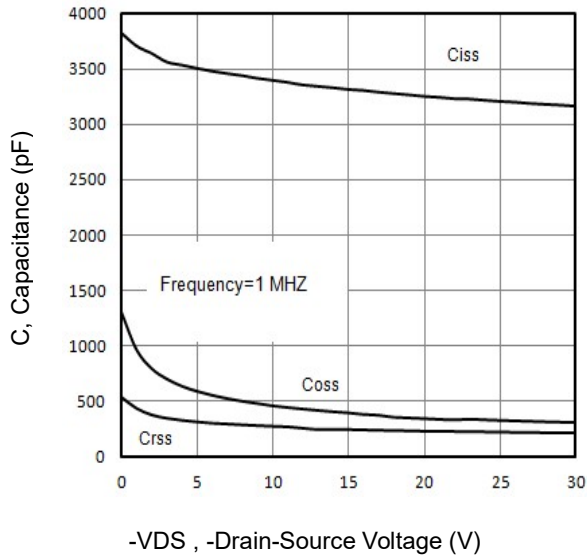


**Fig5.** Typical Source-Drain Diode Forward Voltage

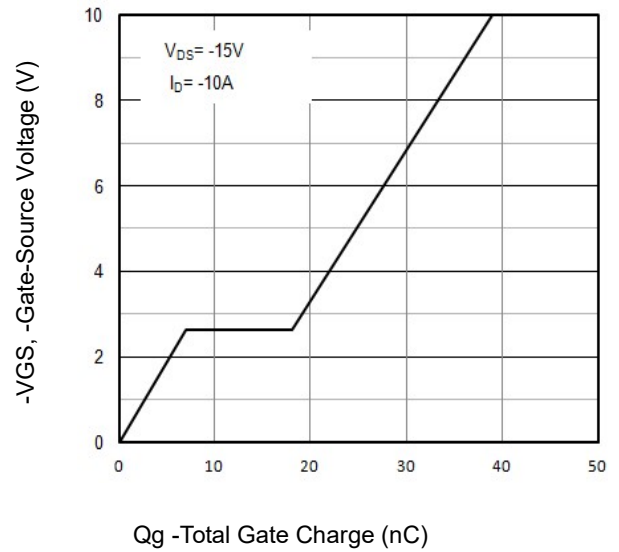


**Fig6.** Maximum Safe Operating Area

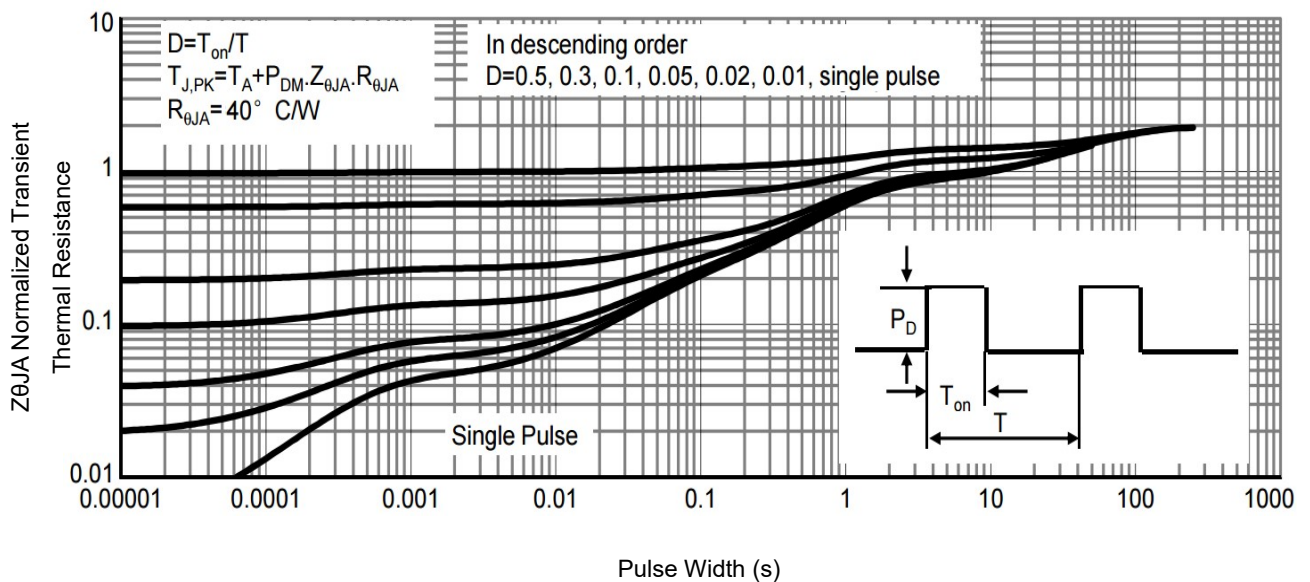
**Typical Characteristics**



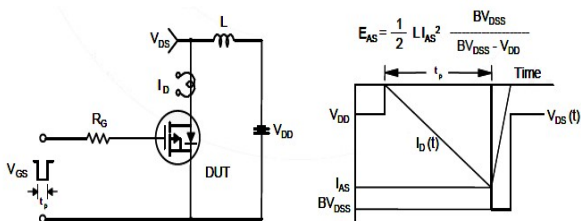
**Fig7.** Typical Capacitance Vs.Drain-Source Voltage



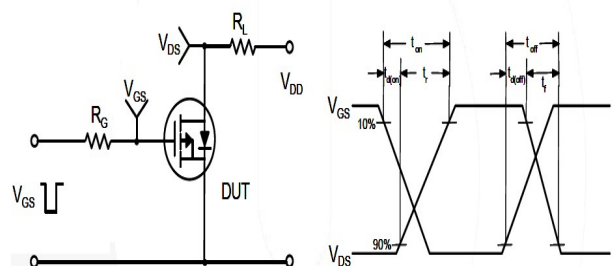
**Fig8.** Typical Gate Charge Vs.Gate-Source Voltage



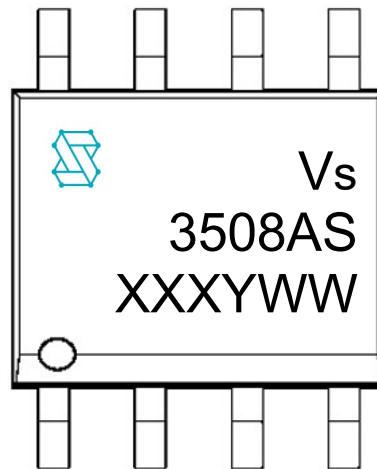
**Fig9.** Normalized Maximum Transient Thermal Impedance



**Fig10.** Unclamped Inductive Test Circuit and Waveforms



**Fig11.** Switching Time Test Circuit and waveforms

**Marking Information**


1<sup>st</sup> line: Vergiga Code (Vs), Vergiga Logo

2<sup>nd</sup> line: Part Number (3508AS)

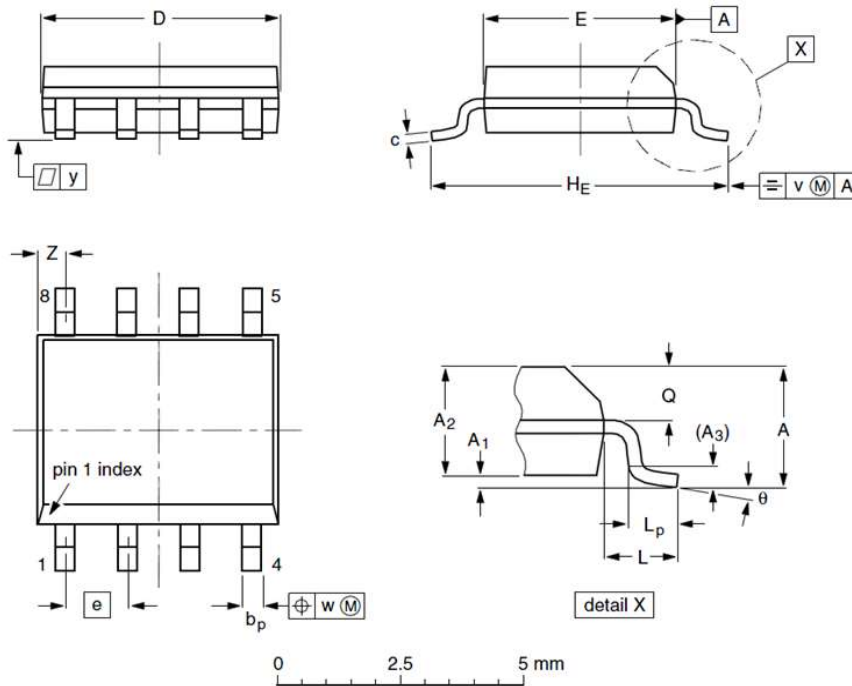
3<sup>rd</sup> line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code , refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

**SOP8 Package Outline Data**


Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A <sub>1</sub>	0.10	0.18	0.25
A <sub>2</sub>	1.25	1.35	1.50
A <sub>3</sub>	--	0.25	--
b <sub>p</sub>	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H <sub>E</sub>	5.80	6.00	6.20
L	--	1.05	--
L <sub>p</sub>	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

**Notes:**

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "b<sub>p</sub>" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "b<sub>p</sub>" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

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