

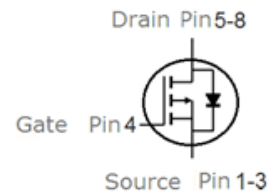
Features

- P-Channel, -5V Logic Level Control
- Low on-resistance RDS(on) @ VGS=-4.5 V
- Fast Switching and High efficiency
- Enhancement mode
- Pb-free lead plating; RoHS compliant

V_{DS}	-30	V
$R_{DS(on),TYP} @ V_{GS}=-10\text{ V}$	15	mΩ
$R_{DS(on),TYP} @ V_{GS}=-4.5\text{ V}$	23	mΩ
I_D	-35	A

PDFN3333


Part ID	Package Type	Marking	Tape and reel information
VS3518AE	PDFN3333	3518AE	5000pcs/Reel



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	-30	V
V _{GS}	Gate-Source voltage	±25	V
I _S	Diode continuous forward current	T _C =25°C	-35 A
I _D	Continuous drain current @VGS=-10V	T _C =25°C	-35 A
		T _C =100°C	-22 A
I _{DM}	Pulse drain current tested ①	T _C =25°C	-140 A
I _{DSM}	Continuous drain current @VGS=-10V	T _A =25°C	-12 A
		T _A =70°C	-10 A
EAS	Avalanche energy, single pulsed ②	49	mJ
P _D	Maximum power dissipation	T _C =25°C	30 W
		T _C =100°C	12 W
P _{DSM}	Maximum power dissipation ③	T _A =25°C	3.5 W
		T _A =70°C	2.3 W
T _{STG} , T _J	Storage and junction temperature range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	4.1	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	35	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =-30V, V _{GS} =0V	--	--	-100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.2	-1.6	-2.3	V
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-10V, I _D =-15A	--	15	22	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance ④	V _{GS} =-4.5V, I _D =-10A	--	23	39	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	800	1315	1800	pF
C _{oss}	Output Capacitance		100	190	280	pF
C _{rss}	Reverse Transfer Capacitance		70	135	200	pF
R _g	Gate Resistance	f=1MHz	--	10.8	--	Ω
Q _g	Total Gate Charge	V _{DS} =-15V, I _D =-15A, V _{GS} =-10V	--	30	--	nC
Q _{gs}	Gate-Source Charge		--	4.5	--	nC
Q _{gd}	Gate-Drain Charge		--	6	--	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-15V, I _D =-15A, R _G =3Ω, V _{GS} =-10V	--	9	--	ns
t _r	Turn-on Rise Time		--	8	--	ns
t _{d(off)}	Turn-Off Delay Time		--	192	--	ns
t _f	Turn-Off Fall Time		--	62	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =-15A, V _{GS} =0V	--	-0.9	-1.2	V
t _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =-15A, V _{GS} =0V	--	22	--	ns
Q _{rr}	Reverse Recovery Charge	di/dt=-100A/μs	--	8	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -11A, V_{GS} = -10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

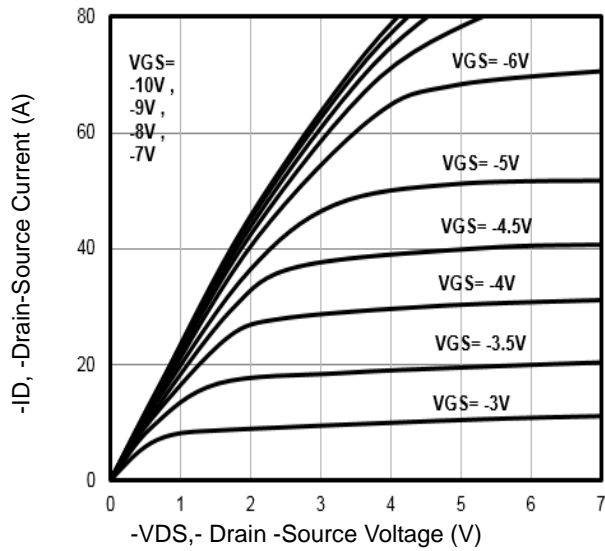


Fig1. Typical Output Characteristics

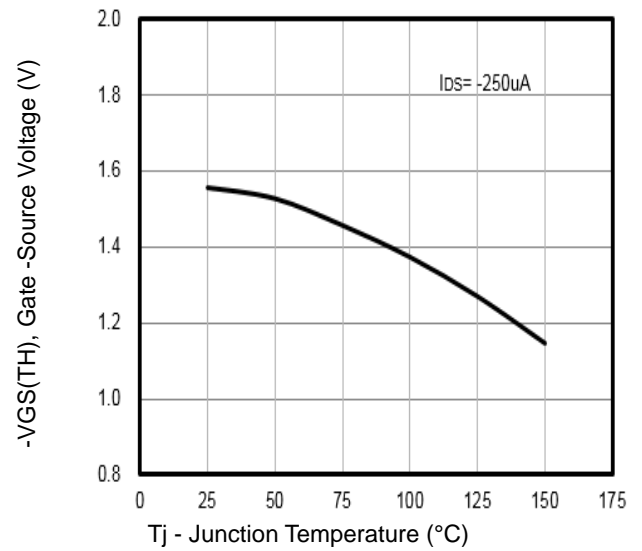


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

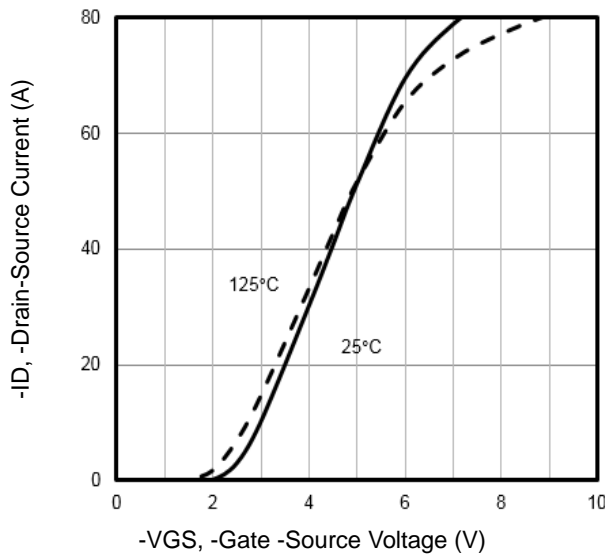


Fig3. Typical Transfer Characteristics

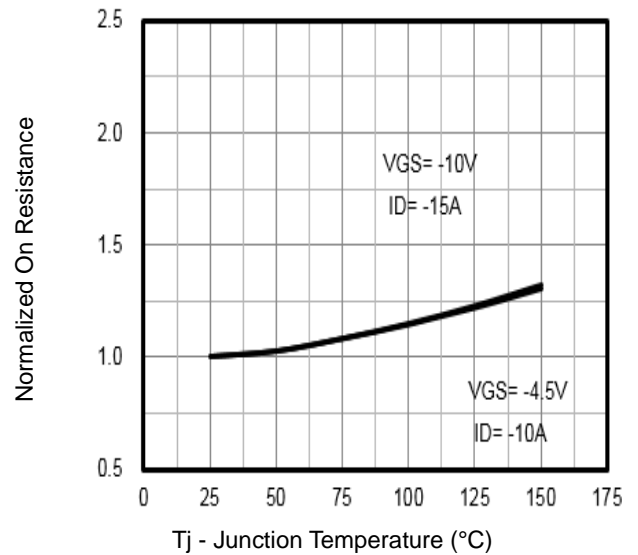


Fig4. Normalized On-Resistance Vs. T_j

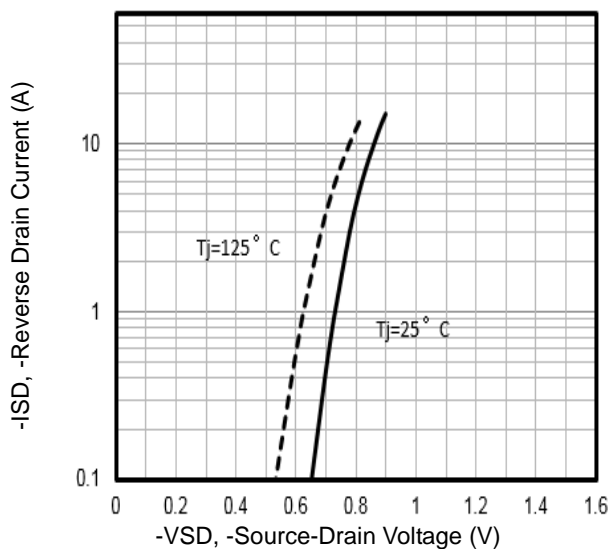


Fig5. Typical Source-Drain Diode Forward Voltage

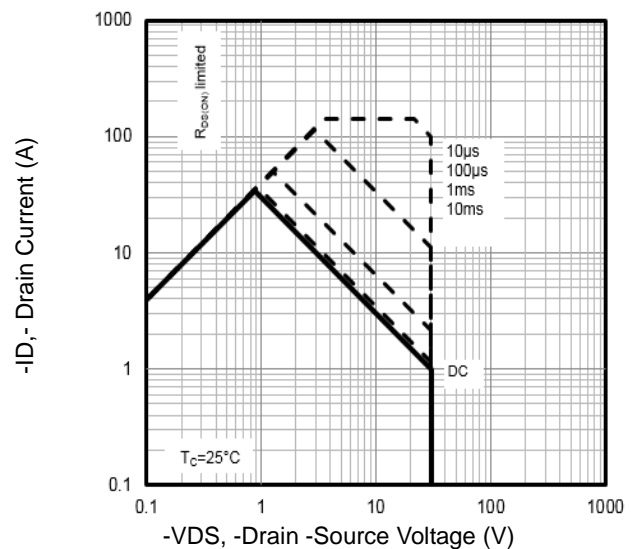


Fig6. Maximum Safe Operating Area

Typical Characteristics

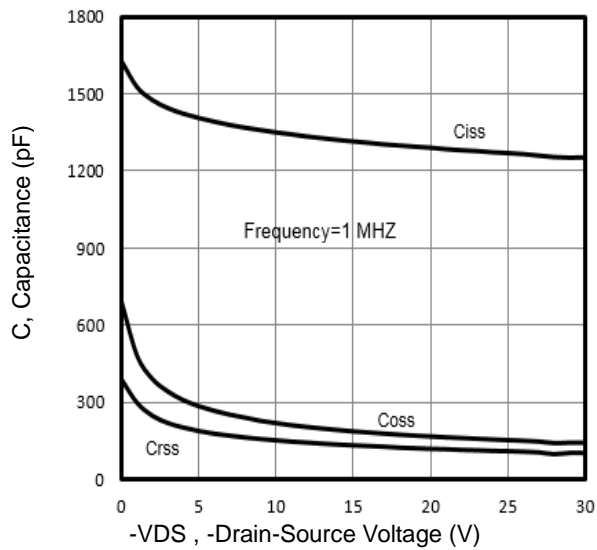


Fig7. Typical Capacitance Vs.Drain-Source Voltage

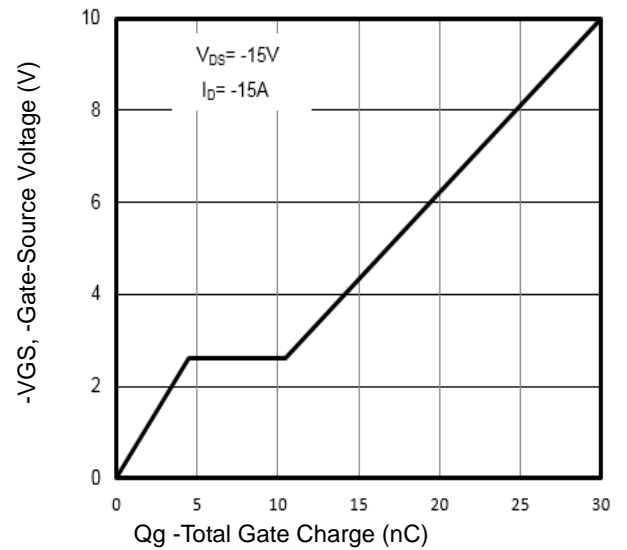


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

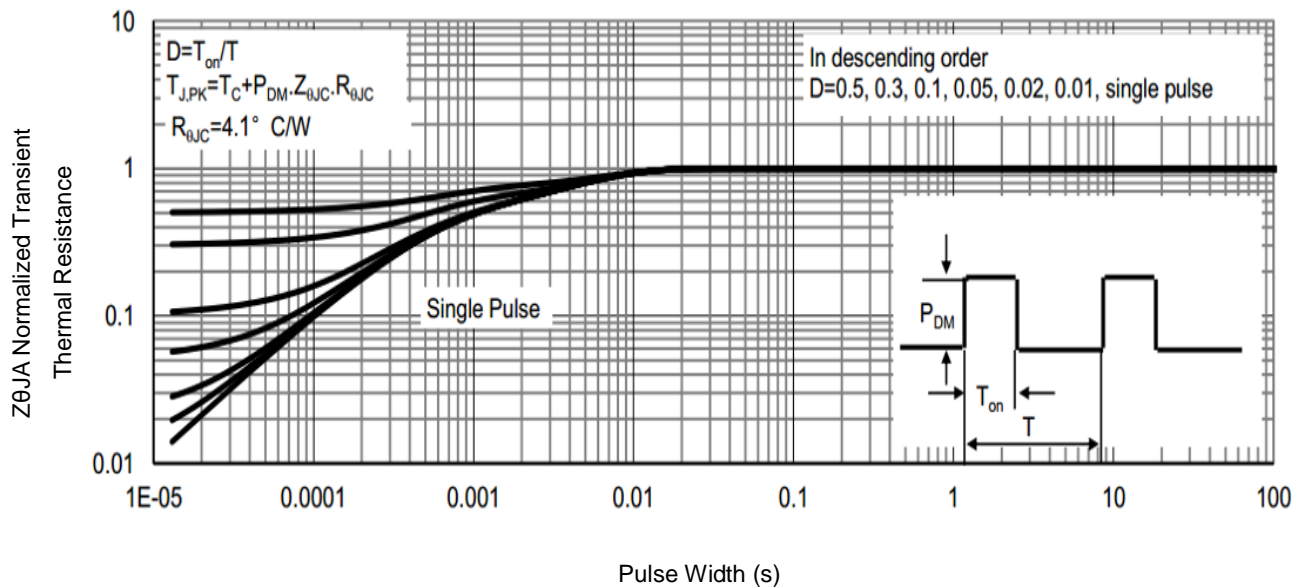


Fig9. Normalized Maximum Transient Thermal Impedance

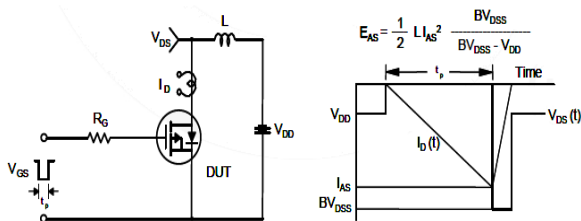


Fig10. Unclamped Inductive Test Circuit and Waveforms

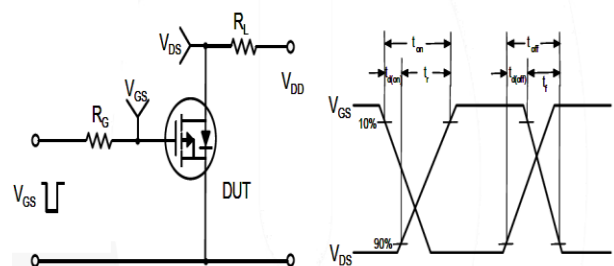
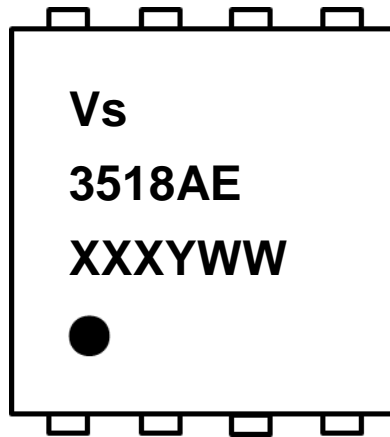


Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vanguard Code (Vs)

2nd line: Part Number (3518AE)

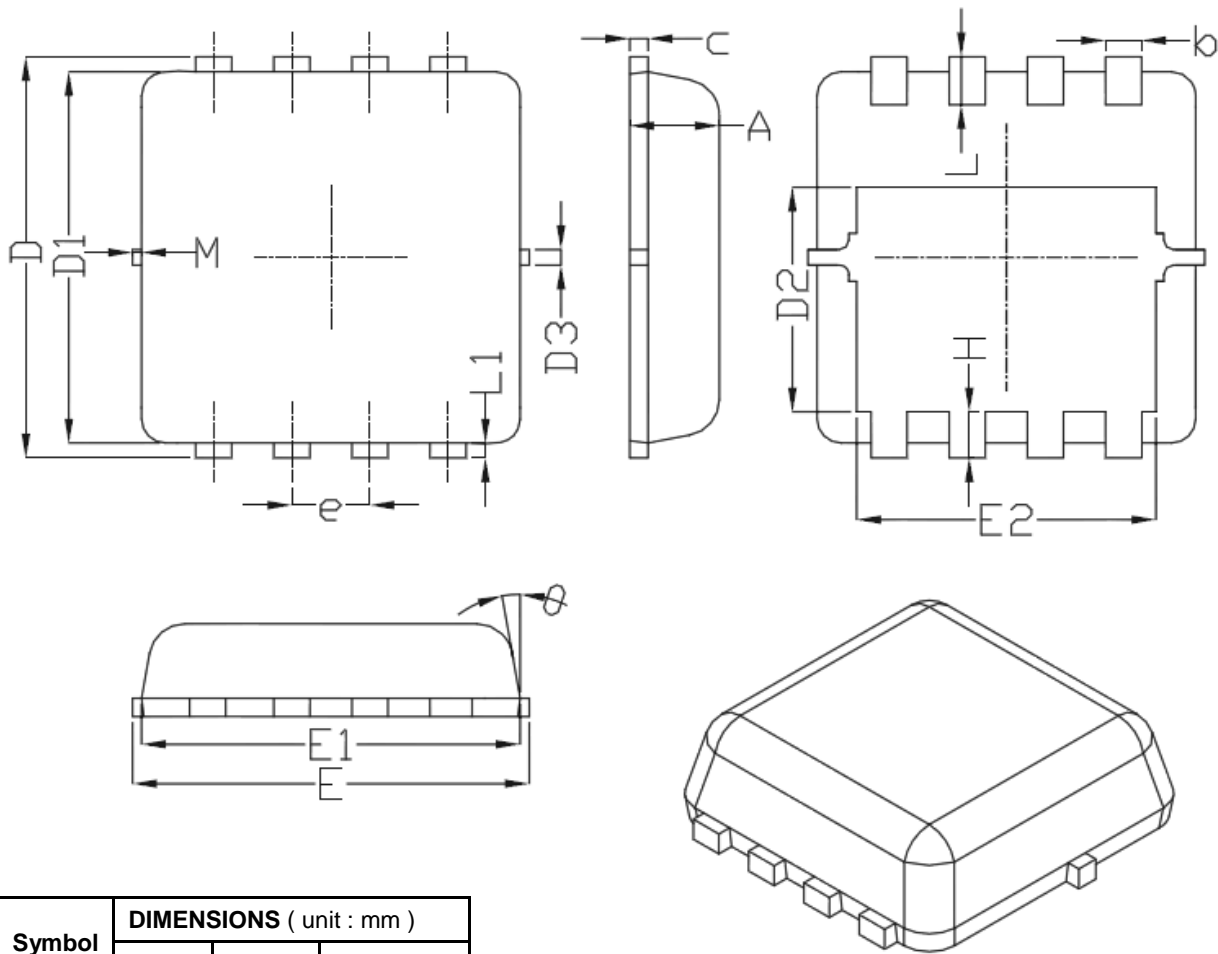
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number

Y: Year Code, e.g. E means 2017

WW: Week Code

PDFN3333 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.7	0.75	0.8
b	0.25	0.3	0.35
C	0.1	0.15	0.25
D	3.25	3.35	3.45
D1	3	3.1	3.2
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.2	3.3	3.4
E1	3	3.15	3.2
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.3	0.39	0.5
L	0.3	0.4	0.5
L1	--	0.13	--
θ	--	10°	12°
M	*	*	0.15
* Not specified			

Notes:

1. Follow JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

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