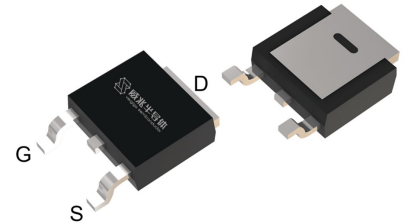


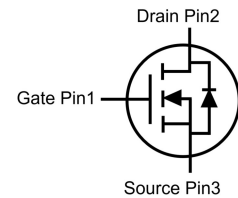
Features

- Enhancement mode
- Very low on-resistance
- Fast Switching and High efficiency
- 100% Avalanche Tested

V_{DS}	40	V
$R_{DS(on),TYP@ V_{GS}=10V}$	3.8	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	4.6	mΩ
$I_D(\text{Silicon Limited})$	165	A
$I_D(\text{Package Limited})$	80	A

TO-252


Part ID	Package Type	Marking	Packing
VS40200AD	TO-252	40200AD	2500pcs/Reel



Maximum ratings, at $T_A=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V
V_{GS}	Gate-Source voltage	± 20	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	165 A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 25^\circ\text{C}$	165 A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 100^\circ\text{C}$	117 A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	80 A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	470 A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	14 A
		$T_A = 70^\circ\text{C}$	11 A
E_{AS}	Avalanche energy, single pulsed ②	225	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	250 W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	1.7 W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	60	72	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =40V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.7	2.3	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =40A	--	3.8	4.9	mΩ
		(T _j =100°C)	--	4.9	--	mΩ
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =40A	--	4.6	6	mΩ
Dynamic Electrical Characteristics @ T_j= 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	3105	6210	10870	pF
C _{oss}	Output Capacitance		280	565	990	pF
C _{rss}	Reverse Transfer Capacitance		190	380	665	pF
R _g	Gate Resistance	f=1MHz	0.2	0.9	5	Ω
Q _{g(10V)}	Total Gate Charge	V _{DS} =20V, I _D =40A, V _{GS} =10V	--	101	177	nC
Q _{g(4.5V)}	Total Gate Charge		--	49	86	nC
Q _{gs}	Gate-Source Charge		--	19	33	nC
Q _{gd}	Gate-Drain Charge		--	20	35	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =40A, R _G =3Ω, V _{GS} =10V	--	14	--	ns
T _r	Turn-on Rise Time		--	80	--	ns
T _{d(off)}	Turn-Off Delay Time		--	61	--	ns
T _f	Turn-Off Fall Time		--	39	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A, V _{GS} =0V	--	0.9	1.2	V
T _{rr}	Reverse Recovery Time	I _{sd} =40A, V _{GS} =0V	--	25	50	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	17	34	nC

NOTE:

- ① Single pulse; pulse width ≤ 100μs.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 30A, V_{GS} = 10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

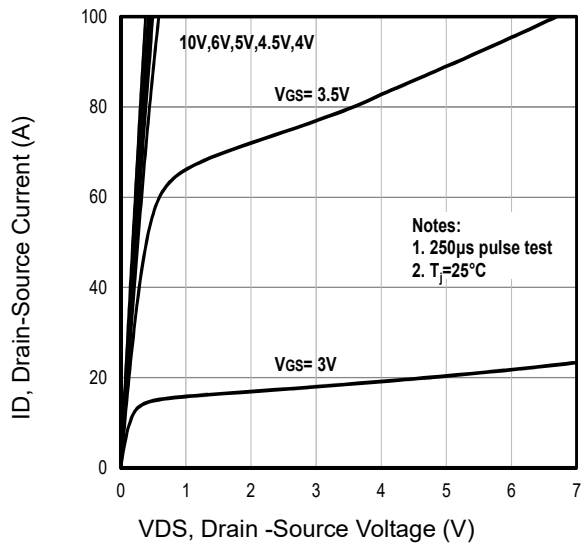


Fig1. Typical Output Characteristics

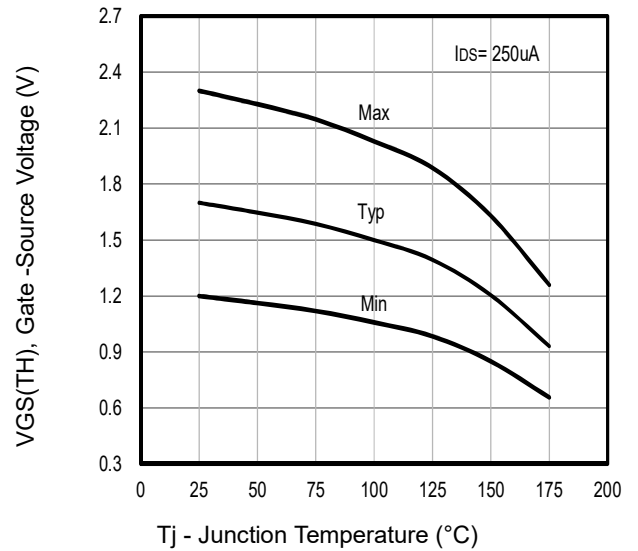


Fig2. Typical VGS(TH) Gate-Source Voltage Vs. Tj

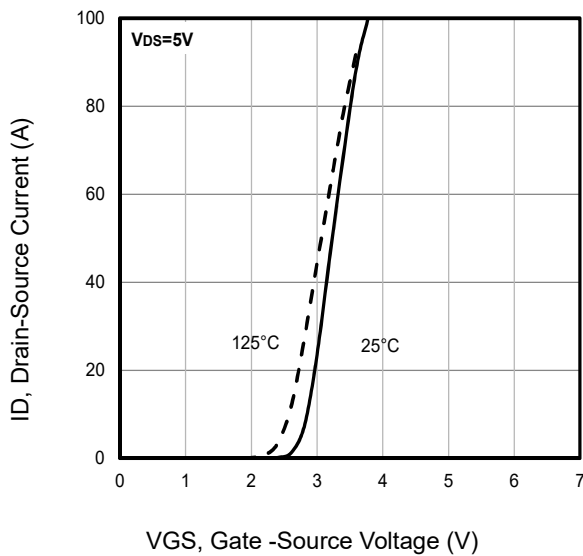


Fig3. Typical Transfer Characteristics

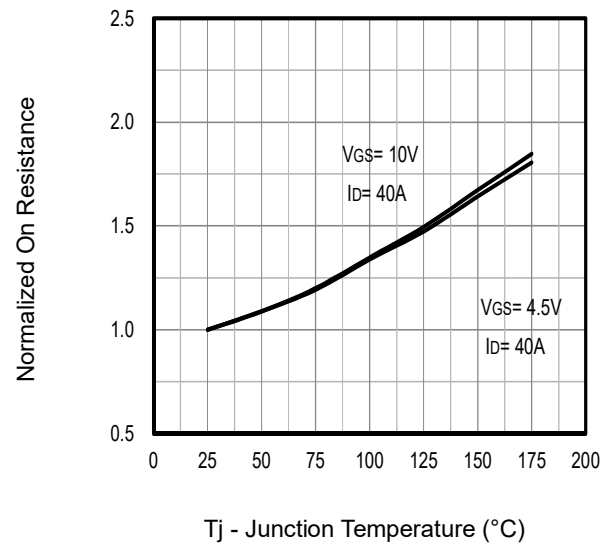


Fig4. Typical Normalized On-Resistance Vs. Tj

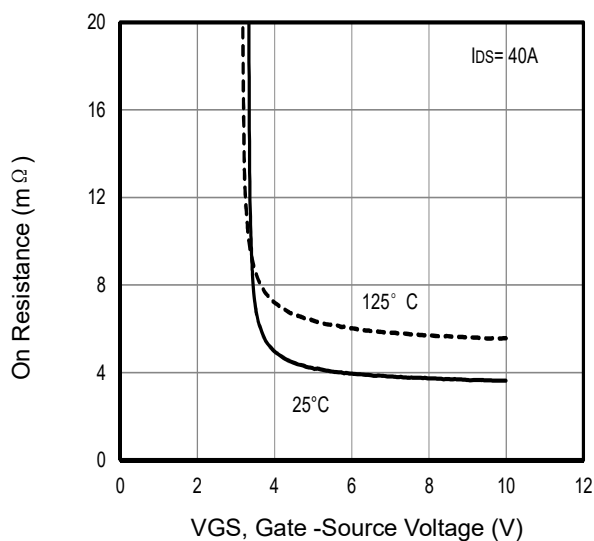


Fig5. Typical On Resistance Vs Gate-Source Voltage

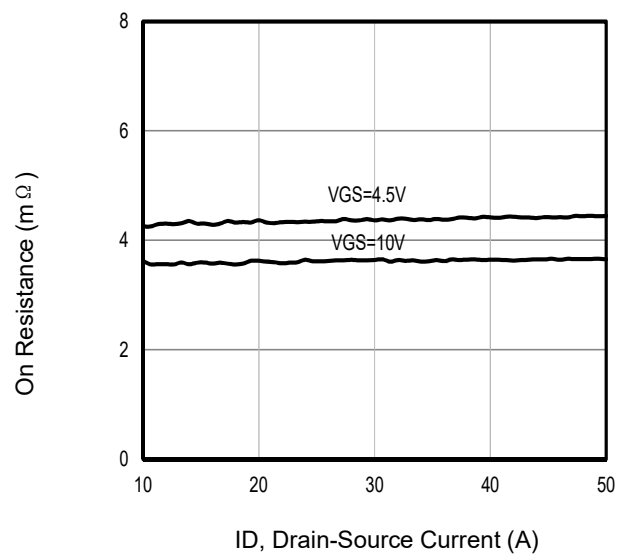


Fig6. Typical On Resistance Vs Drain Current and Gate Voltage

Typical Characteristics

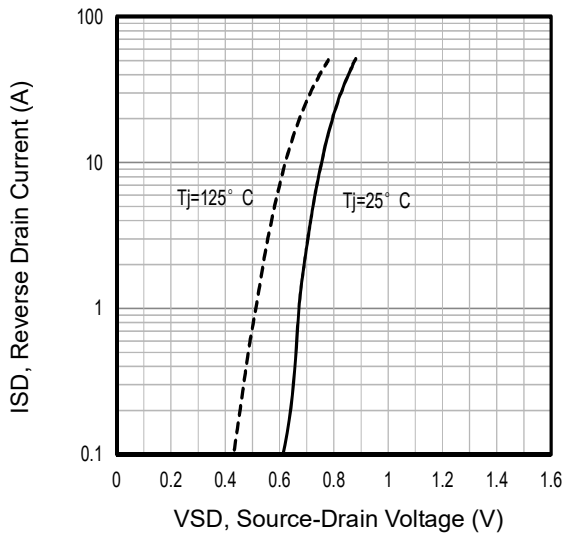


Fig7. Typical Source-Drain Diode Forward Voltage

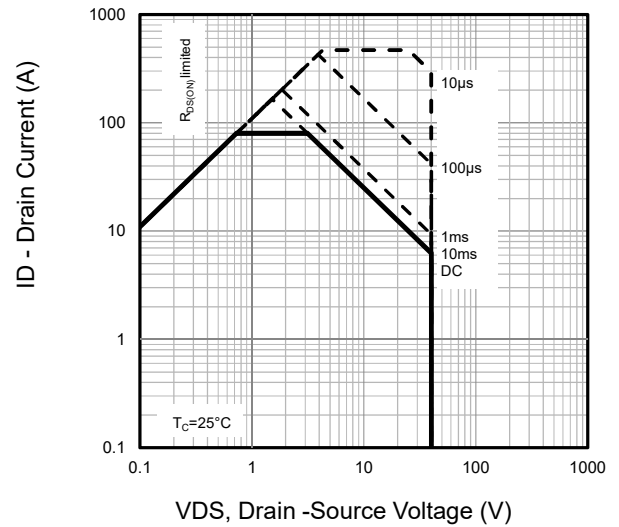


Fig8. Maximum Safe Operating Area

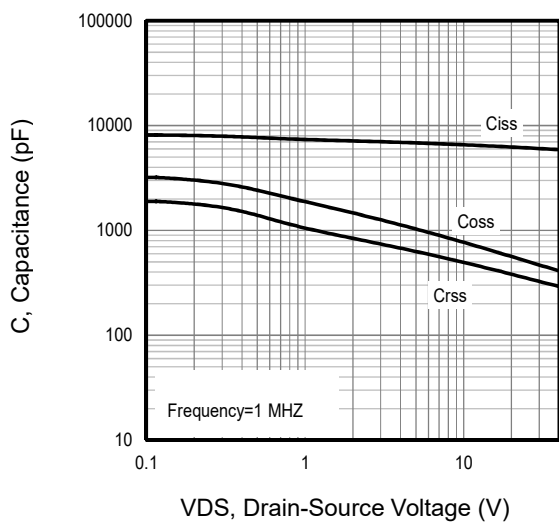


Fig9. Typical Capacitance Vs. Drain-Source Voltage

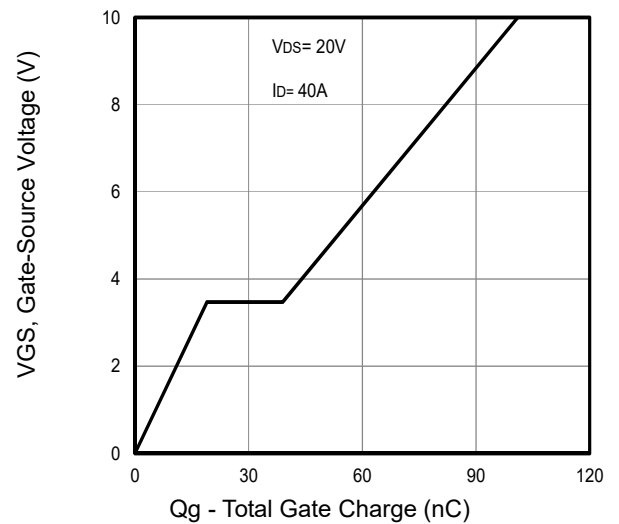


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

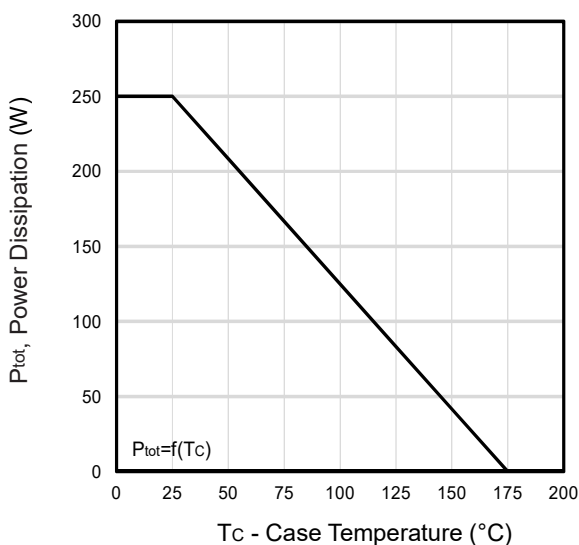


Fig11. Power Dissipation Vs. Case Temperature

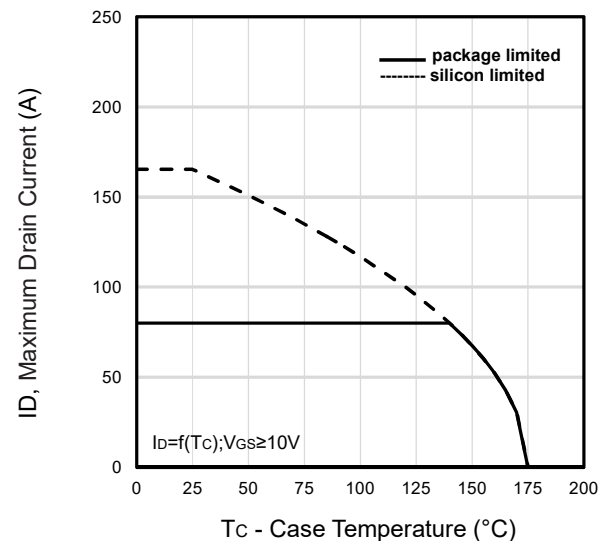


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

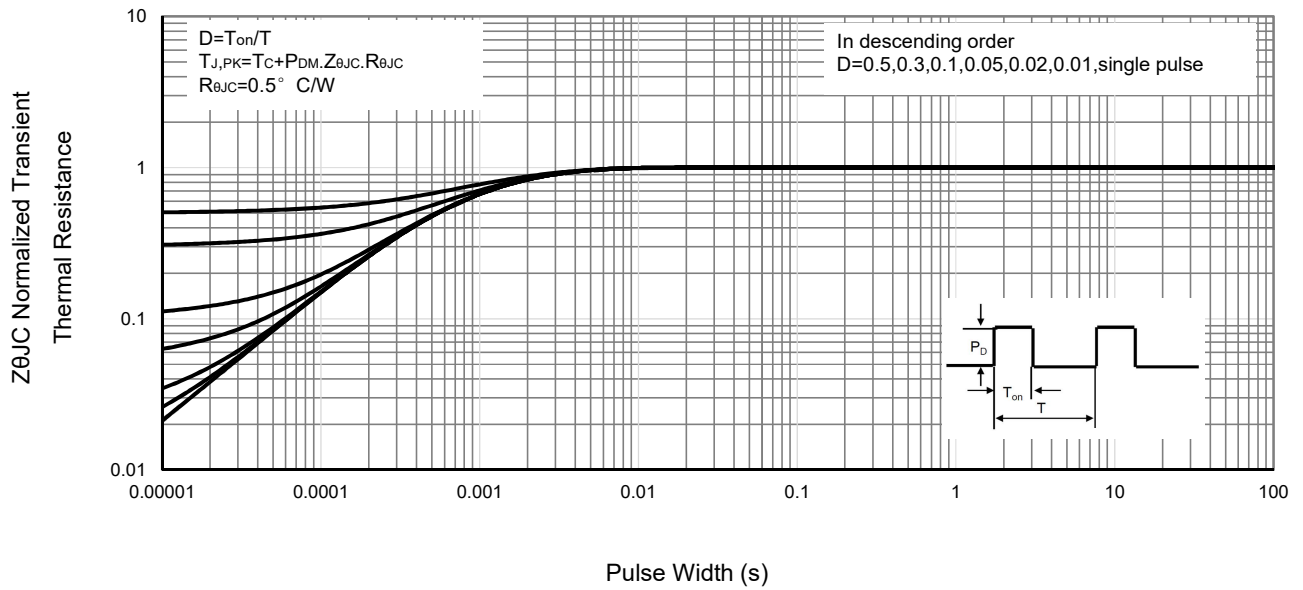


Fig13 . Normalized Maximum Transient Thermal Impedance

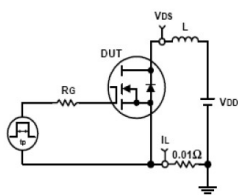


Fig14. Unclamped Inductive Test Circuit and waveforms

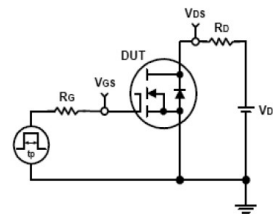
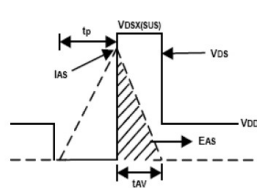
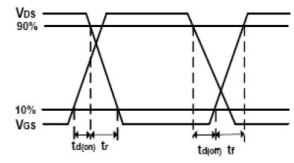
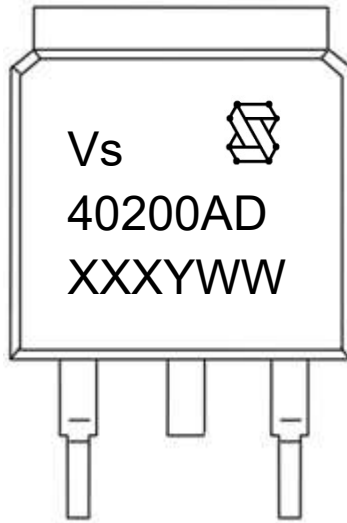


Fig15. Switching Time Test Circuit and waveforms



Marking Information


1st line: Vergiga Code (Vs) Vergiga Logo

2nd line: Part Number (40200AD)

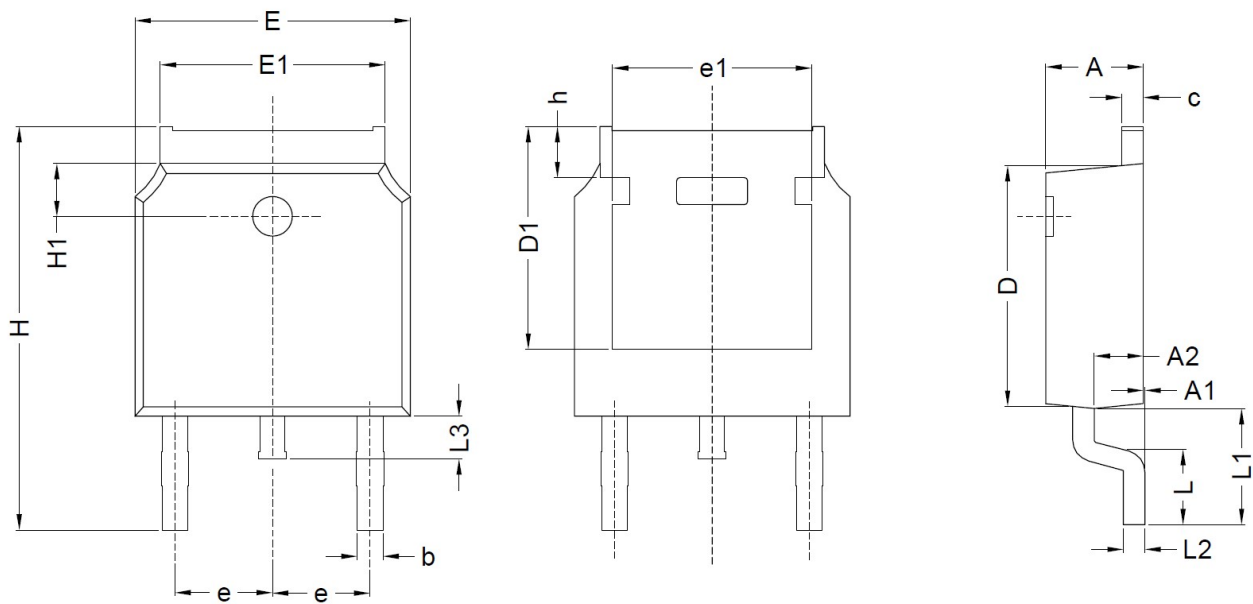
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-252 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.40
A1	--	--	0.20
A2	0.97	1.02	1.17
b	0.60	--	0.90
c	0.43	--	0.61
D	5.98	6.10	6.22
D1	5.15	5.25	5.35
E	6.40	6.60	6.73
E1	5.18	5.33	5.49
e	2.286 BSC		
e1	4.63	--	4.85
H	9.40	10.00	10.50
H1	1.50	--	1.95
h	0.88	--	1.35
L	1.38	1.50	1.75
L1	2.90 REF		
L2	0.51 BSC		
L3	0.50	--	1.00

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

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[BSS340NWH6327XTSA1](#) [MCM3400A-TP](#) [DMTH10H4M6SPS-13](#) [IRF40SC240ARMA1](#) [IPS60R1K0PFD7SAKMA1](#)
[IPS60R360PFD7SAKMA1](#) [IPS60R600PFD7SAKMA1](#)