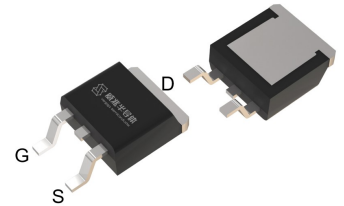


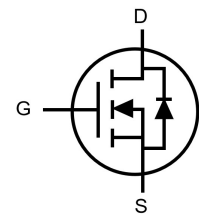
Features

- Enhancement mode
- Very low on-resistance
- Fast Switching and High efficiency
- 100% Avalanche test

V_{DS}	40	V
$R_{DS(on),TYP@ V_{GS}=10V}$	3.5	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	4.3	mΩ
$I_D(\text{Silicon Limited})$	226	A
$I_D(\text{Package Limited})$	120	A

TO-263


Part ID	Package Type	Marking	Packing
VS40200ATD	TO-263	40200ATD	800pcs/Reel



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	40	V
VGS	Gate-Source voltage	±20	V
IS	Diode continuous forward current	$T_C = 25^\circ\text{C}$	226 A
ID	Continuous drain current @VGS=10V (Silicon limited)	$T_C = 25^\circ\text{C}$	226 A
ID	Continuous drain current @VGS=10V (Silicon limited)	$T_C = 100^\circ\text{C}$	159 A
ID	Continuous drain current @VGS=10V (Wire bond limited)	$T_C = 25^\circ\text{C}$	120 A
IDM	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	450 A
IDSM	Continuous drain current @VGS=10V	$T_A = 25^\circ\text{C}$	16 A
		$T_A = 70^\circ\text{C}$	13 A
EAS	Avalanche energy, single pulsed ②	210	mJ
PD	Maximum power dissipation	$T_C = 25^\circ\text{C}$	417 W
PDSM	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	2.1 W
TSTG,TJ	Storage and Junction Temperature Range	-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.3	0.36	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	60	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =40V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.7	2.3	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =60A	--	3.5	4.6	mΩ
		T _J =100°C	--	4.6	--	mΩ
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =30A	--	4.3	5.6	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	3105	6210	10865	pF
C _{oss}	Output Capacitance		280	560	980	pF
C _{rss}	Reverse Transfer Capacitance		175	350	615	pF
R _g	Gate Resistance	f=1MHz	0.2	0.7	5	Ω
Q _g (10V)	Total Gate Charge	V _{DS} =20V, I _D =60A, V _{GS} =10V	--	102	179	nC
Q _g (4.5V)	Total Gate Charge		--	48	84	nC
Q _{gs}	Gate-Source Charge		--	23	40	nC
Q _{gd}	Gate-Drain Charge		--	19	33	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =60A, R _G =3Ω, V _{GS} =10V	--	18	--	ns
T _r	Turn-on Rise Time		--	130	--	ns
T _{d(off)}	Turn-Off Delay Time		--	59	--	ns
T _f	Turn-Off Fall Time		--	101	--	ns
Source- Drain Diode Characteristics@ T_J = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =60A, V _{GS} =0V	--	0.9	1.2	V
T _{rr}	Reverse Recovery Time	I _{sd} =60A, V _{GS} =0V	--	18	36	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	8.4	17	nC

NOTE: ① Single pulse; pulse width ≤ 100μs.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 29A, V_{GS} = 10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

Typical Characteristics

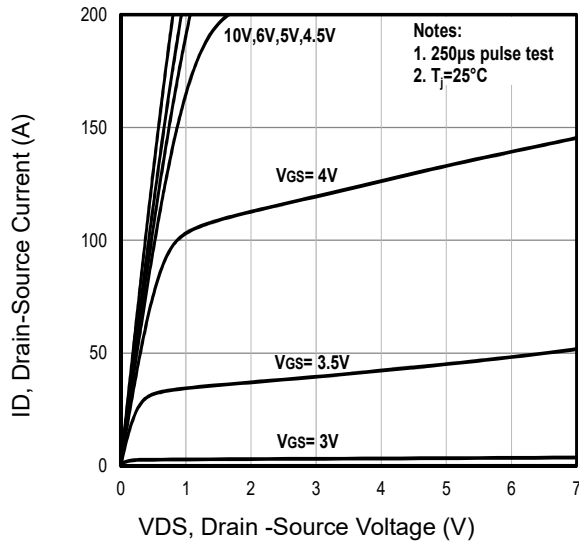


Fig1. Typical Output Characteristics

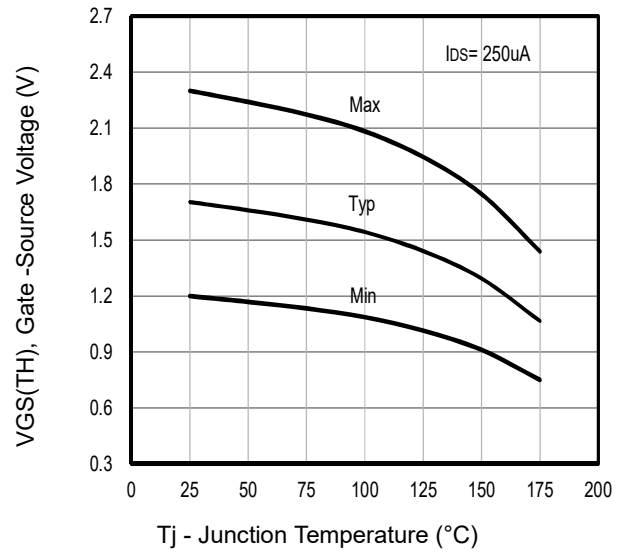


Fig2. Typical V_{GS(TH)} Gate-Source Voltage Vs. T_j

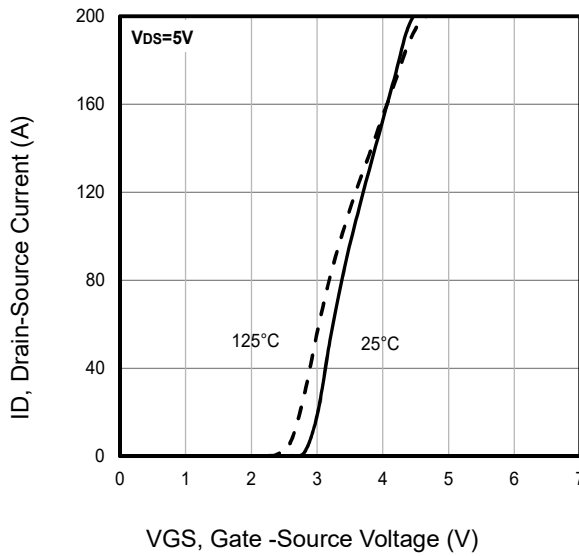


Fig3. Typical Transfer Characteristics

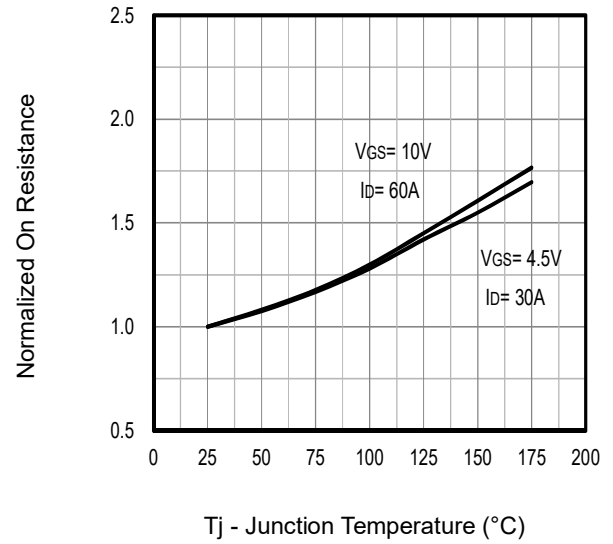


Fig4. Typical Normalized On-Resistance Vs. T_j

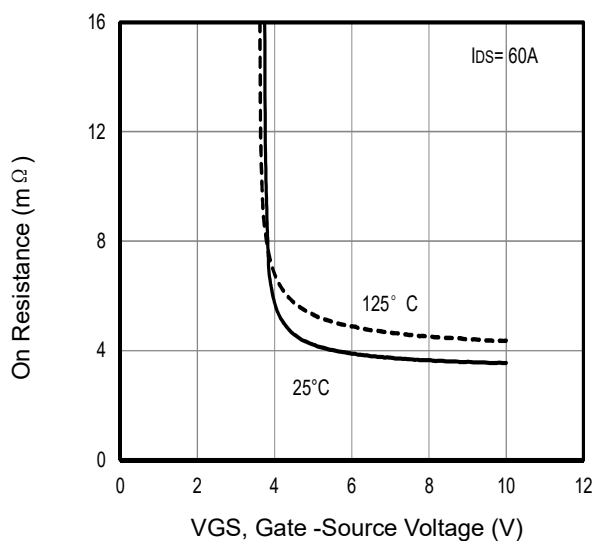


Fig5. Typical On Resistance Vs Gate-Source Voltage

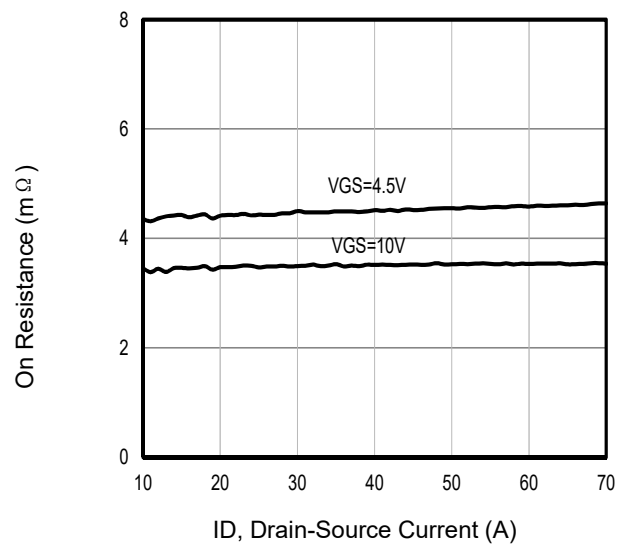


Fig6. Typical On Resistance Vs Drain Current and Gate Voltage

Typical Characteristics

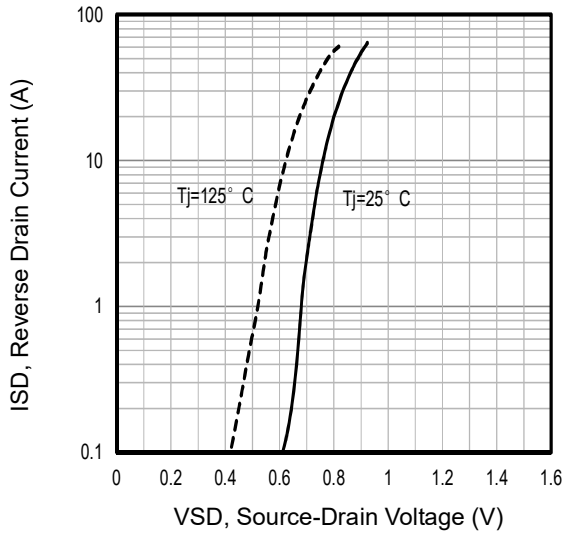


Fig7. Typical Source-Drain Diode Forward Voltage

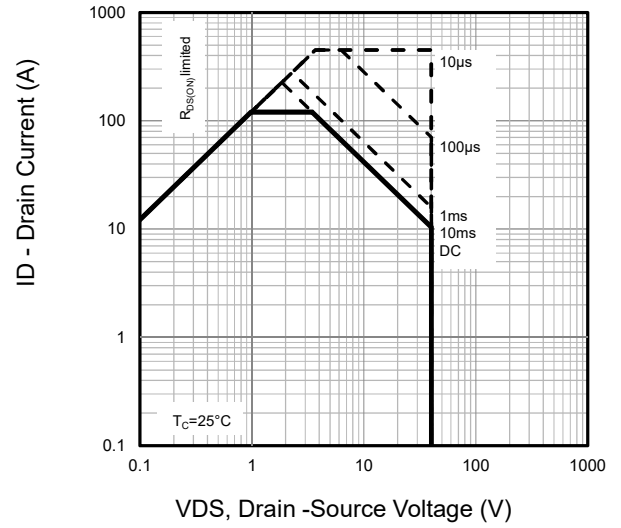


Fig8. Maximum Safe Operating Area

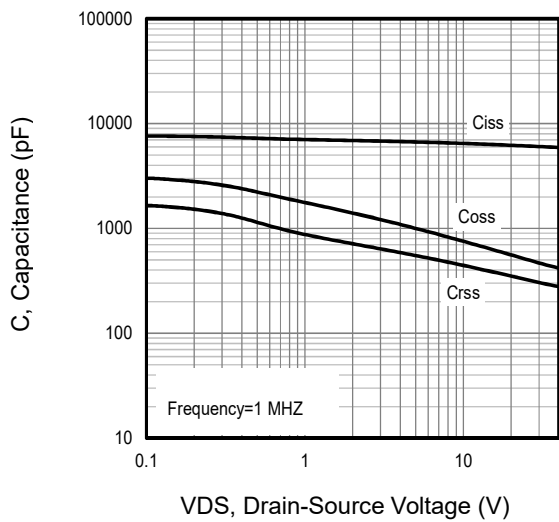


Fig9. Typical Capacitance Vs. Drain-Source Voltage

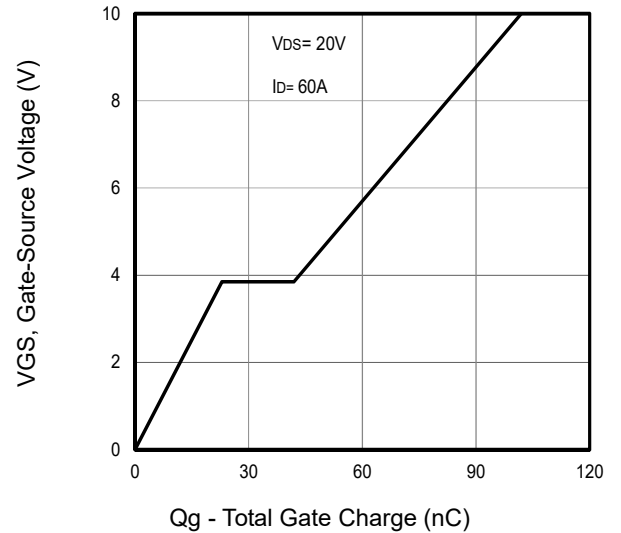


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

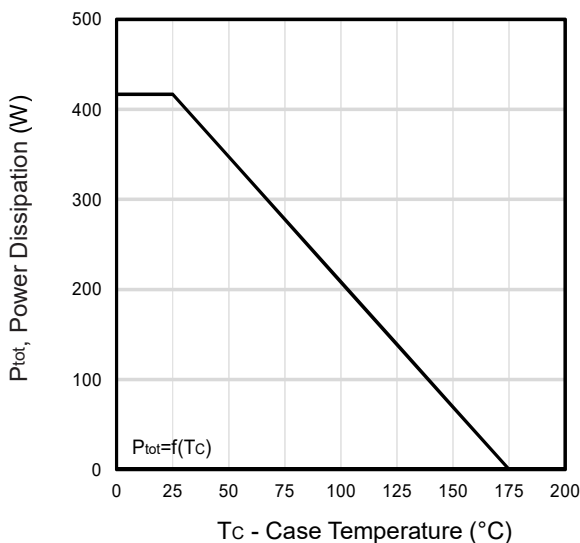


Fig11. Power Dissipation Vs. Case Temperature

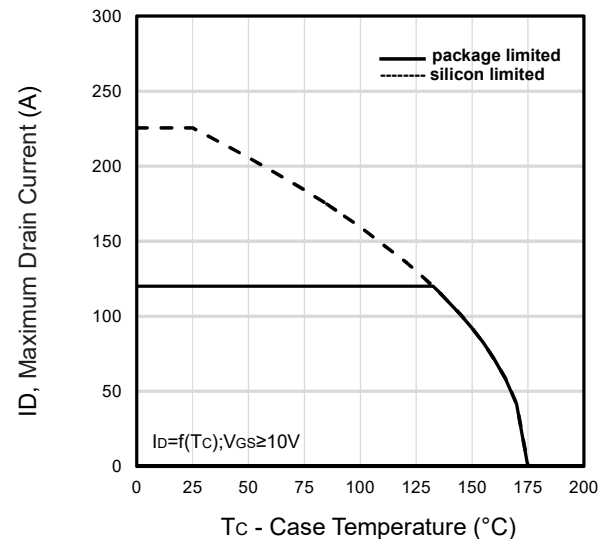


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

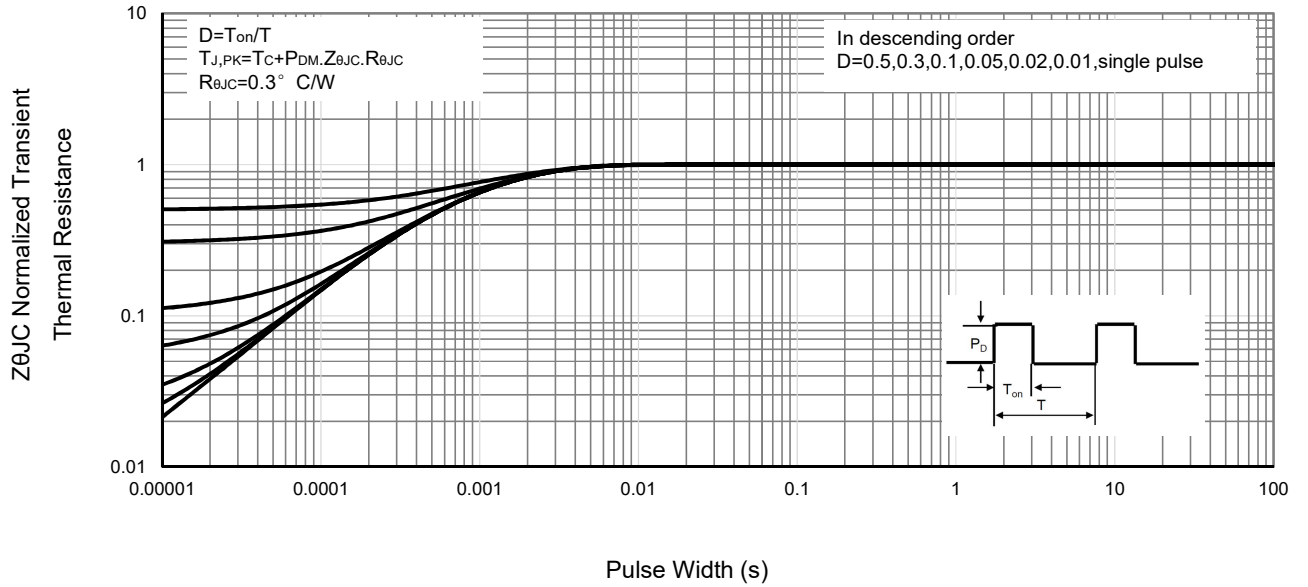


Fig13 . Normalized Maximum Transient Thermal Impedance

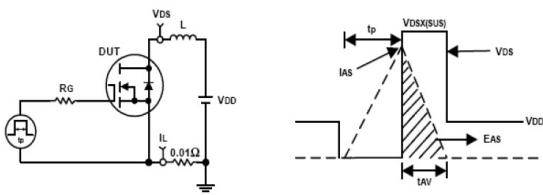


Fig14. Unclamped Inductive Test Circuit and waveforms

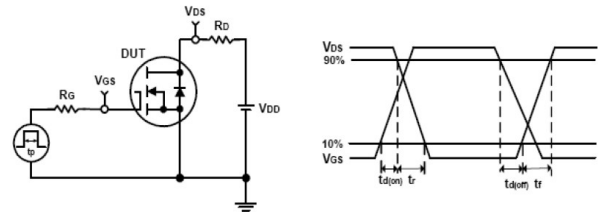
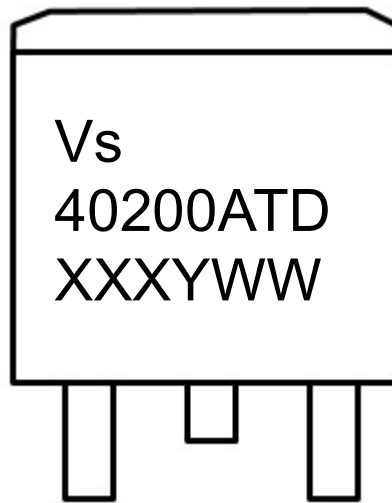


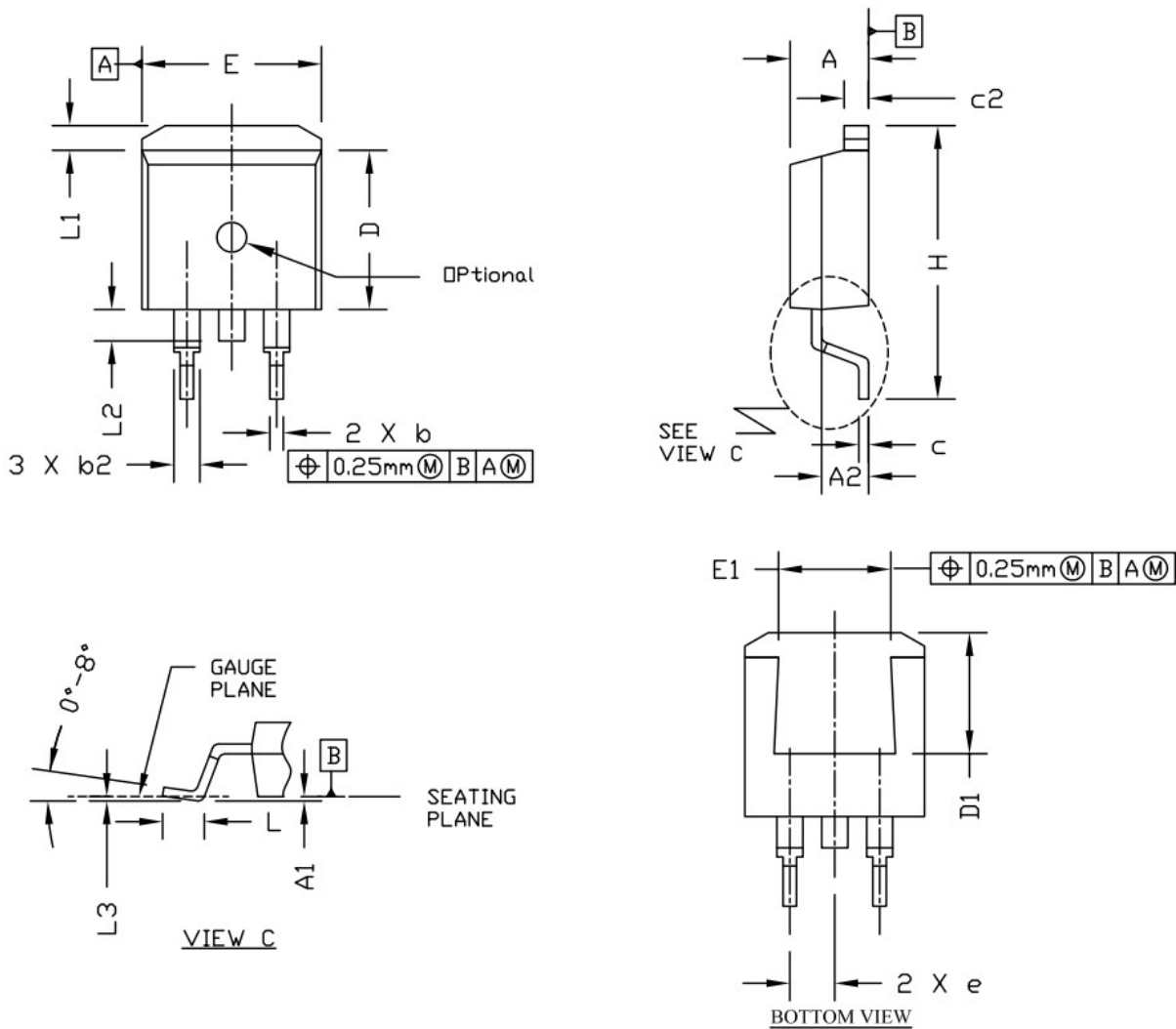
Fig15. Switching Time Test Circuit and waveforms

Marking Information



- 1st line: Vergiga Code (Vs)
- 2nd line: Part Number (40200ATD)
- 3rd line: Date code (XXXYWW)
 - XXX: Wafer Lot Number Code , code changed with Lot Number
 - Y: Year Code , refer to table below
 - WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-263 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.400	4.570	4.700
A1	0.000	0.100	0.200
A2	2.300	2.400	2.500
b	0.700	0.800	0.900
b2	1.200	1.270	1.360
c	0.381	0.500	0.737
c2	1.220	1.300	1.350
D	8.600	9.200	9.300
D1	6.860		
e	2.540 BSC		
E	9.780	9.880	10.260
E1	6.225		
H	14.700	15.100	15.500
L	2.000	2.550	2.750
L1	1.000	1.200	1.400
L2	1.300	1.600	1.700
L3	0.255 BSC		

Notes:

1. Refer to JEDEC TO-263 variation AB
2. Dimension "D" & "E" do NOT include mold flash, mold flash shall not exceed 0.127mm per side.

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[TK31J60W5,S1VQ\(O](#) [2SK2614\(TE16L1,Q\)](#) [DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#)
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[BSS340NWH6327XTSA1](#) [MCM3400A-TP](#) [DMTH10H4M6SPS-13](#) [IRF40SC240ARMA1](#) [IPS60R1K0PFD7SAKMA1](#)
[IPS60R360PFD7SAKMA1](#) [IPS60R600PFD7SAKMA1](#)